2M x 32 SDRAM

512K x 32bit x 4Banks
Synchronous DRAM

G-Link Technology Corporation

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DESCRIPTION

The G-Link GLT5640L32 is a high speed 67,108,864bits CMOS Synchronous DRAM organized as 4 banks of 524,288 words x 32 bits.

GLT5640L32 is offering fully synchronous operation and is referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

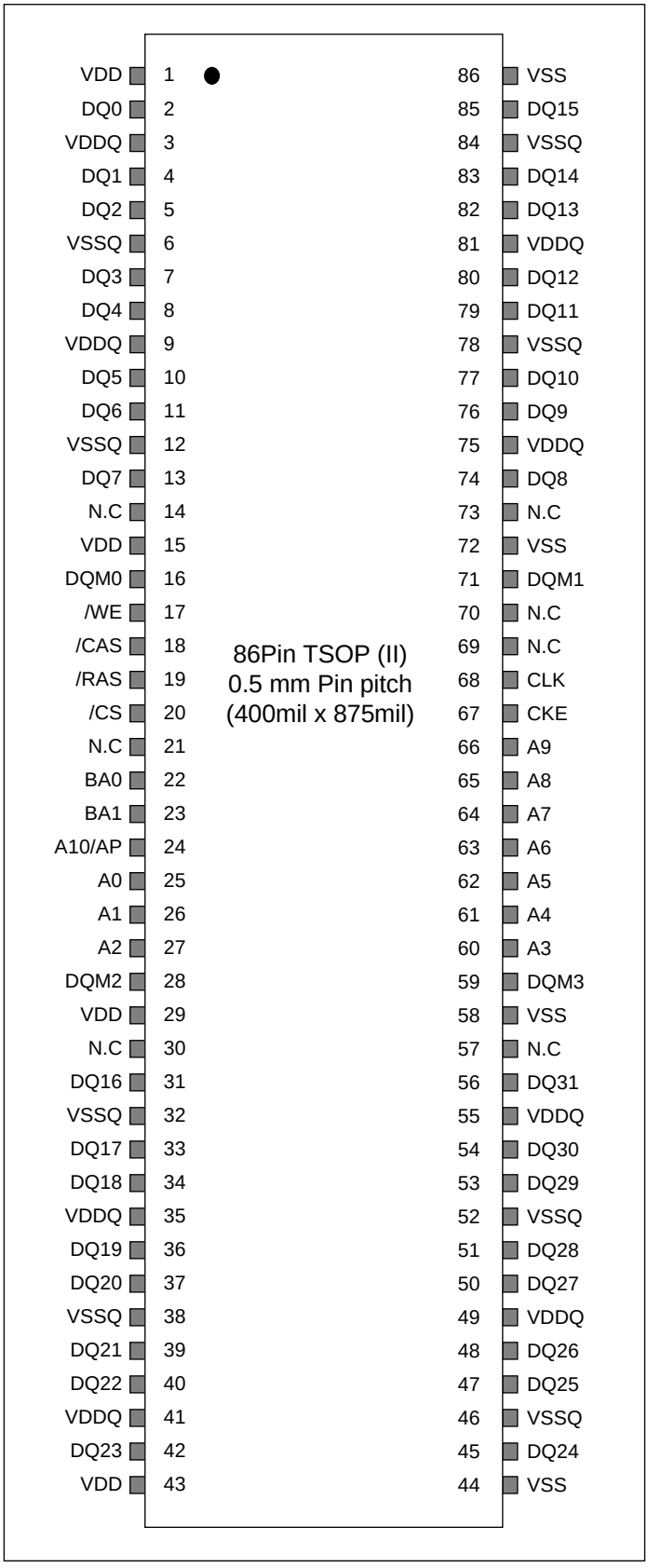
FEATURES

- JEDEC standard 3.3V power supply.
- Auto refresh and self refresh.
- All device pins are compatible with LVTTL interface.
- 4096 refresh cycle / 64ms.
- JEDEC standard 86pin 400mil TSOP-II with 0.5mm of pin pitch.
- Programmable Burst Length and Burst Type.
  - 1, 2, 4, 8 or Full Page for Sequential Burst.
  - 4 or 8 for Interleave Burst.
- Programmable CAS Latency : 2,3 clocks.
- All inputs and outputs referenced to the positive edge of the system clock.
- Data mask function by DQM0,1,2 and 3.
- Internal four banks operation.
- Burst Read Single Write operation.
- Automatic precharge, includes CONCURRENT Auto Precharge Mode and controlled Precharge

ORDERING INFORMATION

PART No.	CLOCK Freq.	POWER	ORGANIZATION	INTERFACE	PACKAGE
GLT5640L32-5 GLT5640L32 -5.5 GLT5640L32 -6 GLT5640L32 -7 GLT5640L32 -8 GLT5640L32 -10	200MHz 183MHz 166MHz 143MHz 125MHz 100MHz	Normal Power	4 Banks x 512K bits x 32	LVTTL	86pin 400mil TSOP-II

PIN ASSIGNMENT (TOP VIEW)



PIN DESCRIPTIONS

PIN	PIN NAME	DESCRIPTIONS
CLK	System Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip select	Enable or disable all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0~A10/AP	Address	Row Address : RA0~RA10, Column Address : CA0~CA7, Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input / Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0~DQ31	Data Input / Output	Multiplexed data input / output pin
VDD / VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ / VSSQ	Data Output Power / Ground	Power supply for output buffers
NC	No Connection	No connection

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT
Ambient Temperature	TA	0~70	°C
Storage Temperature	TSTG	-55~125	°C
Voltage on Any Pin relative to VSS	VIN,VOUT	-1.0~4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0~4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W

CAPACITANCE (TA=25 ℃ , f=1MHz, VDD=3.3V)

PARAMETER	PIN	SYMBOL	MIN	MAX	UNIT
Input Capacitance	CLK	CI1	2.5	4.0	pF
	A0~A10,BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM0~3	CI2	2.5	5.0	pF
Data Input / Output Capacitance	DQ0~DQ31	CI/O	4.0	6.5	pF

DC CHARACTERISTICS & OPERATING CONDITION (TA=0 to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1, 2
Input High Voltage	VIH	2.0	3.0	VDDQ+0.3	V	1, 3
Input Low Voltage	VIL	VSSQ-0.3	0	0.8	V	1, 4
Input Leakage Current	ILI	-1.0	-	1.0	uA	5
Output Leakage Current	ILO	-1.5	-	1.5.	uA	6
Output High Voltage	VOH	2.4	-	-	V	IOH = -2.0mA
Output Law Voltage	VOL	-	-	0.4	V	IOL = +2.0mA

Notice :

1. *All voltages are referenced to VSS =0V*
2. *VDD/VDDQ(min) is 3.15V for GLT5640L32-5/5.5/6*
3. *VIH(max) is acceptable 5.6V AC pulse width with ≤ 3ns of duration with no input clamp diodes*
4. *VIL(min) is acceptable –2.0V AC pulse width with ≤ 3ns of duration with no input clamp diodes*
5. *VIN = 0 to 3.6V, All other pins are not under test = 0*
6. *DOUT is disabled, VOUT=0 to 3.6V*

AC OPERATING CONDTION (TA=0 to 70°C, 3.0V≤VDD≤3.6V, VSS=0V - Note1)

PARAMETER	SYMBOL	TYP.	UNIT	NOTE
AC Input High / Low Level Voltage	VIH / VIL	2.4 / 0.4	V	-
Input Timing Measurement Reference Level Voltage	V_{trip}	1.4	V	-
Input Rise / Fall Time	tR / tF	1 / 1	ns	-
Output Timing Measurement Reference Level	V_{outref}	1.4	V	-
Output Load Capacitance for Access Time Measurement	CL	30	pF	2

DC CHARACTERISTICS (DC Operating Conditions Unless Otherwise Noted)

PARAMETER	SYM.	TEST CONDITION		SPEED						UNIT	NOTE
				5	-5.5	-6	-7	-8	-10		
Operating Current	IDD1	BURST Length = 1, One Bank Active tRAS ≥ tRAS(min), tRP ≥ tRP(min) IOL = 0 mA		230	220	200	1800	170	150	mA	1
Precharge Standby Current in Power-down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		2						mA	-
	IDD2PS	CKE ≤ VIL(max), tCK= ∞		2						mA	-
Precharge Standby Current in Non Power-down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK= 15ns Input signals are changed on time during 2CKLS All this pins ≥ VDD - 0.2 or ≤ 0.2V		30						mA	-
	IDD2NS	CKE ≥ VIH(min), tCK= ∞ Input signals are stable		20						mA	-
Active Standby Current in Power-down Mode	IDD3P	CKE ≥ VIL(max), tCK = 15ns		15						mA	-
	IDD3PS	CKE ≥ VIL(max), tCK= ∞		15						mA	-
Active Standby Current in Non Power-down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK=15ns Input signals are changed on time during 2CLKS All other pin ≥ VDD - 0.2V or ≤ 0.2V		60						mA	-
	IDD3NS	CKE ≥ VIH(min), tCK= ∞ Input signals are stable		50						mA	-
Operating Current (Burst Mode)	IDD4	tCK ≥ tCK(min) tRAS ≥ tRAS(min), IOL = 0 mA All Bank Active	CL=3	440	410	380	340	300	250	mA	1
			CL=2	-	-	-	-	250	200		
Operating Current	IDD5	tRRC ≥ tRRC(min) All banks active		250	240	220	200	190	180	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		2						mA	3

Notice :

1. *IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open*
2. *Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II*
3. *GLT5640L32-5/5.5/6/7/8/10*

AC CHARACTERISTICS - I (AC Operating Conditions Unless Otherwise Noted)

PARAMETER		SYM.	-5		-5.5		-6		-7		-8		-10		UNIT	NOTE
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CAS Latency = 3	tCK	5.0	1000	5.5	1000	6.0	1000	7.0	1000	8.0	1000	10.0	1000	ns	-
	CAS Latency = 2	tCK	-		-		-		-		10.0		12.0			
Clock High Pulse Width		tCHW	2.0	-	2.5	-	2.5	-	3.0	-	3.0	-	3.5	-		1
Clock Pulse Width		tCLW	2.0	-	2.5	-	2.5	-	3.0	-	3.0	-	3.5	-		1
Access Time from Clock	CAS Latency = 3	tAC	-	4.5	-	5.0	-	5.5	-	5.5	-	6.0	-	8.0		2
	CAS Latency = 2	tAC	-	-	-	-	-	-	-	-	-	8.0	-	8.0		
Data-out Hold Time		tOH	1.5	-	2.0	-	2.0	-	2.0	-	2.5	-	2.5	-		-
Input Signal Setup Time		tIS	1.5	-	1.5	-	1.5	-	1.75	-	2.0	-	2.5	-		1, 3
Input Signal Hold Time		tIH	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-		1, 3
CLK to Data Output in Low Z-Time		tOLZ	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-		-
CLK to Data Output in High Z-Time	CAS Latency = 3	tOHZ	-	4.5	-	5.0	-	5.5	-	5.5	-	6.0	-	6.0		-
	CAS Latency = 2	tOHZ	-	-	-	-	-	-	-	-	-	6.0	-	8.0		

Notice :

1. *Assume tR/tF (input rise and fall time) is 1ns. If tR & tF is longer than 1ns, transient time compensation should be considered.*
2. *If clock rising time is longer than 1ns, (tR/2-0.5) ns should be added to the parameter.*
3. *Setup and hold time for Data-Input, Address, CKE and Command pin*

AC CHARACTERISTICS - II (AC Operating Conditions Unless Otherwise Noted)

PARAMETER		SYM.	-5		-5.5		-6		-7		-8		-10		UNIT	NOTE
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	55	-	55	-	60	-	70	-	70	-	70	-	ns	1
	Auto Refresh	tRRC	55		55		60		70		70		70			
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	15	-	16.5	-	18	-	20	-	20	-	20	-		
$\overline{RAS}$ Active Time		tRAS	40	100K	38.5	100K	42	100K	49	100K	48	100K	50	100K		
$\overline{RAS}$ Precharge Time		tRP	15	-	16.5	-	18	-	20	-	20	-	20	-		
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	10	-	11	-	12	-	14	-	16	-	20	-		
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	1	-	1	-	1	-	CLK	-
Data-in to Precharge Command		tDPL	1	-	1	-	1	-	1	-	1	-	1	-		
Data-in to Active Command		tDAL	4	-	4	-	4	-	4	-	4	-	4	-		
DQM to Data-out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	2	-		
DQM to Data-in Mask		tDQM	0	-	0	-	0	-	0	-	0	-	0	-		
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	2	-	2	-		
Precharge to Data-out Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ	3	-	3	-	3	-	3	-	3	-	3	-		2
	$\overline{CAS}$ Latency = 2	tPROZ	-	-	-	-	-	-	-	-	2	-	2	-		
Power Down Exit Time		tPDE	1	-	1	-	1	-	1	-	1	-	1	-		-
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	1	-	1	-		3
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	-	64	ms	-

Notice :

1. *The minimum number of clock cycle is determined by dividing the minimum time required with clock cycle time and them rounding off to the next higher integer.*
2. *In case of row precharge interrupt, auto precharge and read burst stop.*
3. *A new command can be given tRC after self refresh exit.*

DEVICE OPERATING OPTION TABLE

GLT5640L32-5	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
200MHz (5.0ns)	3 CLKs	3CLKs	8CLKs	11CLKs	3CLKs	4.5 ns	1.5 ns
183MHz (5.5ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.0 ns	2.0 ns
166MHz (6.0ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5 ns	2.0 ns

GLT5640L32-5.5	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
183MHz (5.5ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.0 ns	2.0 ns
166MHz (6.0ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5 ns	2.0 ns
143MHz (7.0ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5 ns	2.0 ns

GLT5640L32-6	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
166MHz (6.0ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5 ns	2.0 ns
143MHz (7.0ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5 ns	2.0 ns
125MHz (8.0ns)	3 CLKs	3CLKs	6CLKs	9 CLKs	3CLKs	6.0 ns	2.5 ns

GLT5640L32-7	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
143MHz (7.0ns)	3 CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.5 ns	2.0 ns
125MHz (8.0ns)	3 CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6.0 ns	2.5 ns
100MHz (10.0ns)	2 CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6.0 ns	2.5 ns

GLT5640L32-8	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz (8.0ns)	3 CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6.0 ns	2.5 ns
100MHz (10.0ns)	2 CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6.0 ns	2.5 ns
83MHz (12.0ns)	2 CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6.0 ns	2.5 ns

GLT5640L32-10	$\overline{CAS}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz (10.0ns)	3 CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6.0 ns	2.5 ns
83MHz (12.0ns)	2 CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6.0 ns	2.5 ns
66MHz (15.0ns)	2 CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6.0 ns	2.5 ns

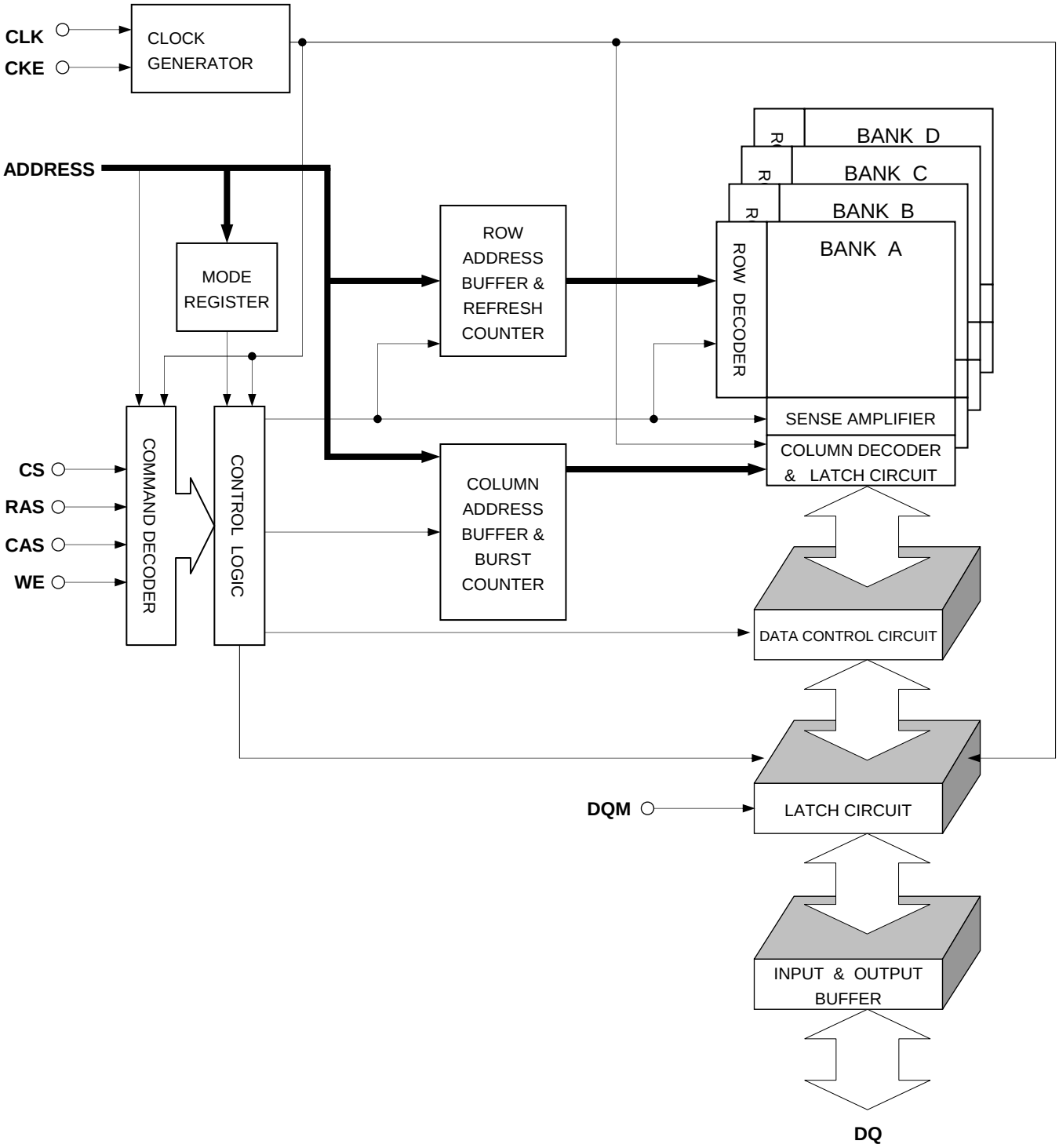
COMMAND TRUTH TABLE

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	NOTE
Read With Autoprecharge		H	X	L	L	L	L	X	OP Code			-
No Operation		H	X	L	X	X	X	X	X			-
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	-
Read		H	X	L	H	L	H	X	CA	L	V	-
Read With Autoprecharge										H		
Write		H	X	L	H	L	H	X	CA	L	V	-
Write With Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	-
Precharge Selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			-
DQM		H	X					V	X			-
Auto Refresh		H	H	L	L	L	H	X	X			-
Self Refresh	Entry	H	L	L	L	L	H	X	X			1
	Exit	L	H	H	X	X	X	X				1
				L	H	H	H					
Precharge Power Down	Exit	H	L	H	X	X	X	X	X			-
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				-
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			-
	Exit			L	V	V	V					
		L	H	X				X				-

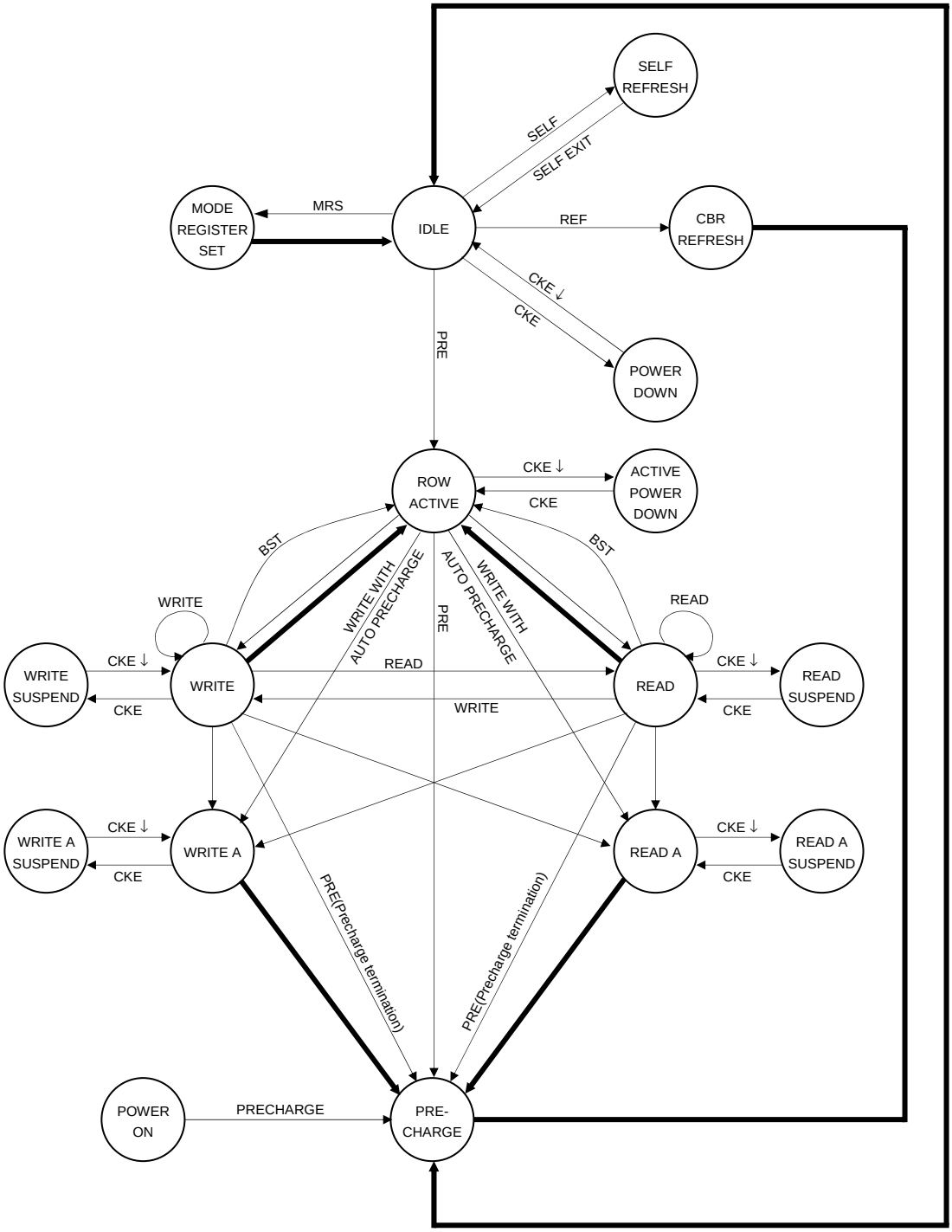
Notice :

1. *Exiting Self Refresh occurs by asynchronously bring CKE from low to high.*
2. ***X** = Don't Care, **H** = Logic High, **L** = Logic Low, **BA** = Bank Address, **RA** = Row Address, **CA** = Column Address, **OP Cpde** = Operand Code, **NOP** = No Operation.*

FUNCTIONAL DIAGRAM



SIMPLIFIED STATE DIAGRAM



FUNCTIONAL DESCRIPTION

In general, this 64Mb SDRAM (512K x 32 x 4 banks) is a quad-bank DRAM that operates at 3.3V and in-cludes a synchronous interface (all signals are regis-tered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 256 columns by 32-bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and con-tinue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A10 select the row). The address bits (A0-A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register defi-nition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and VDDQ (simulta-neously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100ms delay prior to issuing any command other than a COM-MAND INHIBIT or a NOP. Starting at some point during this 100ms period and continuing at least through the end of this period, COMMAND INHIBIT or NOP com-mands should be applied.

Once the 100ms delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register pro-gramming. Because the Mode Register will power up in an unknown state, it should be loaded prior to applying any operational command.

Register Definition

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 1. The Mode Register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode Register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or inter-leaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 is reserved for future use.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

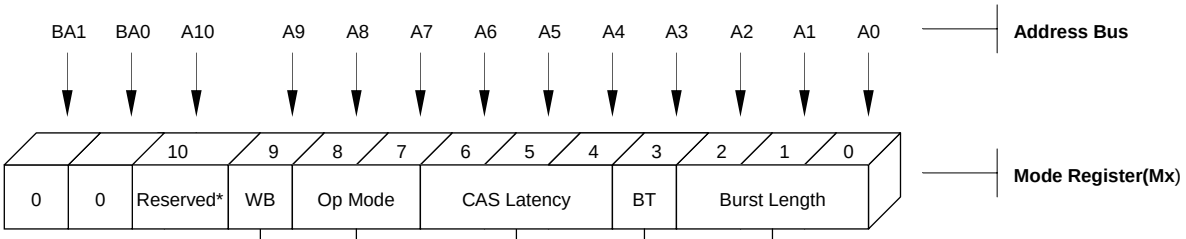
Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 when the burst length is set to two; by A2-A7 when the burst length is set to four; and by A3-A7 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3. The ordering of accesses within a burst is deter-mined by the burst length, the burst type and the starting column address, as shown in Table 1.



M8	M7	M6 - M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All Other States Reserved

M9	Burst Type
0	Programmed Burst Length
1	Single Location Access

M3	Burst Type
0	Sequential
1	Interleave

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M2 M1 M0	Burst Length	
	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	Reserved	Reserved
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

*Should Program M10 = 0,
to ensure compatibility with future device.

Figure 1.
Mode Register Definition

Burst Length	Starting Column Address			Order of Access Within a Burst	
				Type = Sequential	**Type = Interleaved**
2			**A0**		
			0	0>1	0>1
			1	1>0	1>0
4		**A1**	**A0**		
		0	0	0>1>2>3	0>1>2>3
		0	1	1>2>3>0	1>0>3>2
		1	0	2>3>0>1	2>3>0>1
		1	1	3>0>1>2	3>2>1>0
8	**A2**	**A1**	**A0**		
	0	0	0	0>1>2>3>4>5>6>7	0>1>2>3>4>5>6>7
	0	0	1	1>2>3>4>5>6>7>0	1>0>3>2>5>4>7>6
	0	1	0	2>3>4>5>6>7>0>1	2>3>0>1>6>7>4>5
	0	1	1	3>4>5>6>7>0>1>2	3>2>1>0>7>6>5>4
	1	0	0	4>5>6>7>0>1>2>3	4>5>6>7>0>1>2>3
	1	0	1	5>6>7>0>1>2>3>4	5>4>7>6>1>0>3>2
	1	1	0	6>7>0>1>2>3>4>5	6>7>4>5>2>3>0>1
	1	1	1	7>0>1>2>3>4>5>6	7>6>5>4>3>2>1>0
Full page (256)	N = A0 > A7 (Location 0>256)			C_n, C_n+1. C_n+2, C_n+3, C_n+4… …C_n-1, C_n...	Not Supported

Table 1.
Burst Definition

Notice :

1. *For a burst length of two, A1-A7 select the block-of-two burst; A0 selects the starting column within the block.*
2. *For a burst length of four, A2-A7 select the lock-of-four burst; A0-A1 select the starting column within the block.*
3. *For a burst length of four, A3-A7 select the lock-of-four burst; A0-A2 select the starting column within the block.*
4. *For a full-page burst, the full row is selected and A0-A7 select the starting column*
5. *Whenecer a boundart of the block is reached within a given sequence above, the following access wraps within the block.*
6. *For a burst length of one, A0-A7 select the unique column to be accessed, and Mode Register bit M3 is ignored.*

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The atency can be set to one, two or three clocks. If a READ command is registered at clock edge n, and the latency is *m* clocks, the data will be available by clock edge *n* + m. The DQs will start driving as a result of the clock edge one cycle earlier *(n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2. Table 2 below,

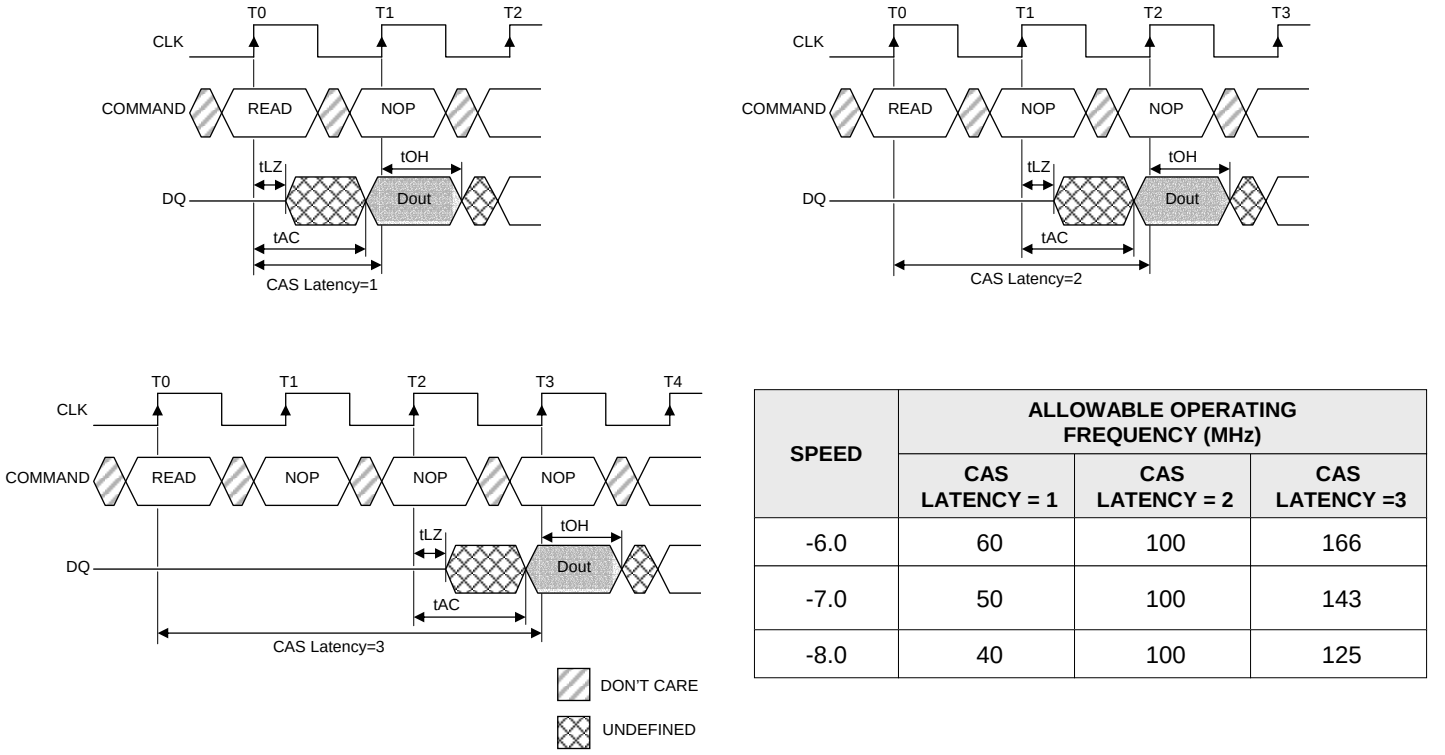


Figure 2.
CAS Latency

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)		
	CAS LATENCY = 1	CAS LATENCY = 2	CAS LATENCY =3
-6.0	60	100	166
-7.0	50	100	143
-8.0	40	100	125

Table 2.
CAS Latency

indicates the operating frequencies at which each CAS latency setting can be used. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

COMMANDS

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The Mode Register is loaded via inputs A0-A10. See Mode Register heading in the Register Definition sec-tion. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A0-A10 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0 and BA1 (B1) inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE iis not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQMx signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQMx signal was registered LOW, the corresponding DQs will provide valid data. DQM0 corresponds to DQ0-DQ7, DQM1 corresponds to DQ8-DQ15, DQM2 corresponds to DQ16-DQ23 and DQM3 corresponds to DQ24-DQ31.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE com-mand.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analagous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 64Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (tREF), regardless of width option. Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to t RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing con-straints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for tXSR because time is required for the completion of any internal refresh in progress.

Operation

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. See Figure 4.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be issued. For example, at RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 3, which covers any case where 2 < t RCD (MIN)/tCK . 3. (The same procedure is used to convert other specification limits from time units to clock cycles.) A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access over-head. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

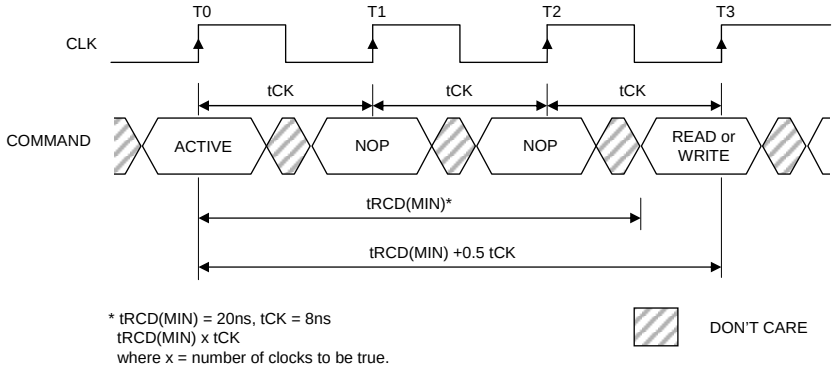


Figure 3.
Example : Meeting tRCD(MIN) When 2 < tRCD(MIN)/tCK . 3

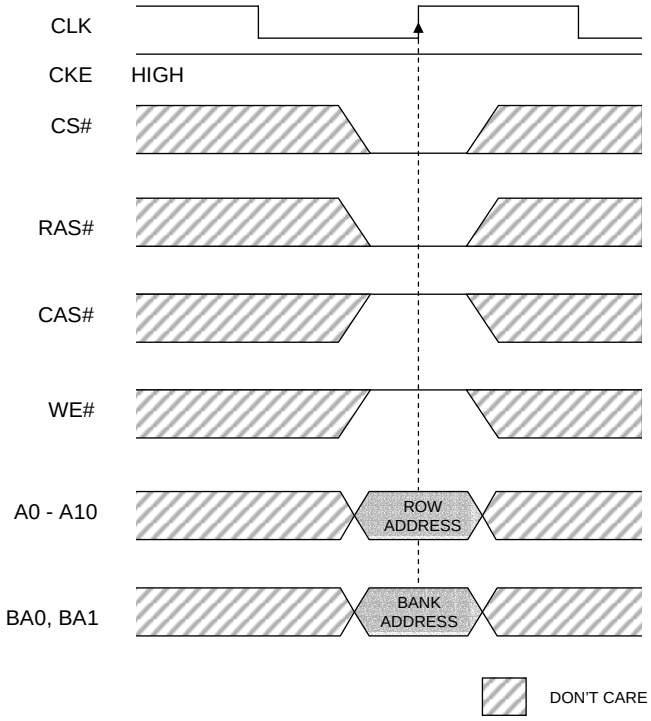


Figure 4.
Activating a Specific Row in a Specific Bank

READ Operation

READ bursts are initiated with a READ command, as shown in Figure 5. The starting column and bank addresses are pro-vided with the READ command, and AUTOPRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 6 shows general timing for each possible CAS latency setting.

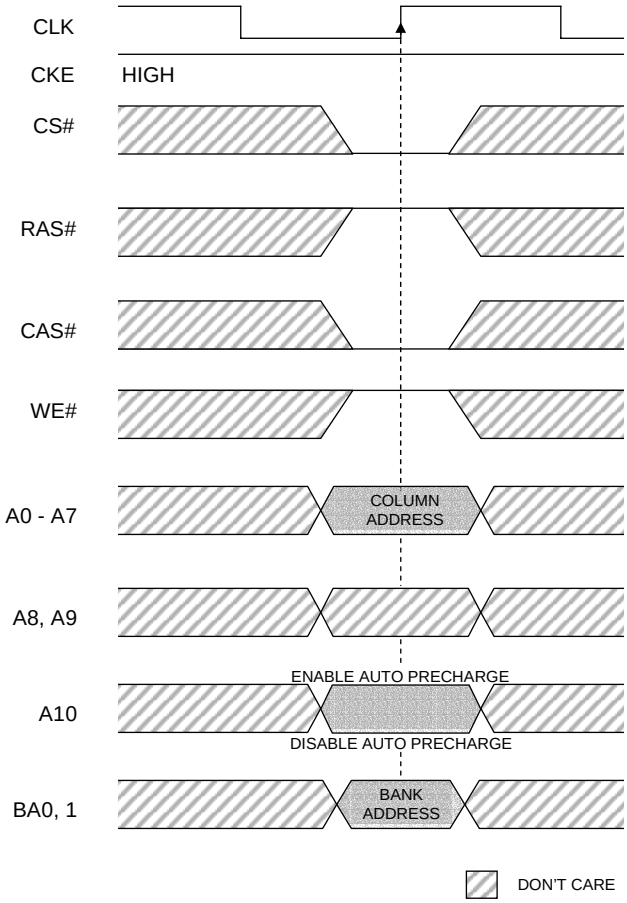


Figure 5.
READ Command

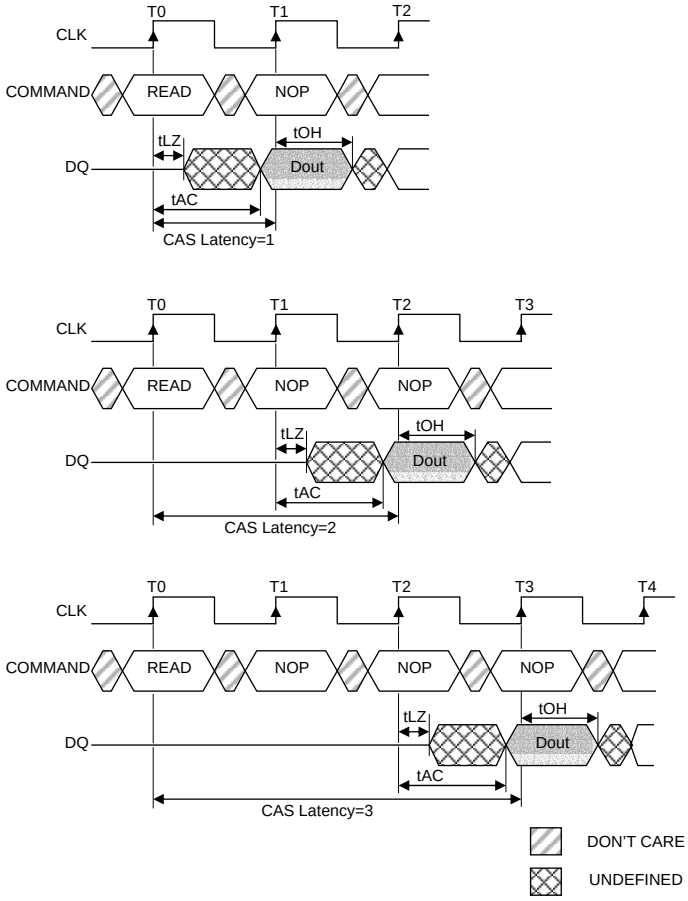


Figure 6.
CAS Latency

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continu-ous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one.

This is shown in Figure 7 for CAS latencies of one, two and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. This 64Mb SDRAM uses a pipelined architecture and therefore does not require the *2n* rule associated with a prefetch architecture.

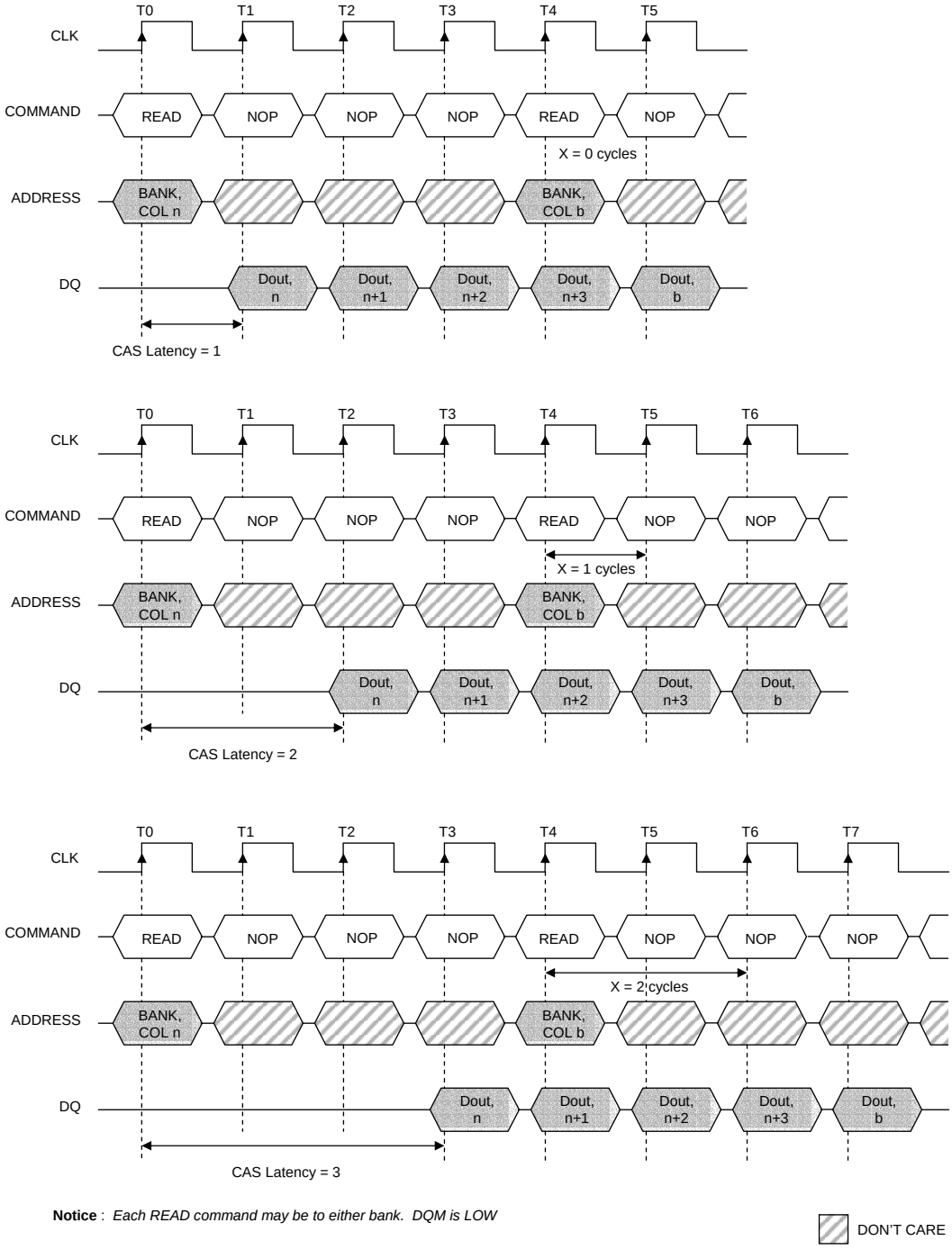


Figure 7.
Consecutive READ Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 8, or each subsequent READ may be performed to a different bank.

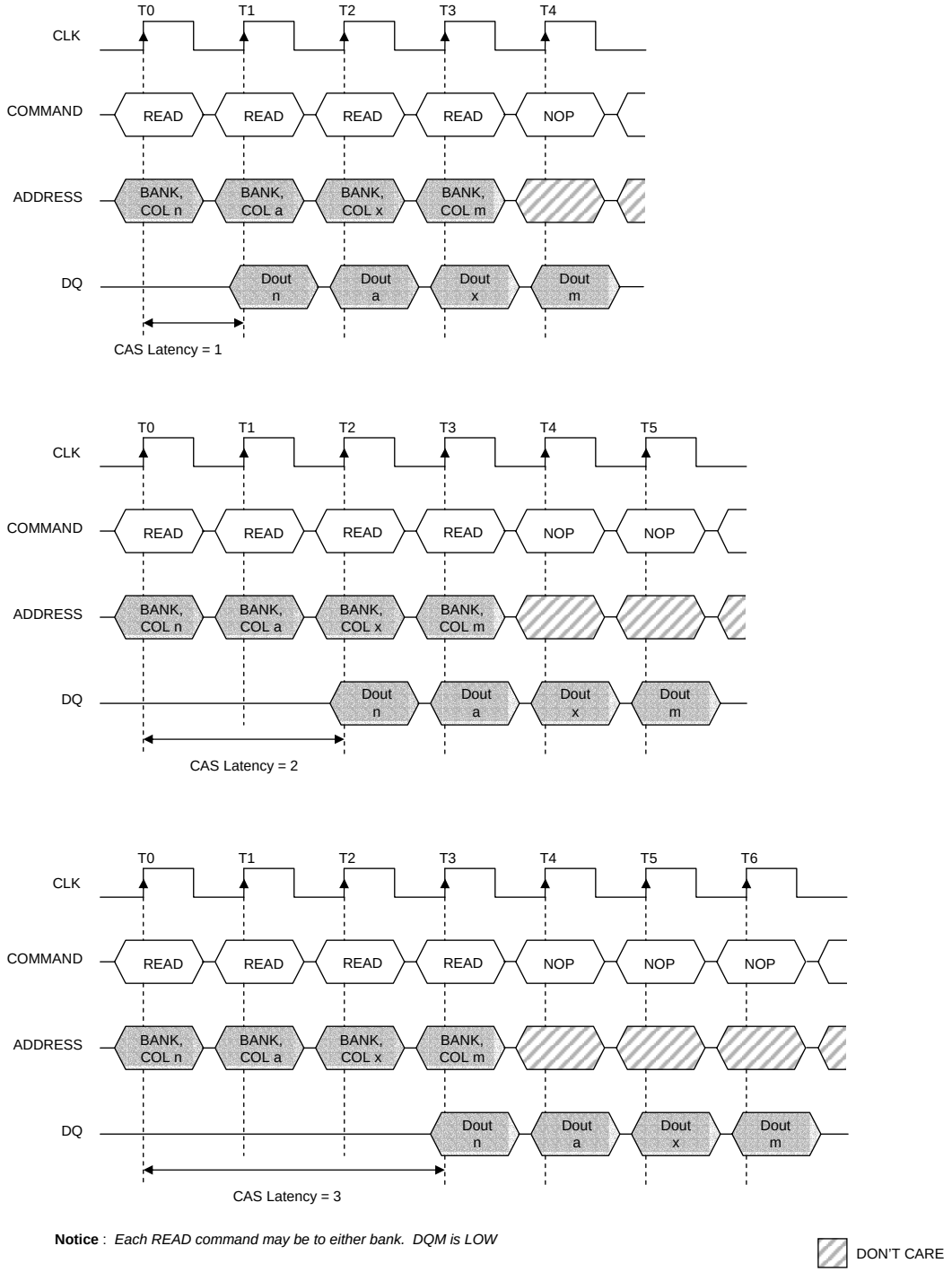
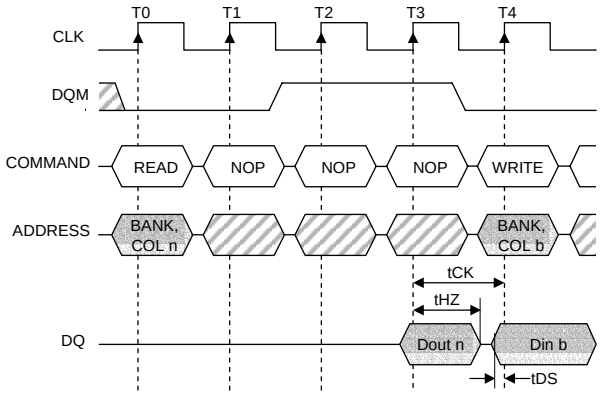


Figure 8.
Random READ Access

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turn-around limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

The DQM input is used to avoid I/O contention, as shown in Figures 9 and 10. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buff-ers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal; provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was low during T4 in Figure 10, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

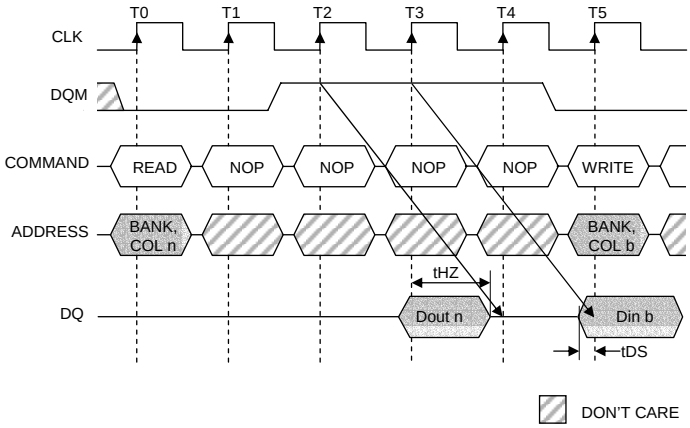
The DQM signal must be deasserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 9 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 10 shows the case where the additional NOP is needed.



Notice :

A CAS latency of three is used for illustration. The READ command may be to any bank,and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

Figure 9.
READ to WRITE



Notice :

A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank.

Figure 10.
READ to WRITE With Extra Clock Cycle

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not acti-vated), and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 11 for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data element(s). In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same

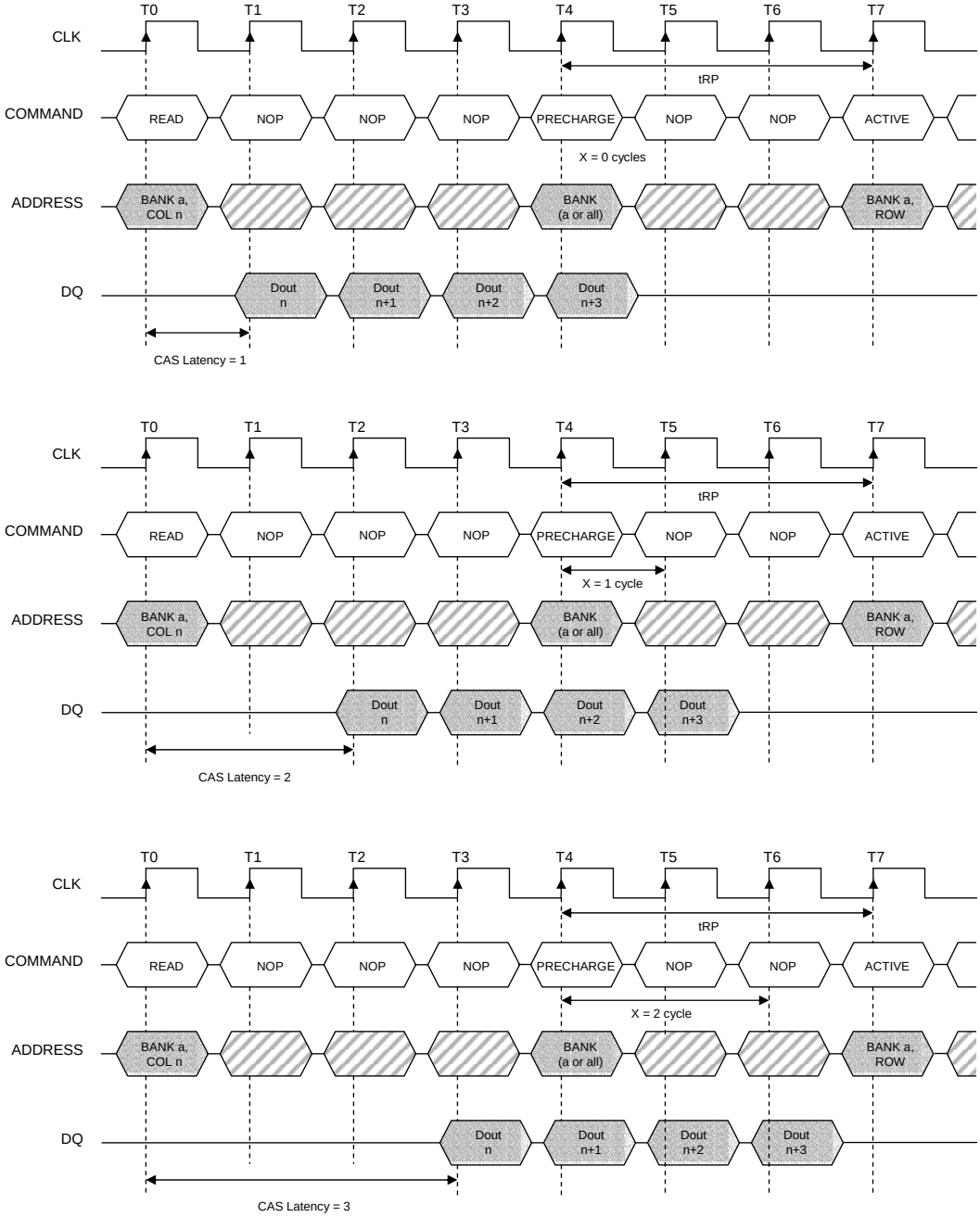


Figure 11.
READ to PRECHARGE

operation that would result from the same fixed-length burst with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that AUTO PRECHARGE was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 12 for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

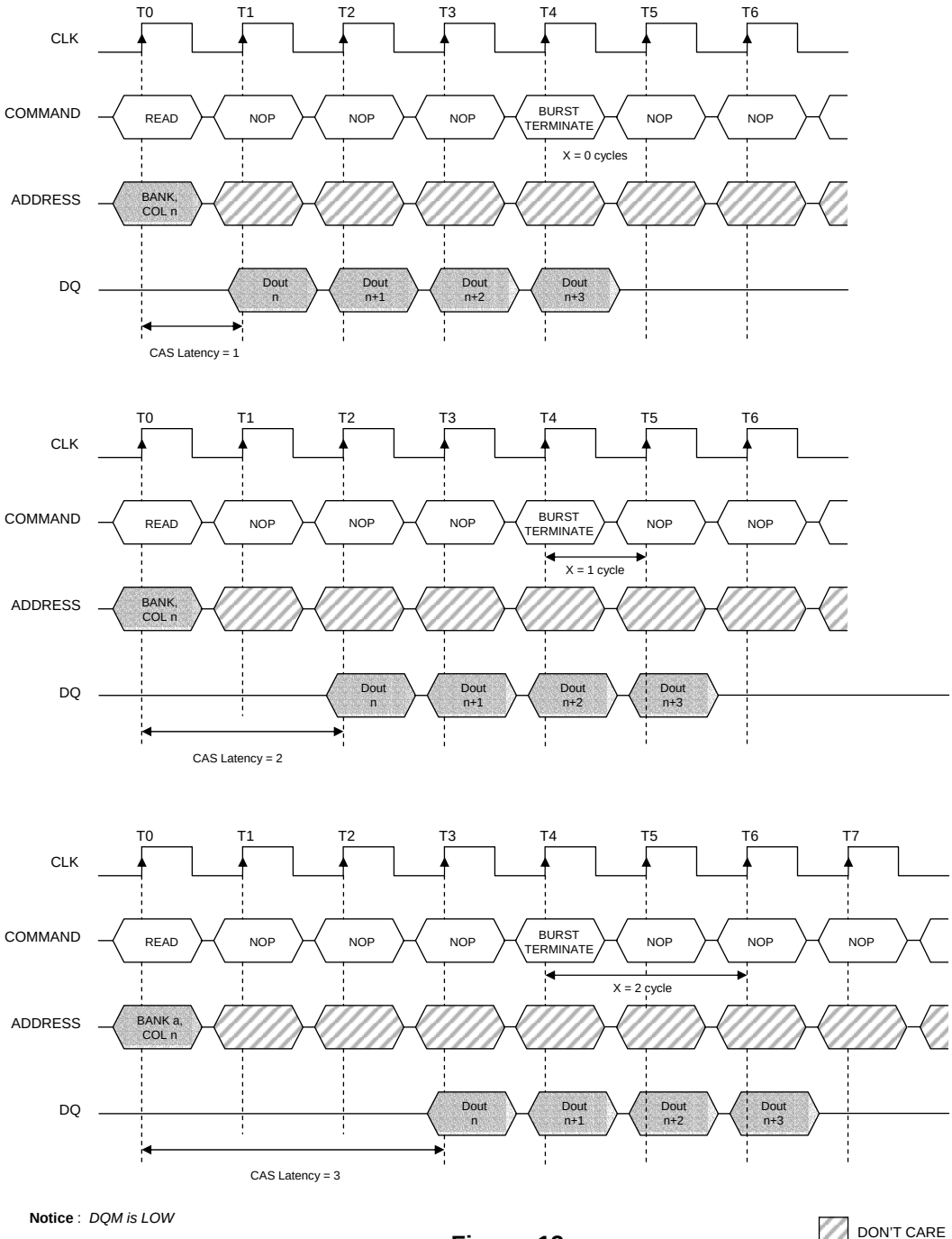


Figure 12.
Terminating a READ Burst

WRITE Operation

WRITE bursts are initiated with a WRITE command, as shown in Figure 13. The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled. During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 14). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous

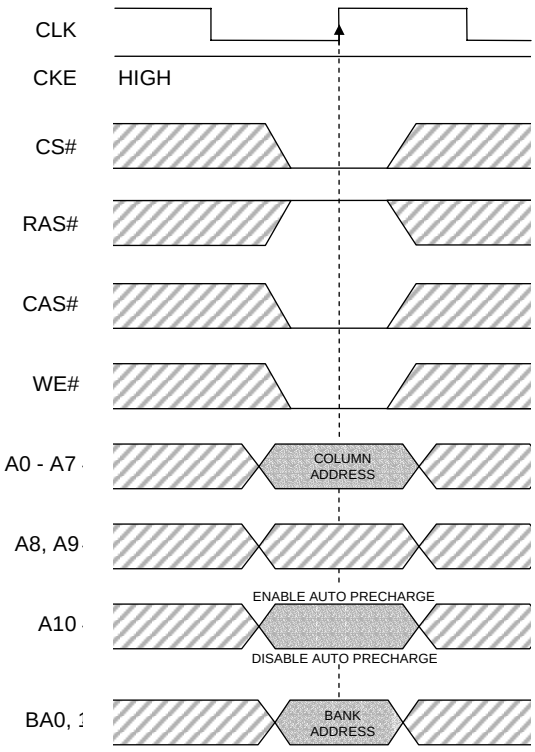
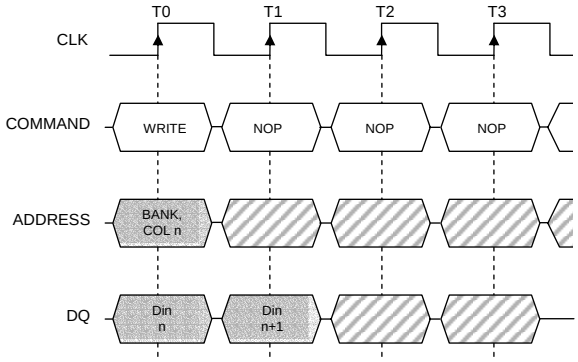
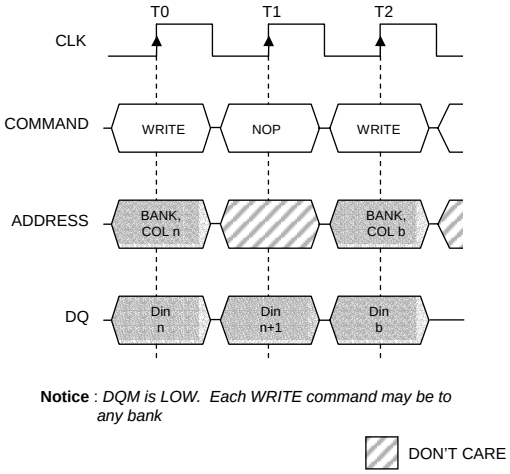


Figure 13.
WRITE Command



Notice : *Burst length = 2. DQM is LOW*

Figure 14.
WRITE Burst



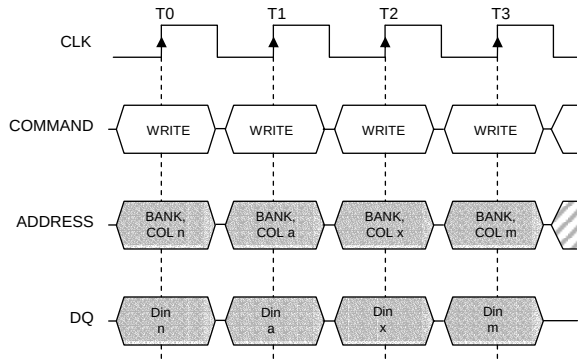
Notice : *DQM is LOW. Each WRITE command may be to any bank*

Figure 15.
WRITE to WRITE

WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 15. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. This 64Mb SDRAM uses a pipelined architecture and therefore does not require the *2n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 16, or each subsequent WRITE may be performed to a different bank.

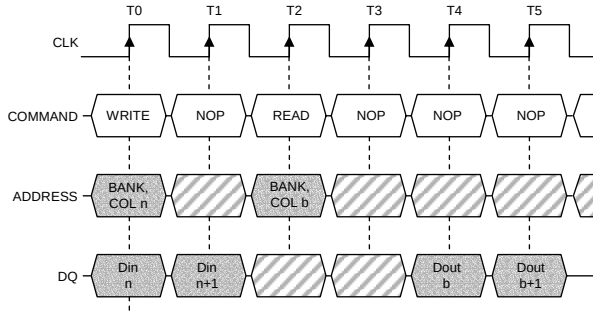
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is regis-tered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in Figure 17. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be fol-lowed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued t WR after the clock edge at which the last desired input data element is registered. The "two-clock" write-back requires at least one clock plus time, regardless of frequency,



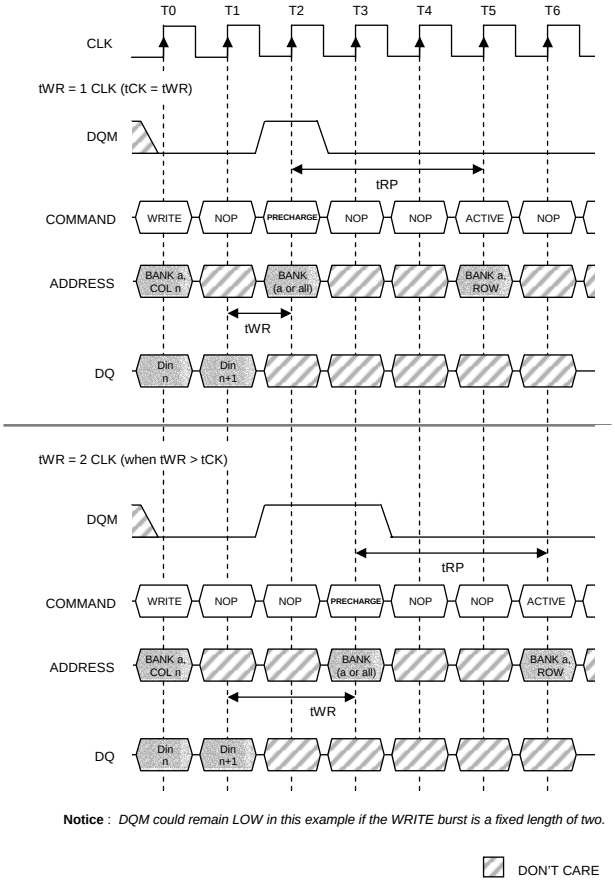
Notice : *Each WRITE command may be to any bank. DQM is LOW.*

Figure 16.
Random WRITE Cycle



Notice : *The WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW. CAS latency = 2 for illustration.*

Figure 17.
WRITE to READ



Notice : *DQM could remain LOW in this example if the WRITE burst is a fixed length of two.*

Figure 18.
WRITE to PRECHARGE

in auto precharge mode. In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 18. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. The precharge will actually begin coincident with the clock-edge (T2 in Figure 18) on a "one-clock" tWR and sometime between the first and second clock on a "two-clock" tWR (between T2 and T3 in Figure 18.) In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Fixed-length or full-page WRITE bursts can be trun-cated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coin-cident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 19, where data *n* is the last desired data element of a longer burst.

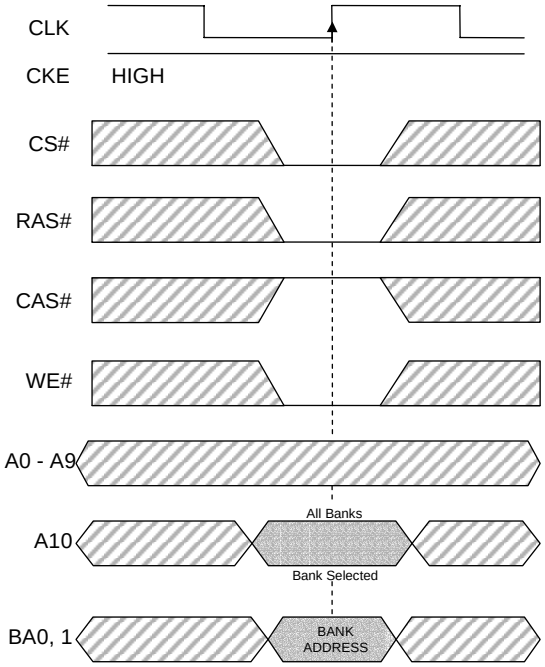


Figure 20.
PRECHARGE Command

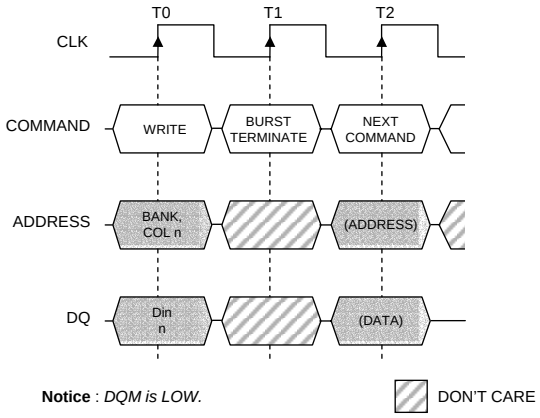


Figure 19.
Terminating a WRITE Burst

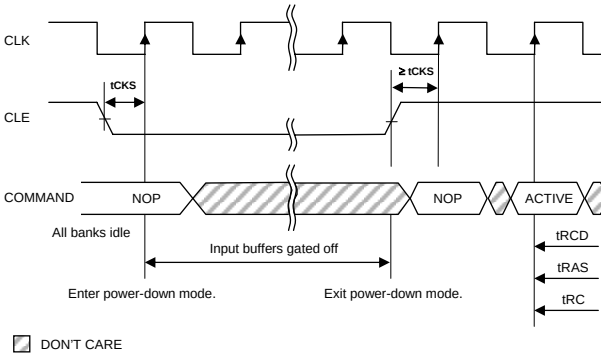


Figure 21.
Power-Down

PRECHARGE

The PRECHARGE command (Figure 20) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0 and BA1 select the bank. When all banks are to be precharged, inputs BA0 and BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress (see Figure 21). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in either bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode. The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting tCKS).

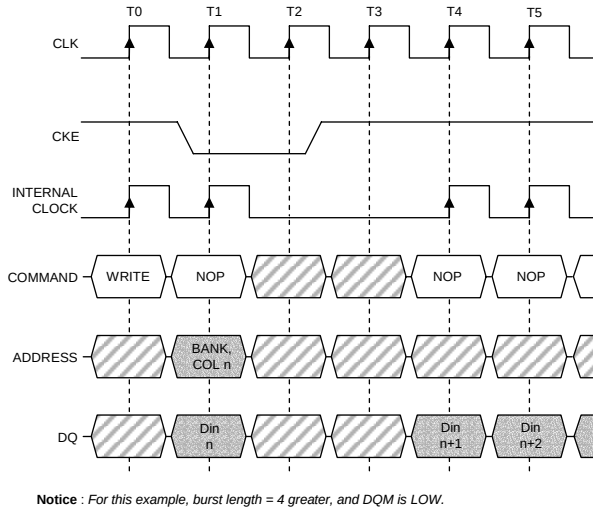
CLOCK SUSPEND

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, “freezing” the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is sus-pended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figures 22 and 23.) Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

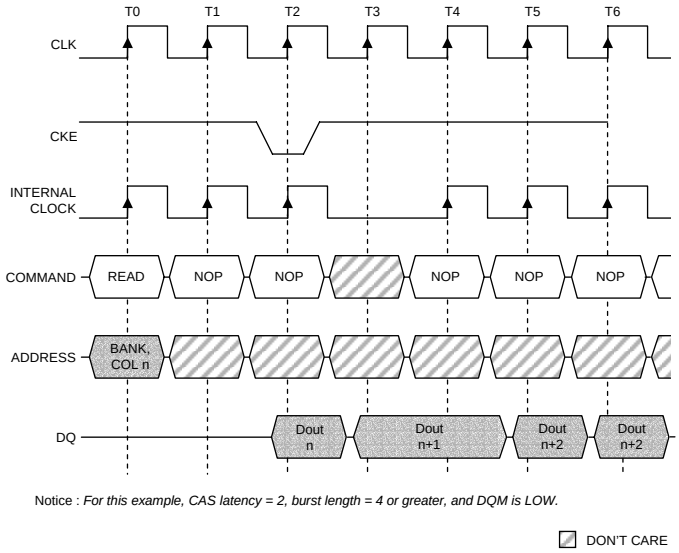
BURST READ/SINGLE WRITE

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the Mode Register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).



Notice : *For this example, burst length = 4 greater, and DQM is LOW.*

Figure 22.
Clock Suspend During WRITE Burst



Notice : *For this example, CAS latency = 2, burst length = 4 or greater, and DQM is LOW.*

Figure 23.
Clock Suspend During READ Burst

CONCURRENT AUTO PRECHARGE

An access command to (READ or WRITE) another bank while an access command with AUTOPRECHARGE enabled is executing is not allowed by SDRAMs, unless the SDRAM supports CONCURRENT AUTO PRECHARGE. SDRAMs support CONCURRENT AUTO PRECHARGE. Four cases where CONCURRENT AUTO PRECHARGE occurs are defined below.

READ with AUTO PRECHARGE

1. Interrupted by a READ (with or without AUTO PRECHARGE): A READ to bank *m* will interrupt a READ on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 24).
2. Interrupted by a WRITE (with or without AUTO PRECHARGE): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 25).

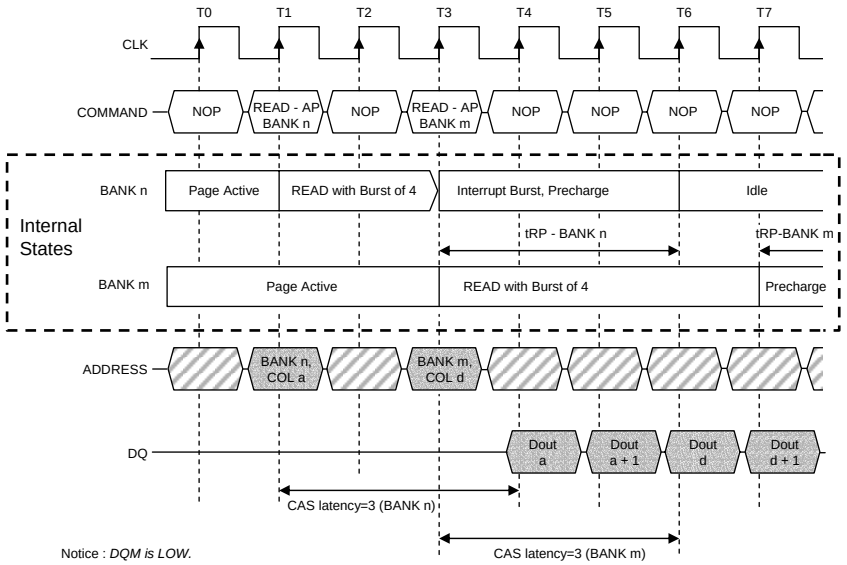


Figure 24.
READ With Auto Precharge Interrrupted by a READ

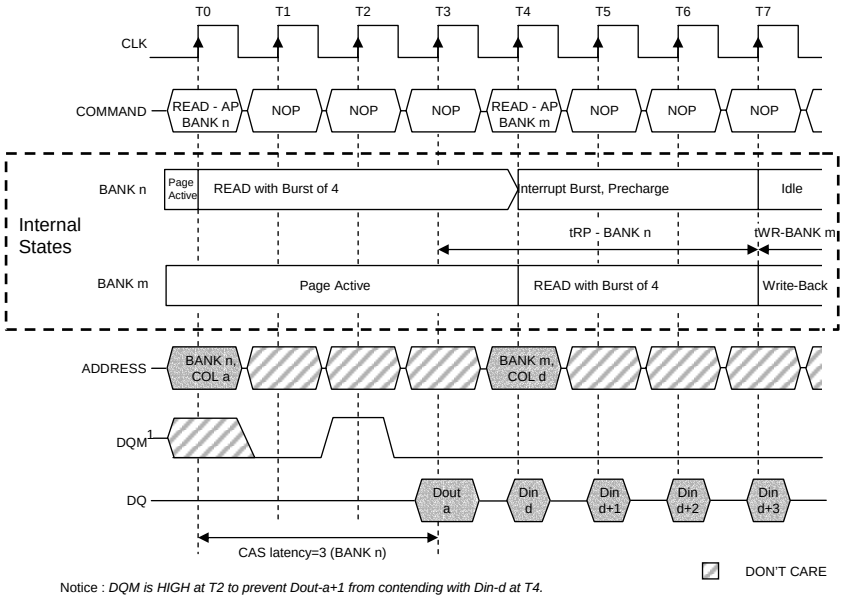


Figure 25.
READ With Auto Precharge Interrrupted by a WRITE

WRITE with AUTO PRECHARGE

3. Interrupted by a READ (with or without AUTO PRECHARGE): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank *n* will begin after tWR is met, where tWR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 26).
4. Interrupted by a WRITE (with or without AUTO PRECHARGE): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after tWR is met, where tWR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (Figure 27).

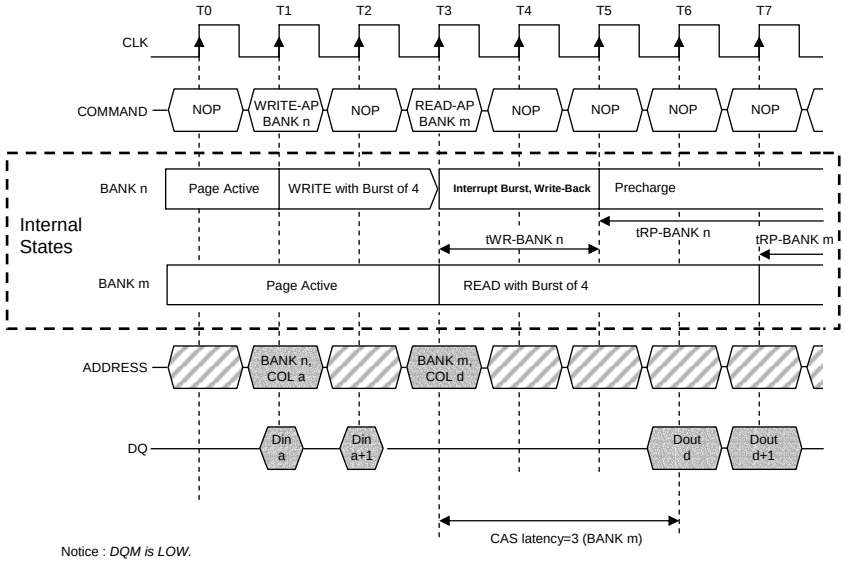


Figure 26.
WRITE With Auto Precharge Interrrupted by a WRITE

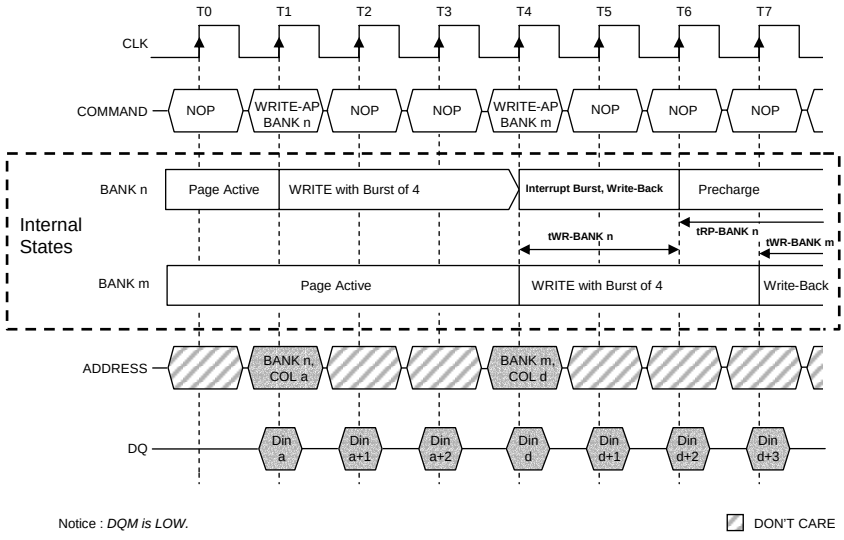


Figure 27.
WRITE With Auto Precharge Interrrupted by a READ

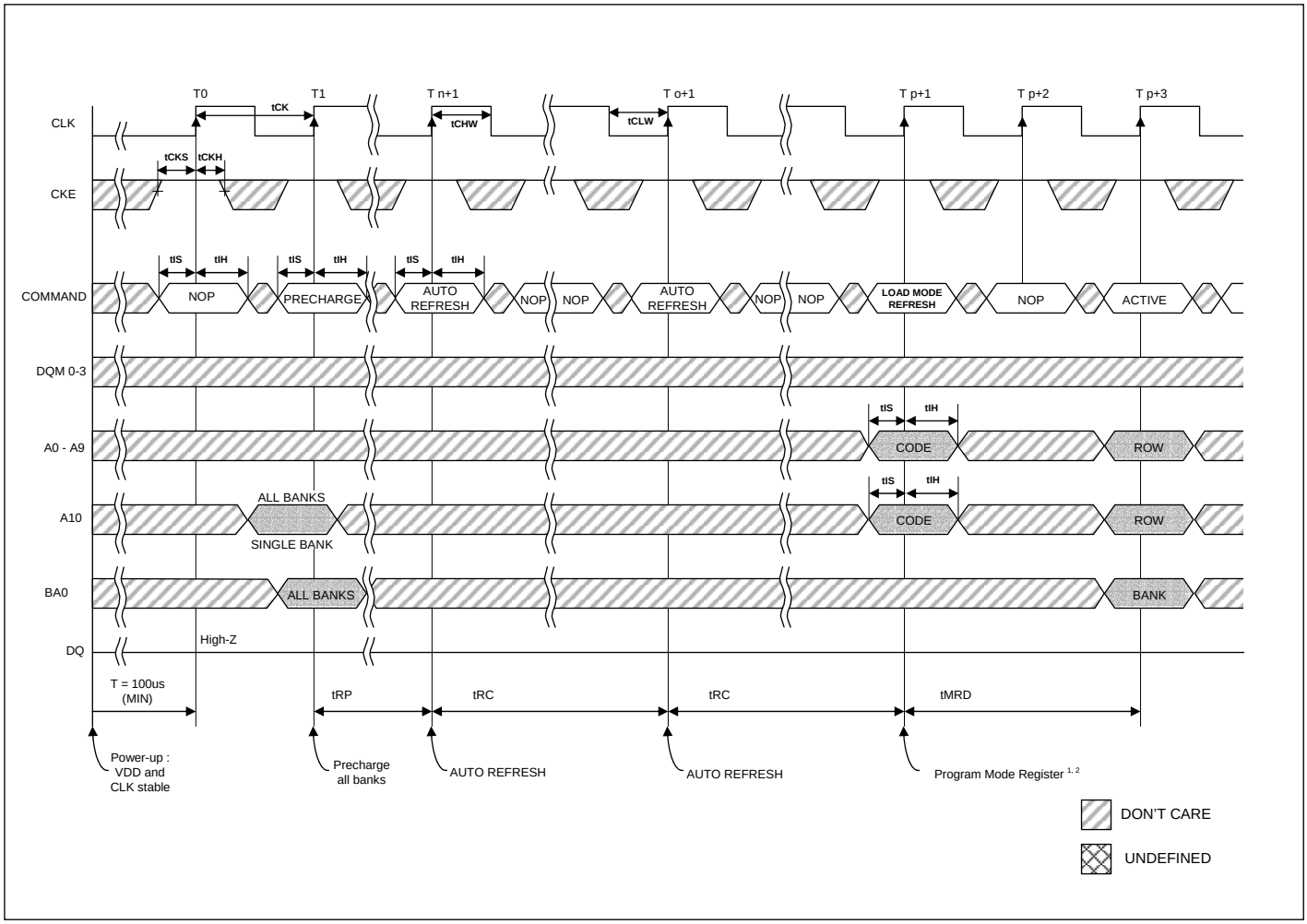
TIMING WAVEFORMS

INITIALIZE AND LOAD MODE REGISTER

Notice :

[1] The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.

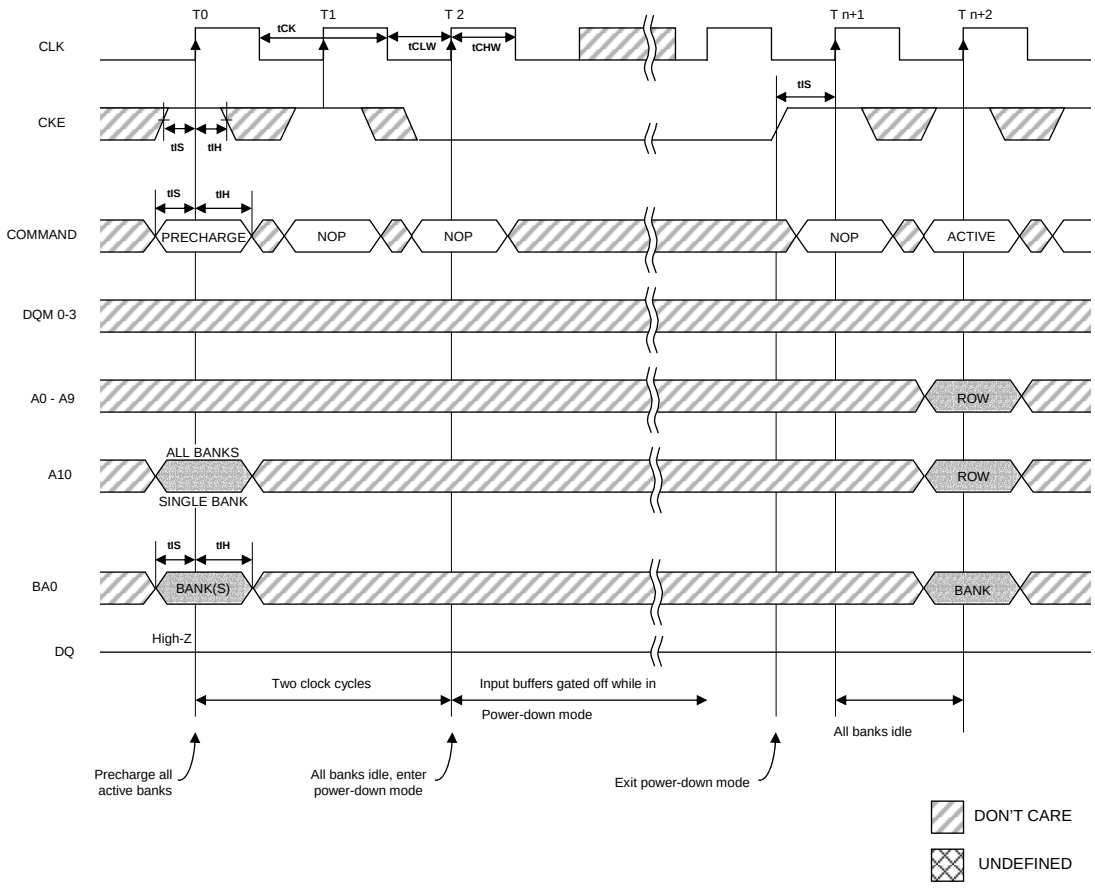
[2] Outputs are guaranteed High-Z after command is issued.



POWER-DOWN MODE [1]

Notice :

[1] *Violating refresh requirements during power-down may result in a loss of data.*

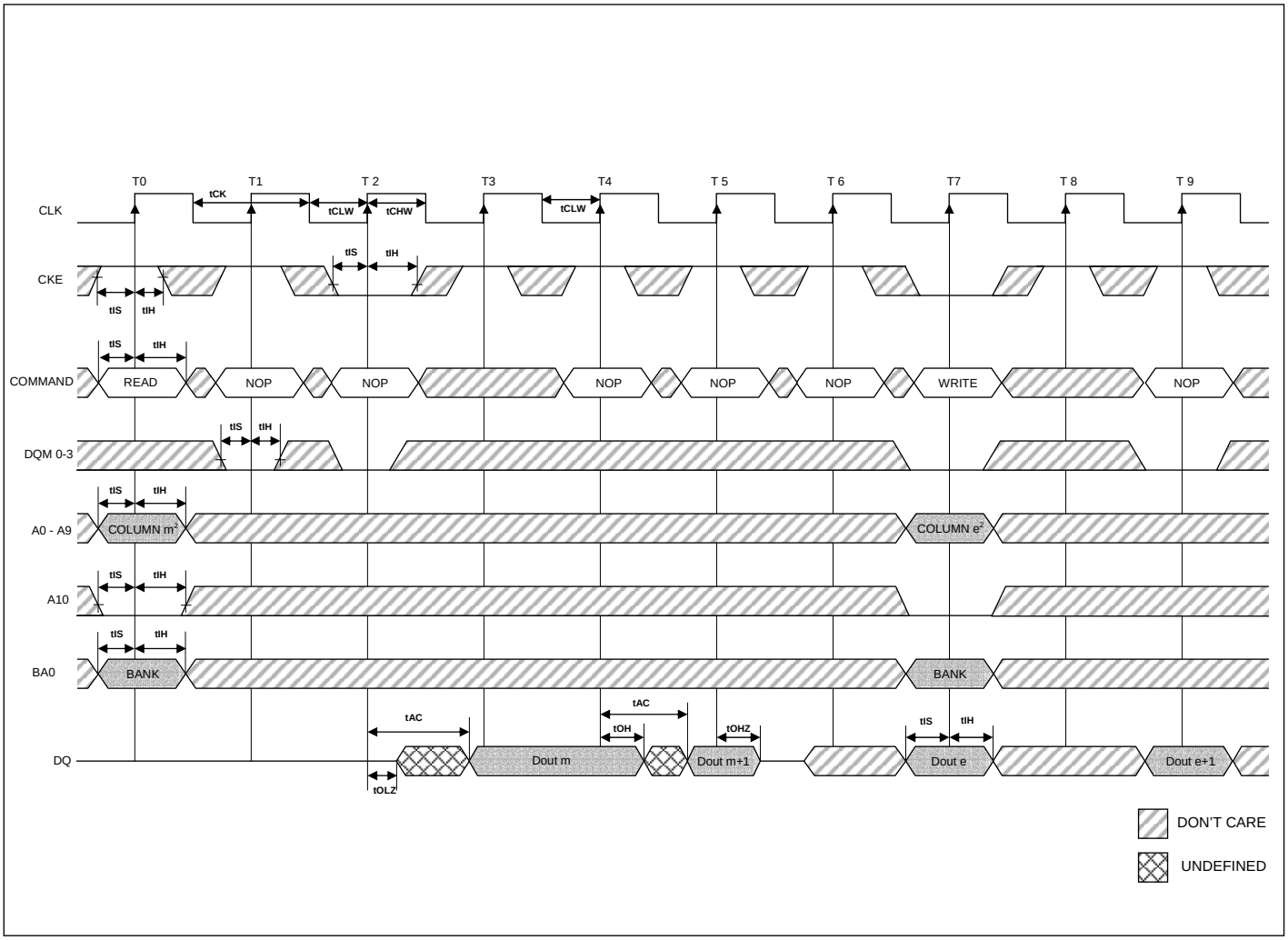


CLOCK SUSPEND MODE [1]

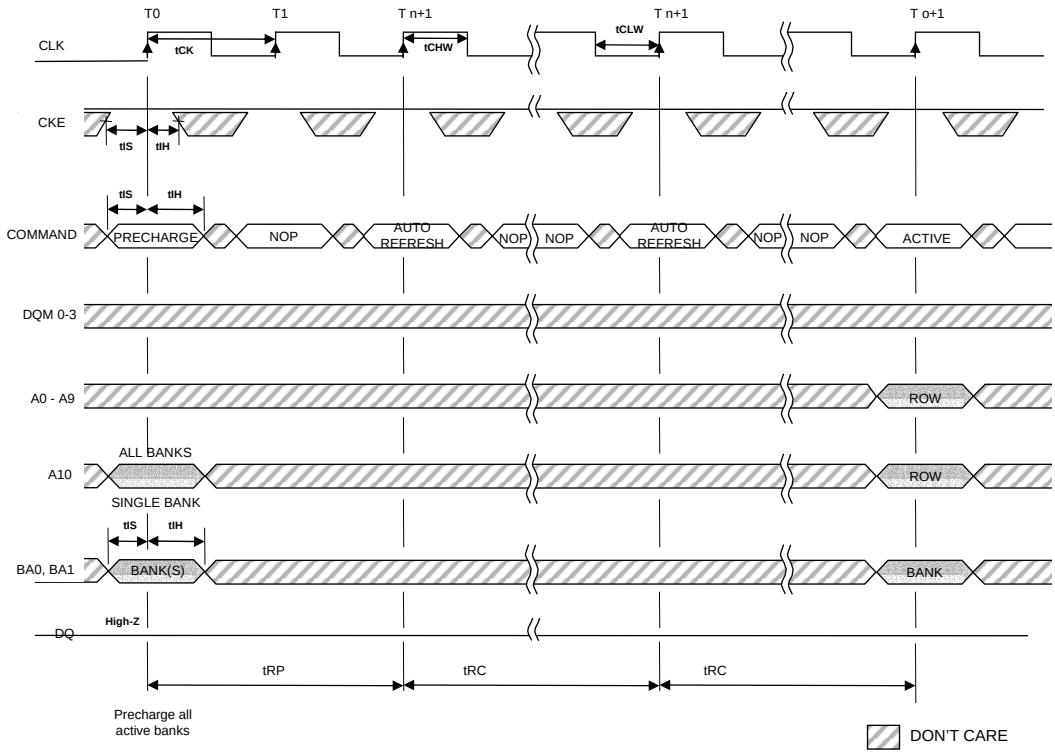
Notice :

[1] *For this example, the burst length = 2, the CAS latency = 3, and AUTO PRECHARGE is disabled.*

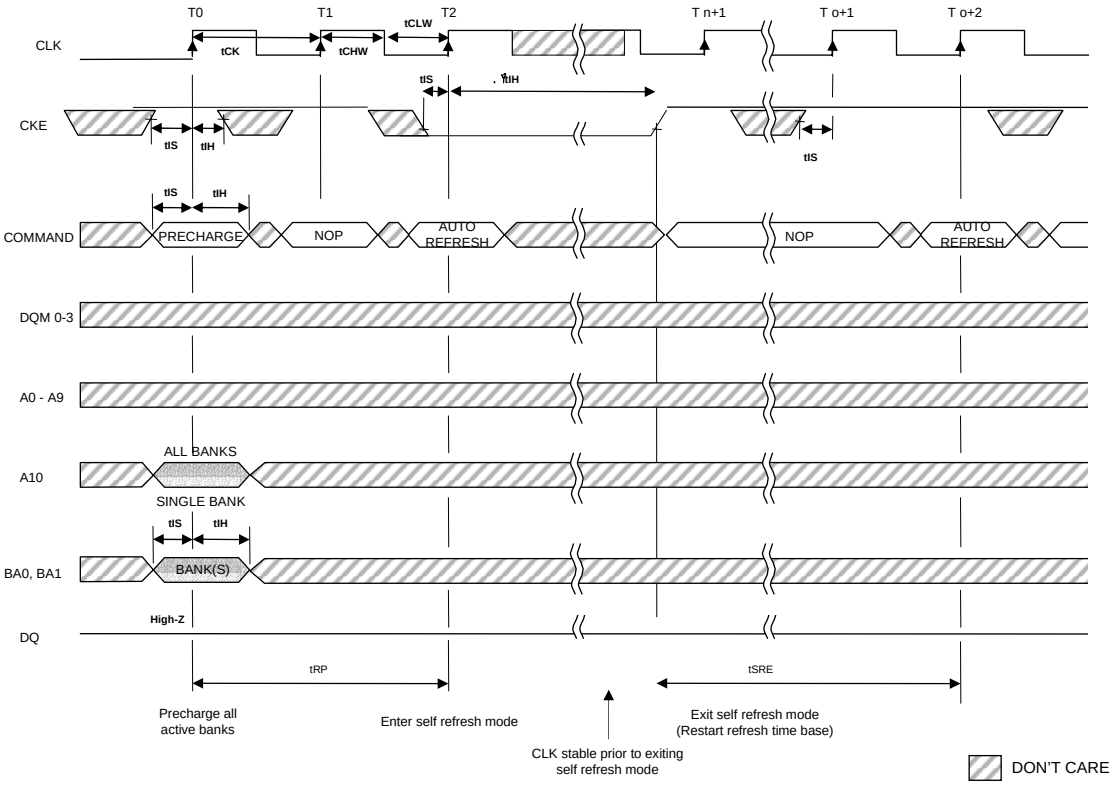
[2] *A8 and A9 = " Don't' Care."*



AUTO REFERSH MODE



SELF REFERSH MODE

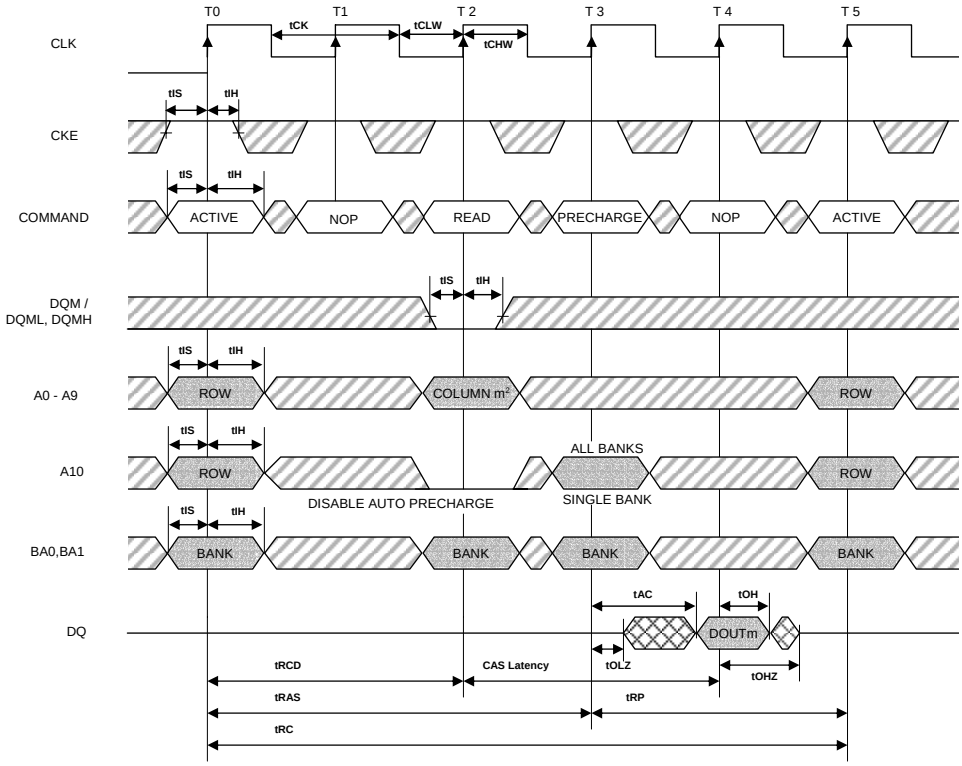


READ OPERATIONS

SIGNAL READ, WITHOUT AUTO PRECHARGE [1]

Notice :

[1] *For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by "manual" PRECHARGE.*
[2] *A8 and A9 = " Don't' Care."*



DON'T CARE

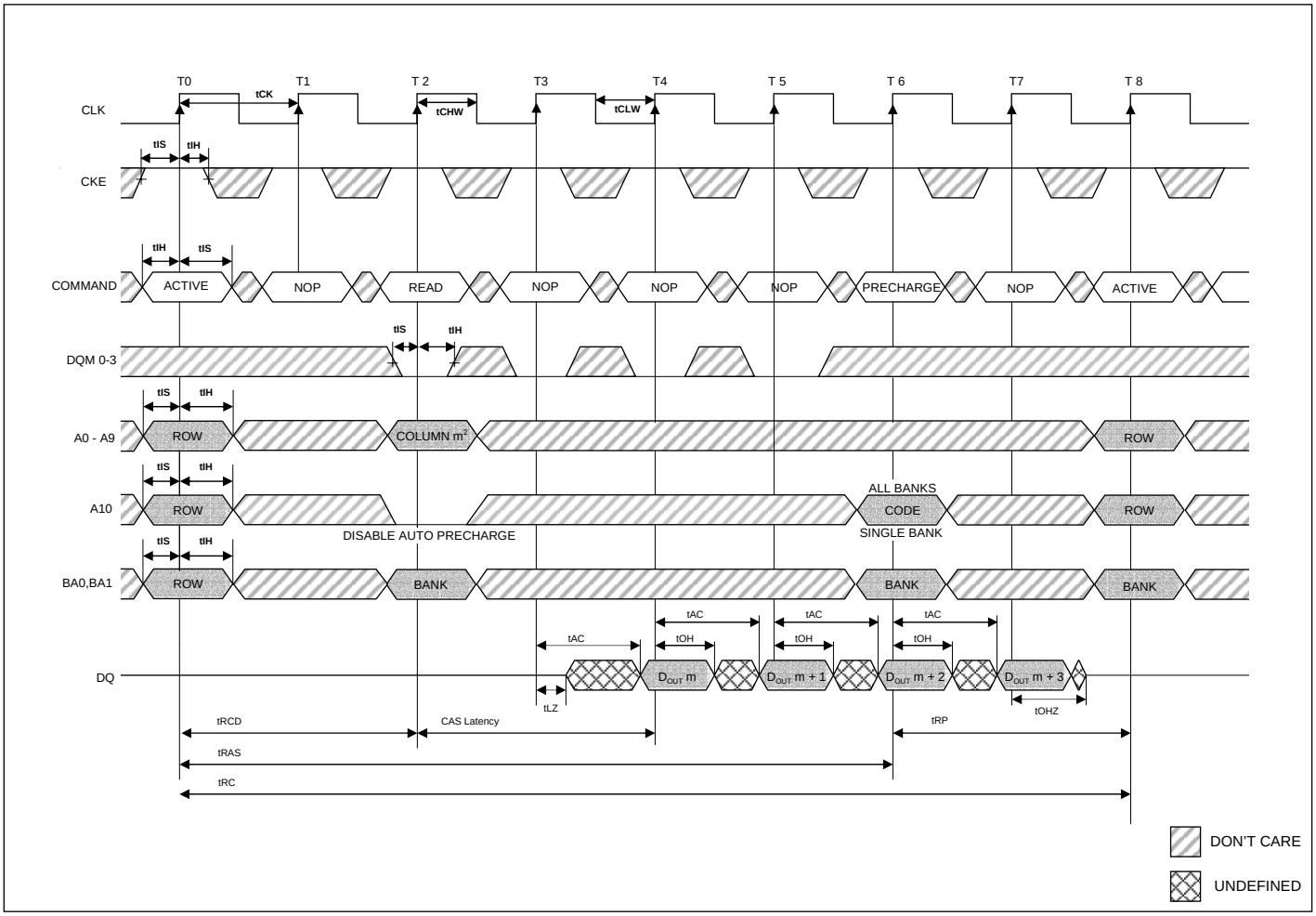
UNDEFINED

READ, WITHOUT AUTO PRECHARGE [1]

Notice :

[1] *For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by "manual" PRECHARGE.*

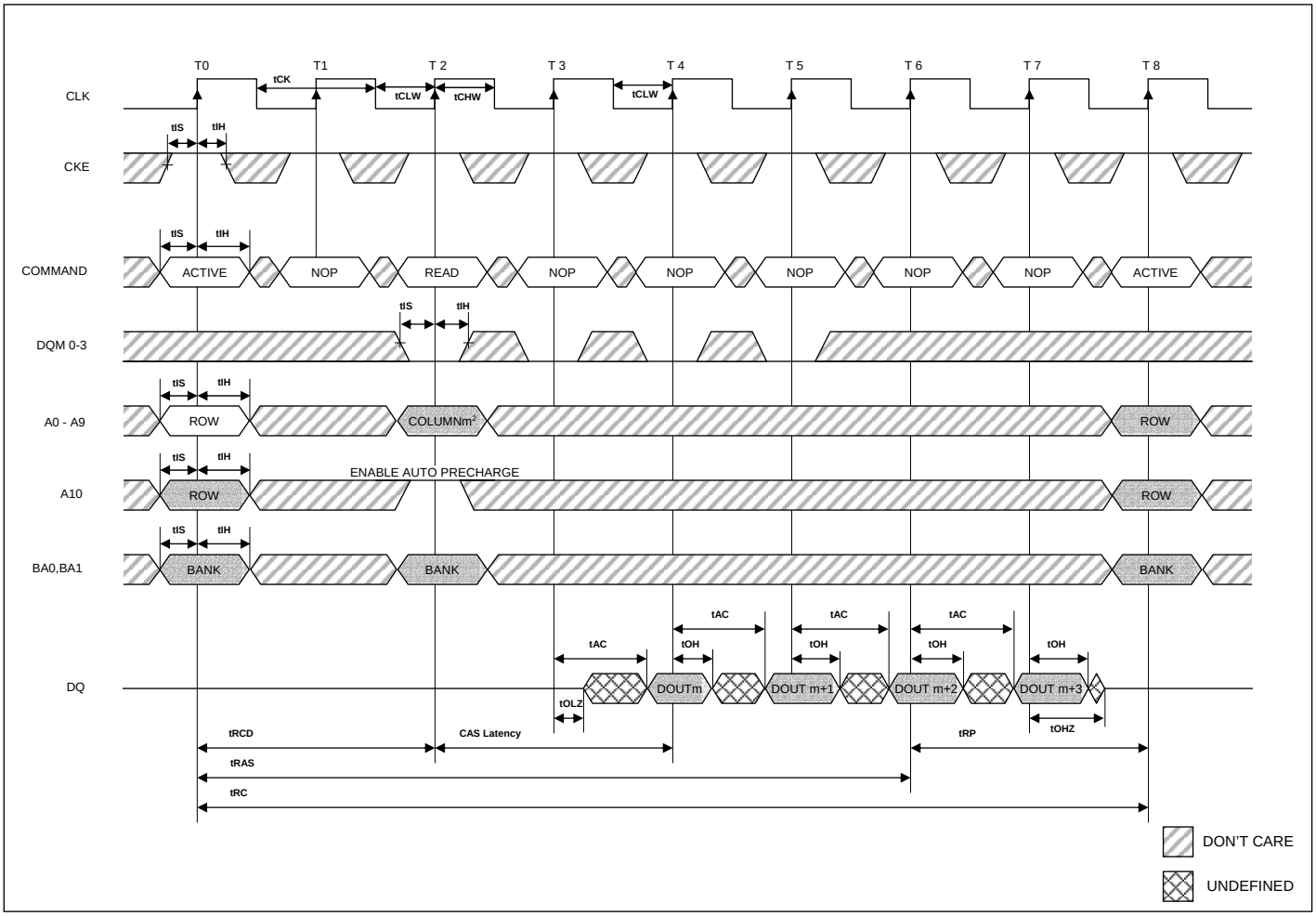
[2] *A8 and A9 = " Don't' Care."*



READ, WITH AUTO PRECHARGE [1]

Notice :

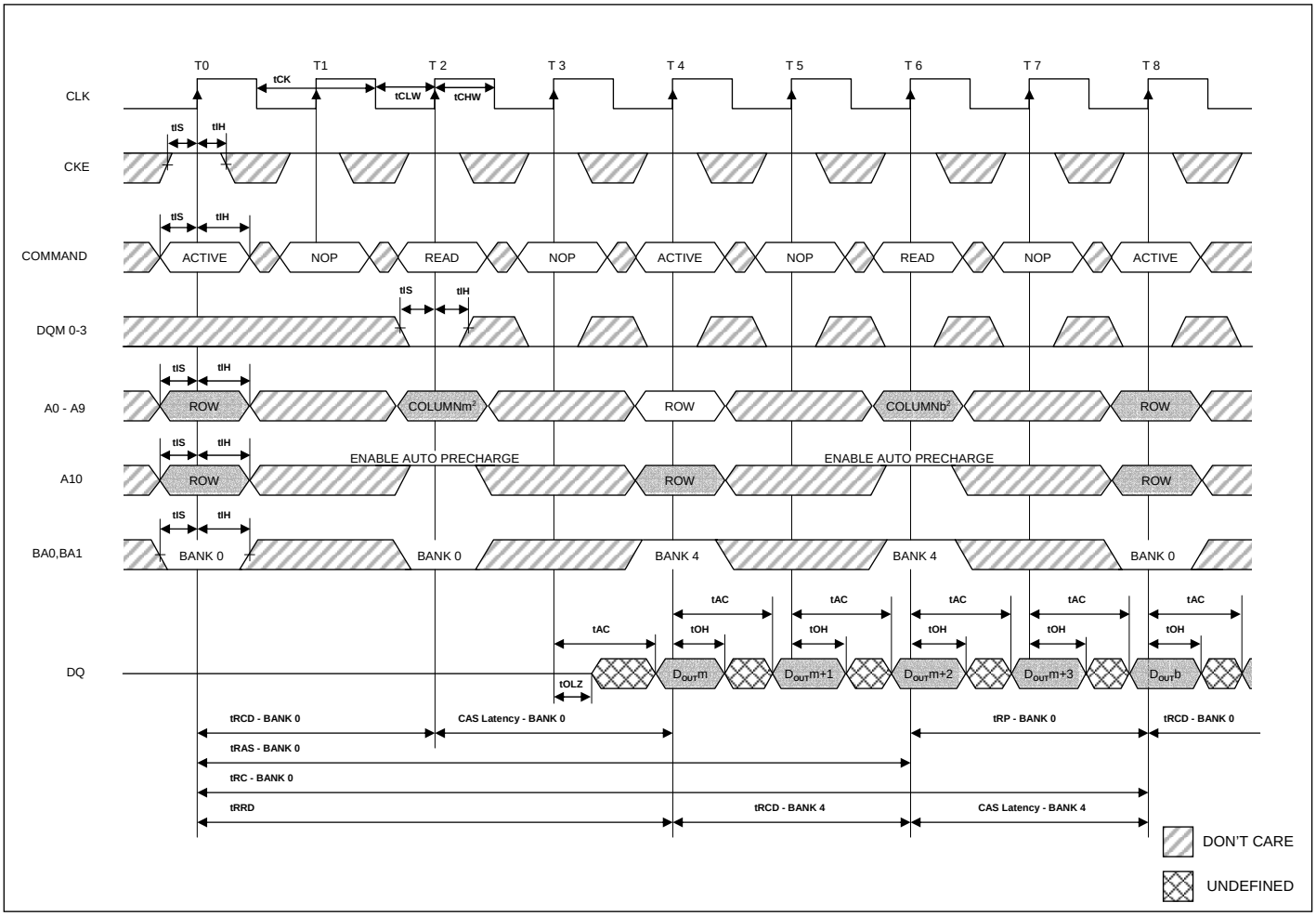
[1] *For this example, the burst length = 4, the CAS latency = 2.*
[2] *A8 and A9 = " Don't' Care."*



ALTERNATING BANK READ ACCESS [1]

Notice :

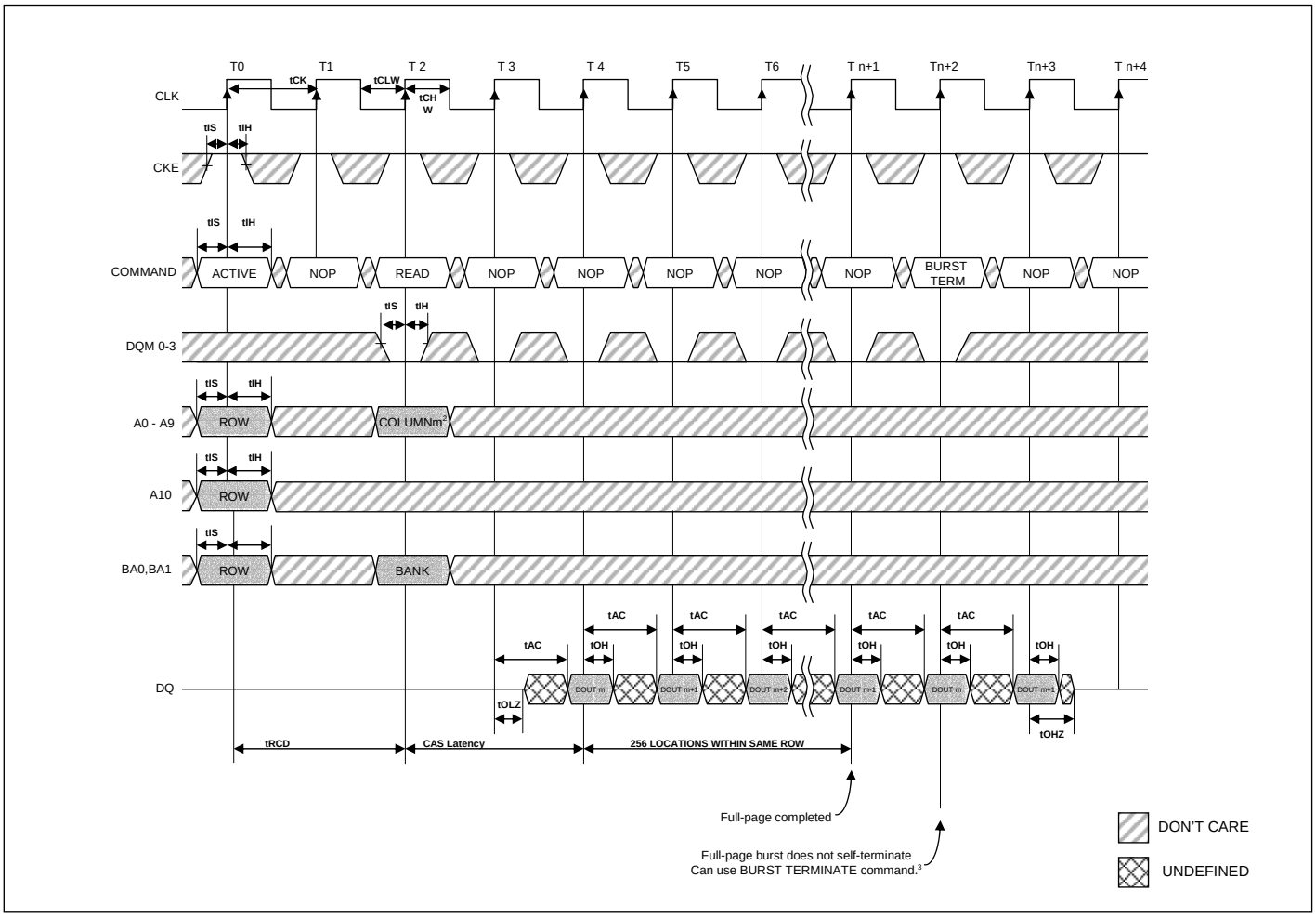
[1] *For this example, the burst length = 4, the CAS latency = 2.*
[2] *A8 and A9 = " Don't' Care."*



READ, FULL-PAGE BURST [1]

Notice :

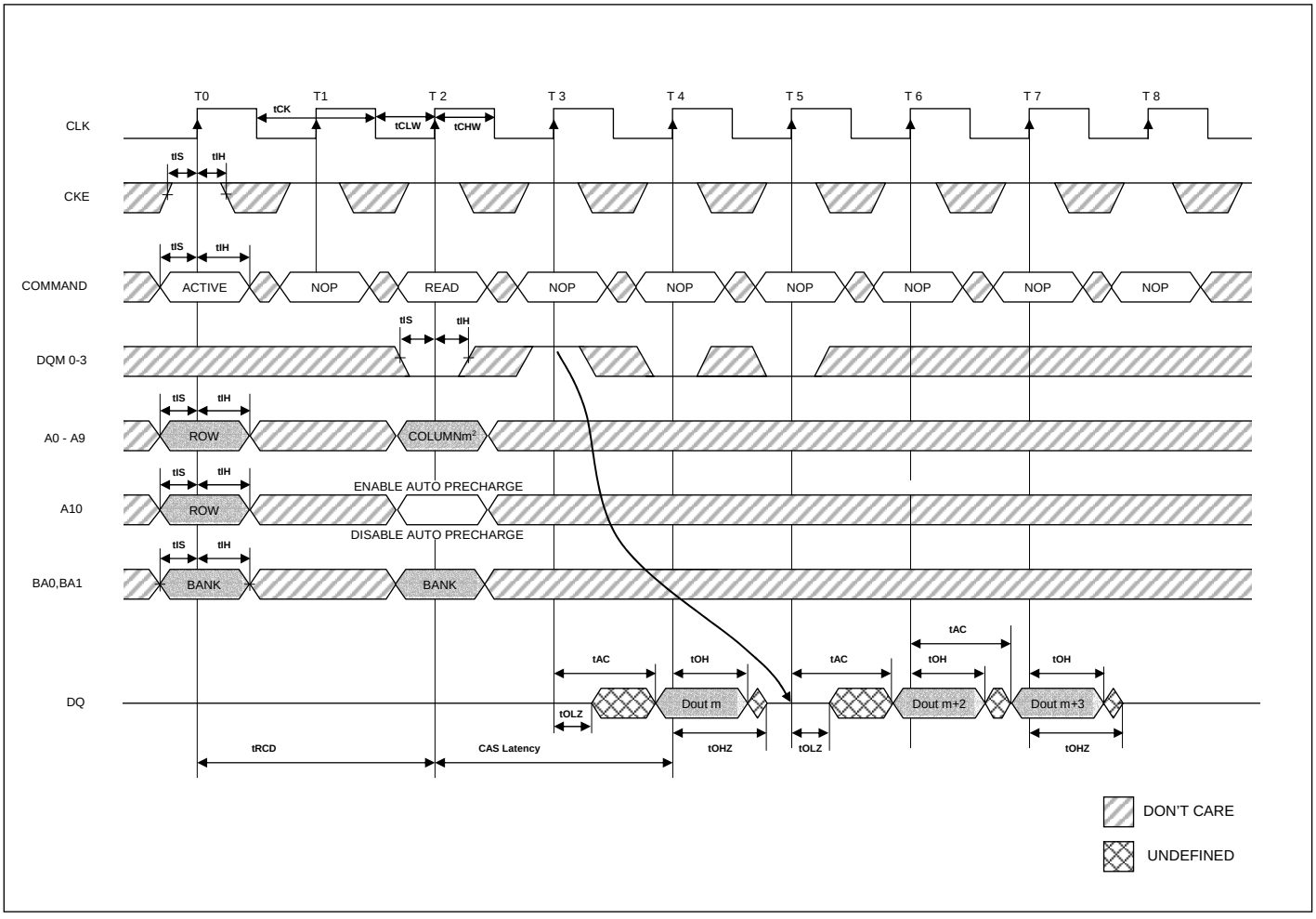
[1] *For this example CAS latency = 2.*
[2] *A8 and A9 = " Don't' Care."*
[3] *Page left open ; no tRP.*



READ, DQM OPERATION [1]

Notice :

[1] *For this example CAS latency = 2.*
[2] *A8 and A9 = " Don't' Care."*

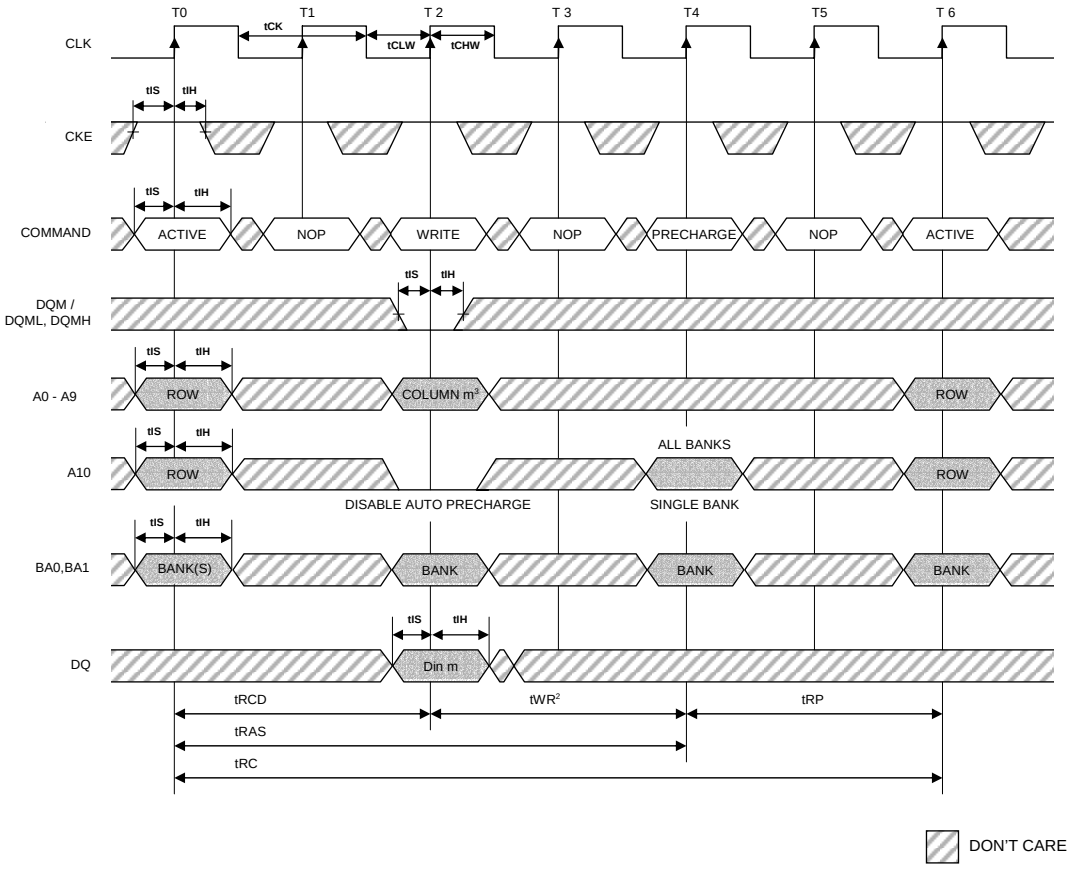


WRITE OPERATIONS

SINGLE WRITE, WITHOUT AUTO PRECHARGE [1]

Notice :

[1] *For this example, the burst length = 4, and the WRITE burst is followed by a "manual" PRECHARGE.*
[2] *10ns is required between <D_{IN} m> and the PRECHARGE command, regardless of frequenct, to meet tWR.*
[3] *A8 and A9 = "Don't Care."*



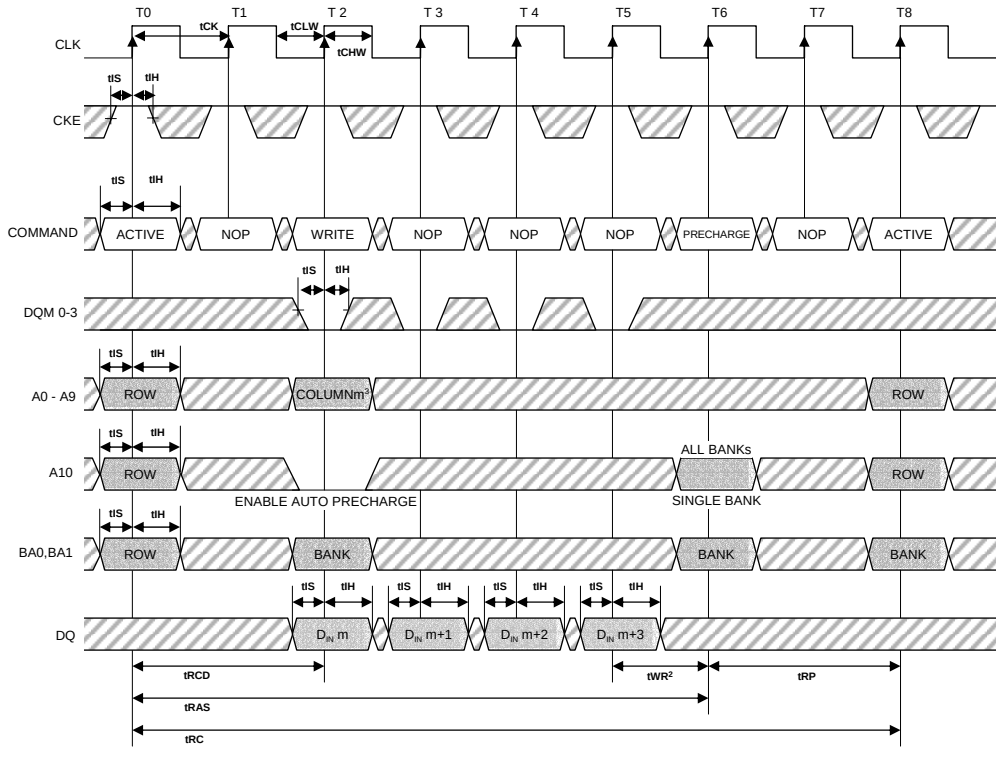
WRITE, WITHOUT AUTO PRECHARGE [1]

Notice :

[1] *For this example, the burst length = 4, and the WRITE burst is followed by a "manual" PRECHARGE.*

[2] *Faster frequencies require two clocks (when tWR > tCK).*

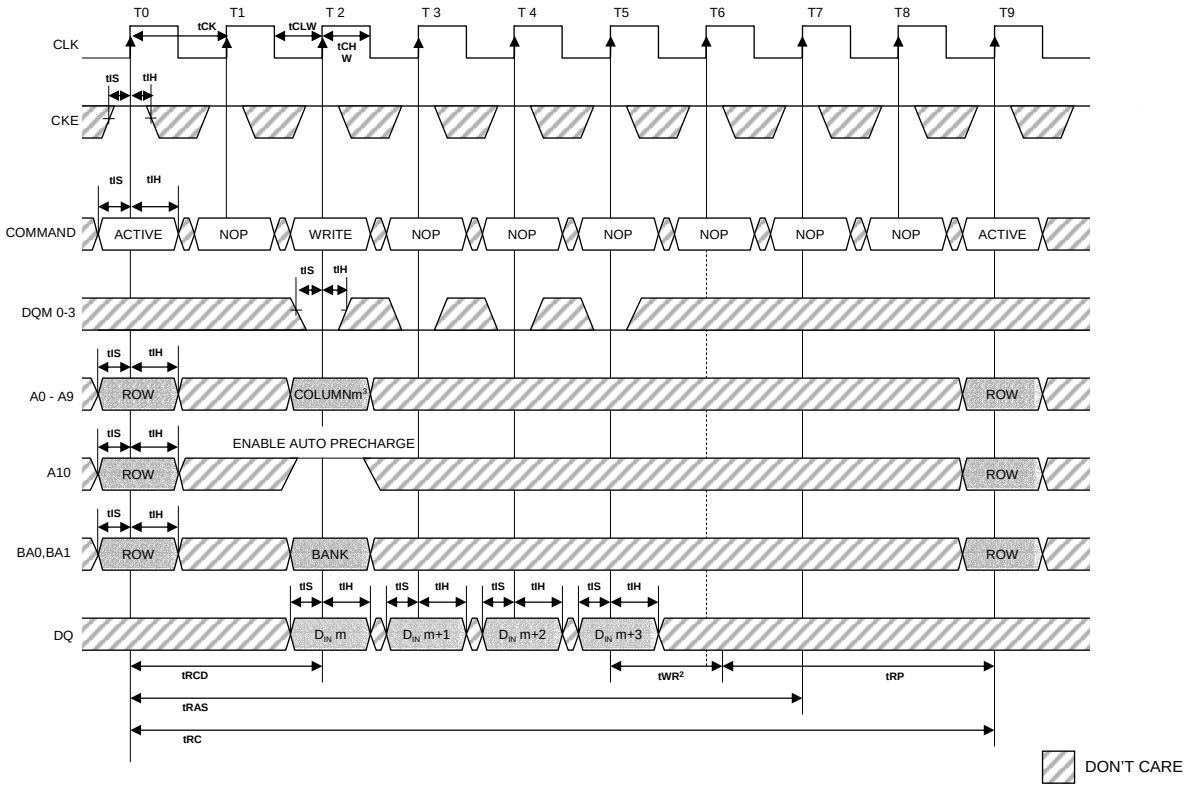
[3] *A8 and A9 = "Don't Care."*



WRITE, WITH AUTO PRECHARGE [1]

Notice :

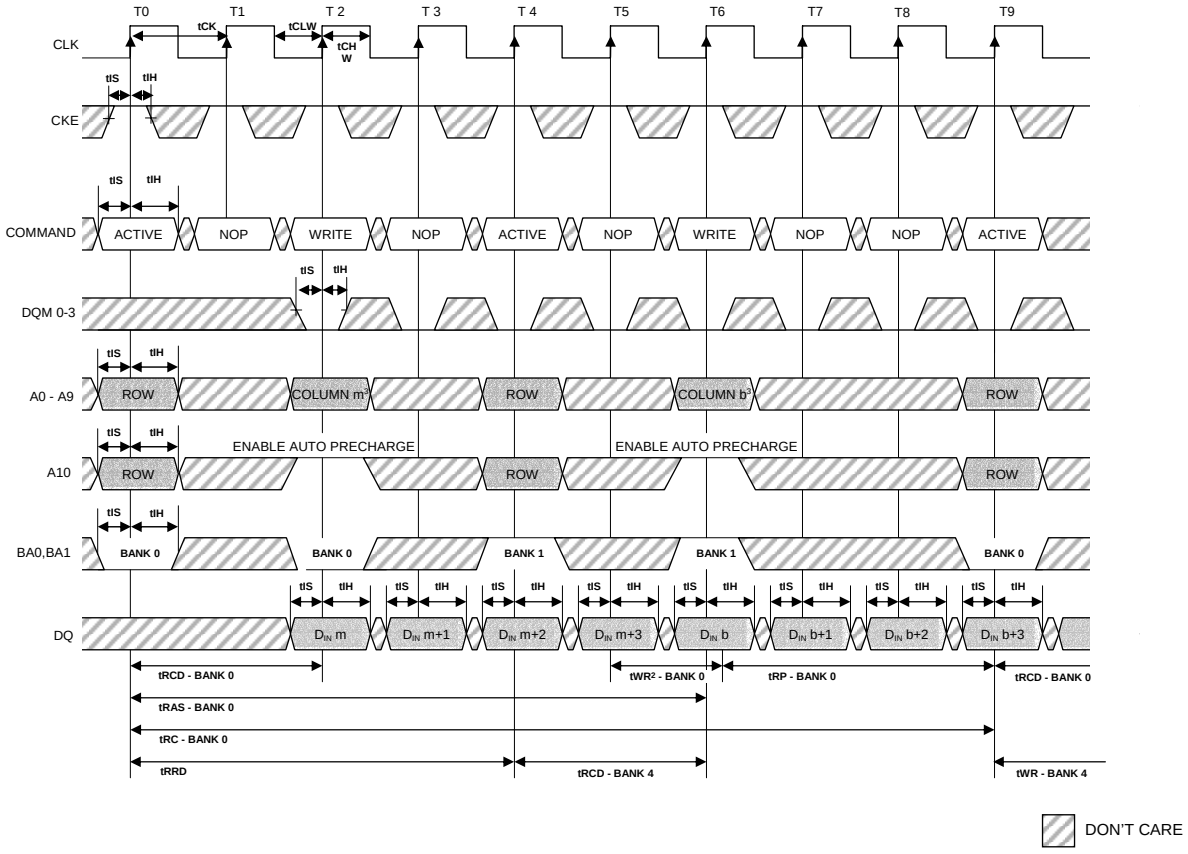
[1] *For this example, the burst length = 4.*
[2] *Faster frequencies require two clocks (when tWR > tCK).*
[3] *A8 and A9 = "Don't Care."*



ALTERNATING BANK WRITE ACCESS [1]

Notice :

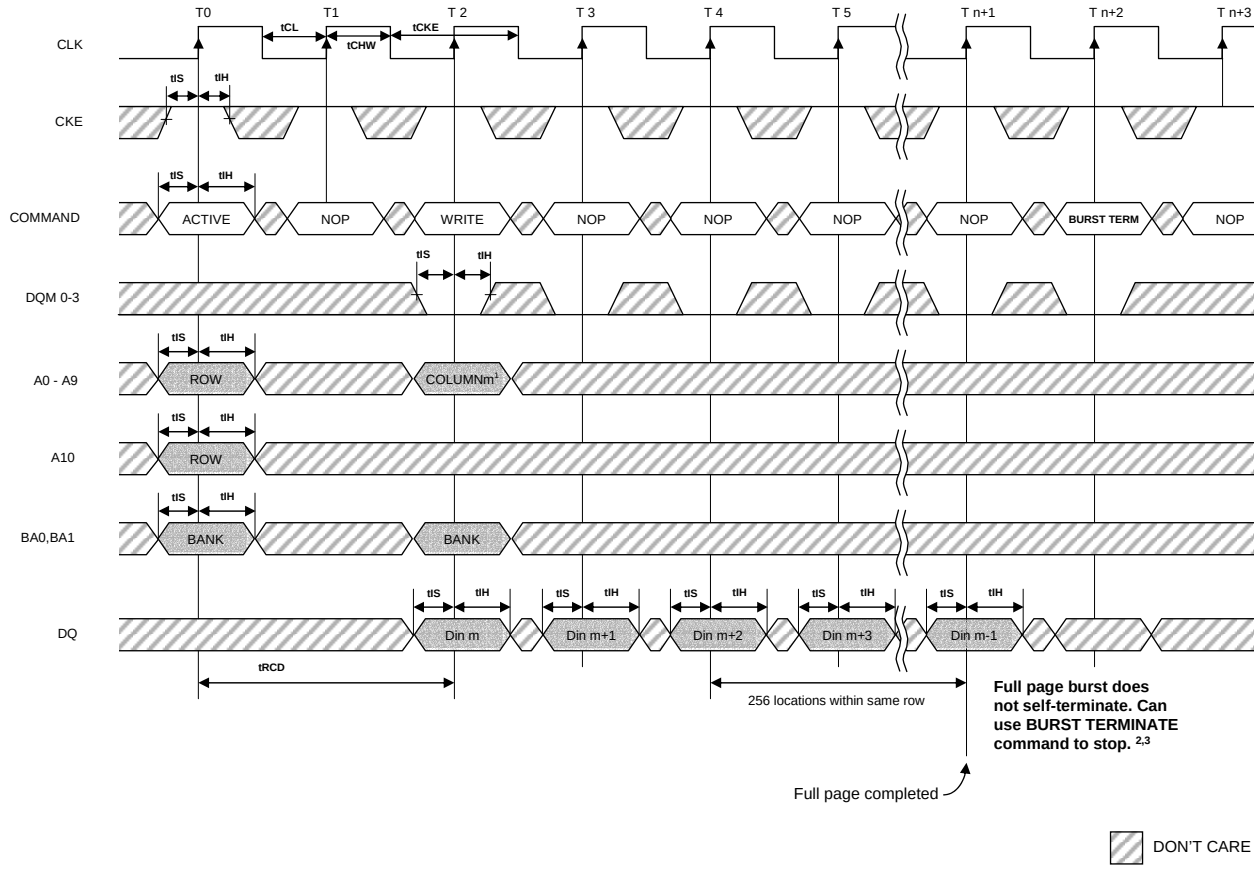
[1] *For this example, the burst length = 4.*
[2] *Faster frequencies require two clocks (when tWR > tCK).*
[3] *A8 and A9 = "Don't Care."*



WRITE, FULL-PAGE BURST [1]

Notice :

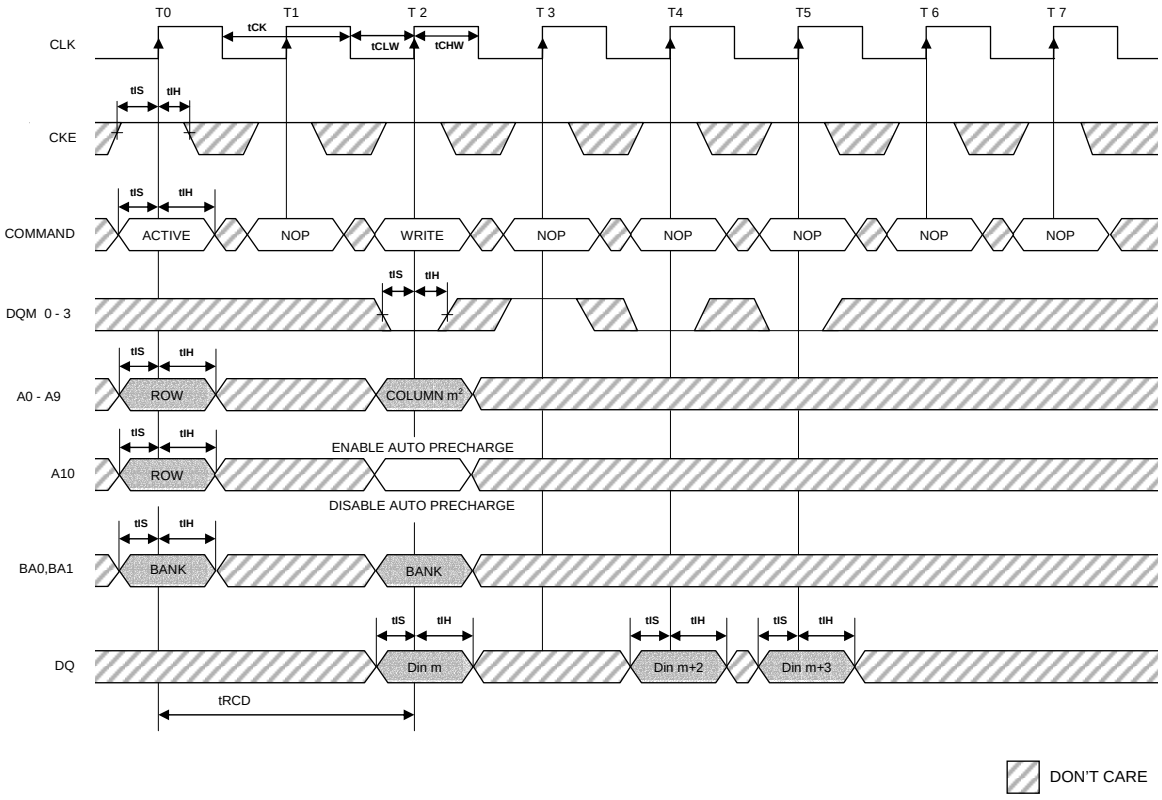
[1] *A8 and A9 = "Don't Care."*
[2] *tWR must be satisfied prior to PRECHARGE command.*
[3] *Page left open ; no tRP.*



WRITE, DQM OPERATION [1]

Notice :

[1] *For this example, the burst length = 4.*
[2] *A8 and A9 = "Don't Care."*



GLT 5 640 L 32 - 10 TC

4 : DRAM
5 : Synchronous DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM
9 : SGRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M

-DRAM
10 : 1M(C/EDO)
11 : 1M(C/FPM)
12 : 1M(H/EDO)
13 : 1M(H/FPM)
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
160 : 16M(EDO)
161 : 16M(FPM)
640 : 64M(EDO)
641 : 64M(FPM)

-SDRAM
40 : 4M
160 : 16M
640 : 64M

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.1V

POWER
Blank : Standard
L : Low Power
LL : Low Low Power
SL : Super Low Power

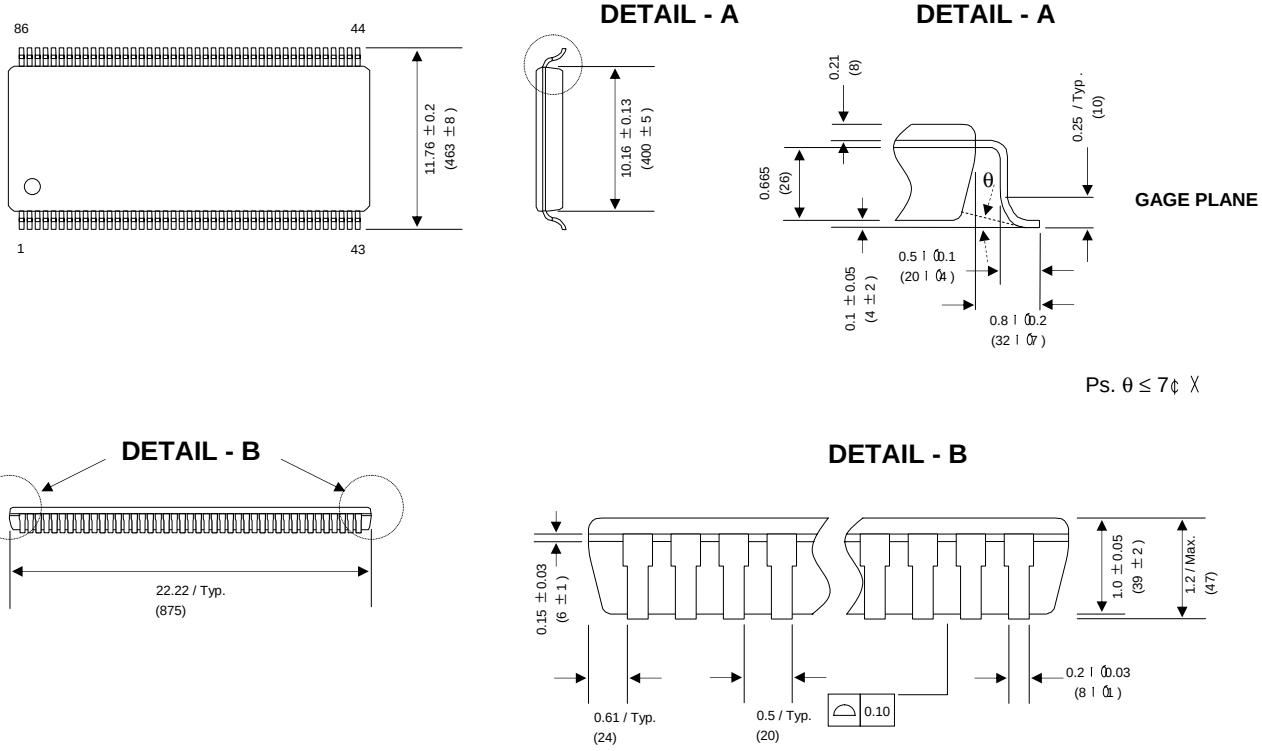
SPEED
-SRAM
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns
SDRAM :
5 : 5ns/200 MHZ
5.5 : 5.5ns/182 MHZ
6 : 6ns/166 MHZ
7 : 7ns/143 MHZ
10 : 10ns/100 MHZ

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP
FG : 48Pin BGA 9x12
FH : 48Pin BGA 8x10
FI : 48Pin BGA 6x8

Temperature Range
E : Extended Temperature
I : Industrial Temperature
Blank : Commercial Temperature

PACKAGE DIMENSIONS

86 PIN TSOP-II 400mil PLASTIC



Notice : *Dimension UNIT, Milimeter(mil).*

G-Link Technology Corp.