

January 2001

## CMOS HIGH VOLTAGE DISPLAY DRIVER

### GENERAL DESCRIPTION

The HI-8020 & HI-8120 high voltage display drivers are functional replacements for the AMI S5420 and Micrel MIC8013/8014 series. These CMOS products are designed to drive liquid crystal displays by converting 5 volt serial data to parallel segment and backplane waveforms with amplitudes up to 30 volts. The HI-8020 & HI-8120 differ from the HI-8010 by only the shift register clock and chip select gating logic. The HI-8020 has TTL logic inputs whereas the HI-8120 has CMOS logic inputs.

Both devices can drive up to 38 segments and have 3 possible shift register data taps to provide options to cascade devices for larger displays. Data is clocked into a 38 stage shift register and parallel latched before the output translators by a Load input.

The HI-8020 & HI-8120 are available in a variety of ceramic and plastic packaging including DIP; leaded and leadless chip carriers; and J-lead and gull-wing quad flat packs.

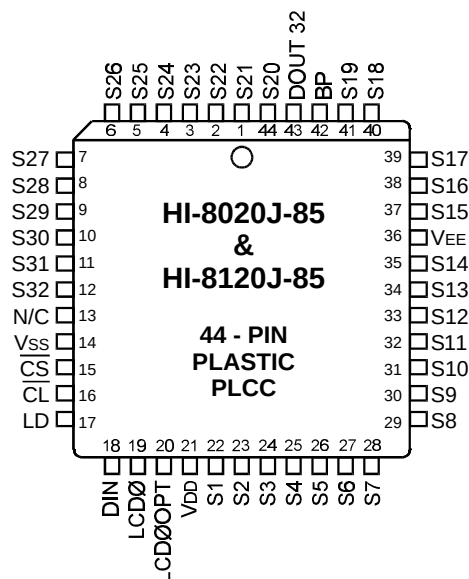
### FEATURES

- 5 volt input translated to 30 volts or less
- Pin-out adaptable to drive 30, 32 or 38 LCD segments
- RC oscillator or high voltage (BP) clock input
- TTL compatible inputs (HI-8020 only)
- CMOS compatible inputs (HI-8120 only)
- Low power consumption
- Industrial (-40°C to +85°C) & Military (-55°C to +125°C) temperature ranges
- Pin for pin compatible with the Micrel MIC8010/8011 series and the AMI S4520 series drivers
- Cascadable
- Military level processing available

### APPLICATIONS

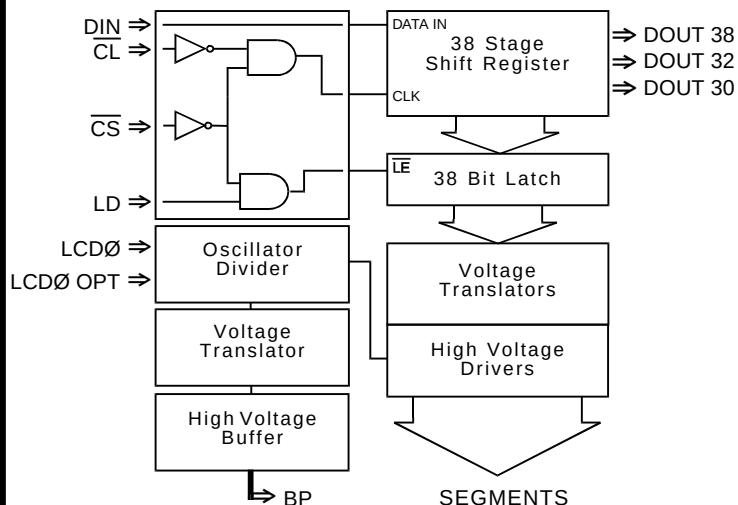
- Dichroic Liquid Crystal Displays
- Standard Liquid Crystal Displays
- Vacuum Fluorescent Displays

### PIN CONFIGURATION (Top View)



(See page 3-6 for additional package pin configurations)

### FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

Whenever a Logic "0" is applied to the Chip Select ( $\overline{CS}$ ) input, one bit of data is clocked into the shift register from the serial data input (DIN) with each negative transition of the Clock ( $\overline{CL}$ ) input.  $\overline{CS}$  is internally tied to VSS on some versions. A Logic "1" present at the Load (LD) input will cause a parallel transfer of data from the shift register to the data latch. If the Load (LD) input is held high while data is clocked into the shift register, the latch will be transparent. All four logic inputs are TTL compatible on the HI-8020 and CMOS compatible on the HI-8120.

To display segments, a Logic "1" is stored in the appropriate shift register bit position, and the segment output is out-of-phase with the backplane.

The backplane output functions in 1 of 2 modes; externally driven or self-oscillating. When the LCD $\emptyset$  input is externally driven with the LCD $\emptyset$ OPT input open circuit (Figure 2), the backplane output will be in-phase with LCD $\emptyset$ . Utilizing the self-oscillating mode, inputs LCD $\emptyset$  and LCD $\emptyset$ OPT are tied together and connected to an RC circuit (Figure 3). A 150K $\Omega$  resistor with a 470pF capacitor generates an approximate backplane frequency of 100Hz. The LCD $\emptyset$ /LCD $\emptyset$ OPT oscillator frequency is divided by 256 to determine the backplane output frequency. The resistor value (R) must be at least 30K $\Omega$  for proper self-oscillator operation.

For displays having a number of segments greater than 38, two or more of the display drivers may be cascaded together by connecting the serial data output (DOUT) from the first driver, to the serial data input (DIN) of the following driver, etc. (See Figures 2 & 3). Data out (DOUT) will change state

on the rising edge of the Clock ( $\overline{CL}$ ). Clock ( $\overline{CL}$ ), Load (LD) and Chip Select ( $\overline{CS}$ ) should be tied in common with each other, respectively, between all cascaded display drivers.

## INTERNAL OSCILLATOR CIRCUIT

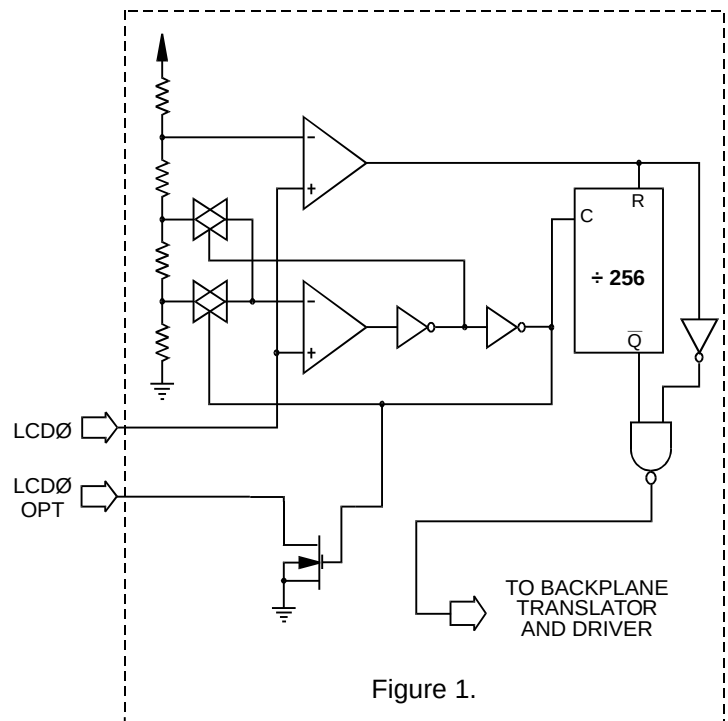
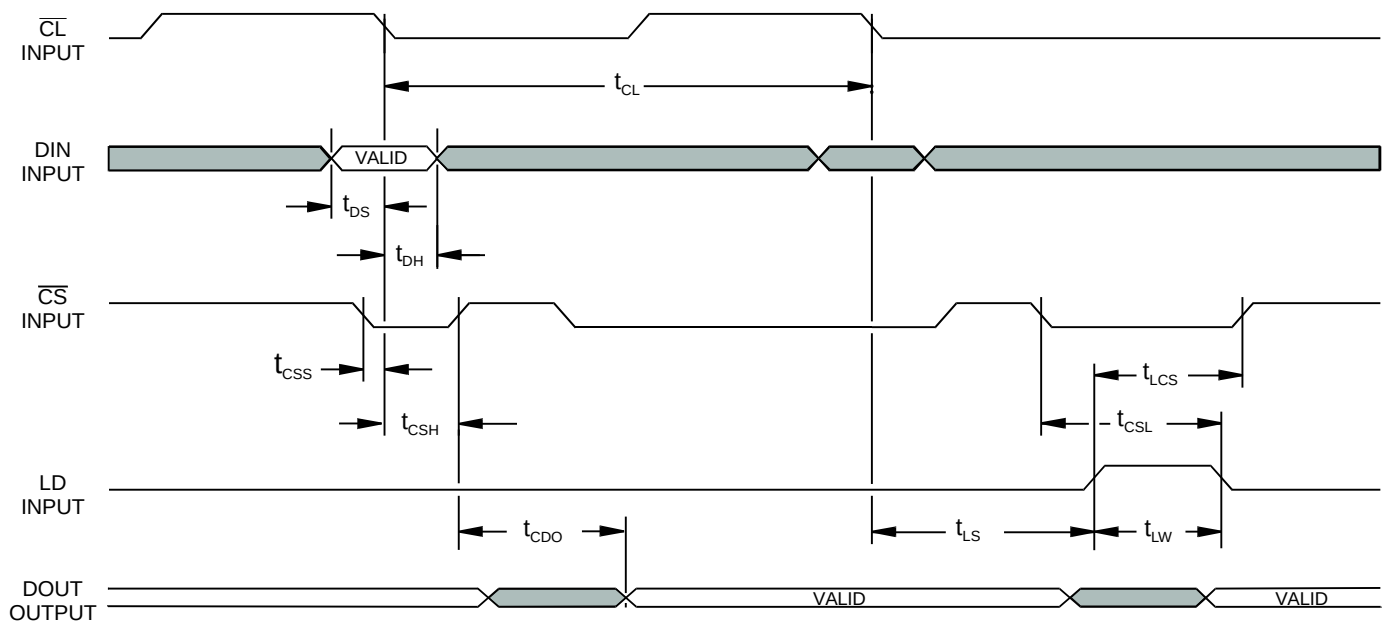


Figure 1.

## TIMING DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Voltages referenced to VSS = 0V

|                                   |                                            |                                                            |
|-----------------------------------|--------------------------------------------|------------------------------------------------------------|
| Supply Voltage                    | VDD..... 0V to 7V<br>VEE.....VDD-35V to 0V | Power Dissipation.....300 mW                               |
| Voltage at any input, except LCDØ | ..-0.3 to VDD+0.3V                         | Operating Temperature Range - Industrial.....-40° to +85°C |
| Voltage at LCDØ input.....        | VDD-35 to VDD+0.3V                         | Operating Temperature Range - Hi-Temp/Mil...-55° to +125°C |
| DC Current any input pin.....     | 10 mA                                      | Storage Temperature Range.....-65° to +150°C               |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

VDD = 5V, VEE = -25V, VSS = 0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER                                 | SYMBOL  | CONDITION                  | MIN     | TYP | MAX     | UNITS |
|-------------------------------------------|---------|----------------------------|---------|-----|---------|-------|
| Operating Voltage                         | VDD     |                            | 3.0     |     | 7.0     | V     |
| Supply Current                            | IDD     | Static, No Load            |         |     | 200     | µA    |
|                                           | IEE     | Static, No Load fBP=100Hz  |         |     | 150     | µA    |
| Input Low Voltage, HI-8020 (except LCDØ)  | VILTTL  |                            | 0       |     | 0.8     | V     |
| Input High Voltage, HI-8020 (except LCDØ) | VIHTTL  |                            | 2       |     | VDD     | V     |
| Input Low Voltage, HI-8120 (except LCDØ)  | VILCMOS |                            | 0       |     | 0.3 VDD | V     |
| Input High Voltage, HI-8120 (except LCDØ) | VIHCMOS |                            | 0.7 VDD |     | VDD     | V     |
| Input Low Voltage (LCDØ)                  | VILX    |                            | VEE     |     | 3       | V     |
| Input High Voltage (LCDØ)                 | VIHX    |                            | 3.5     |     | VDD     | V     |
| Input Current                             | IIN     | VIN = 0 to 5V              |         |     | 1       | µA    |
| Input Capacitance (not tested)            | CI      |                            |         |     | 5       | pF    |
| Segment Output Impedance                  | RSEG    | IL = 10µA                  |         |     | 10,000  | Ω     |
| Backplane Output Impedance                | RBP     | IL = 10µA                  |         |     | 450     | Ω     |
| Data Out Current:                         | IDOH    | Source Current, VOH = 4.5V |         |     | -0.6    | mA    |
|                                           | IDOL    | Sink Current, VOL = 0.5V   | 0.6     |     |         | mA    |

## AC ELECTRICAL CHARACTERISTICS

VDD = 5V, VEE = -25V, VSS = 0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER                    | SYMBOL | VDD | MIN  | TYP | MAX | UNITS |
|------------------------------|--------|-----|------|-----|-----|-------|
| Clock Period                 | tCL    | 5V  | 1200 |     |     | ns    |
| Clock Pulse Width            | tcw    | 5V  | 520  |     |     | ns    |
| Data In - Setup              | tDS    | 5V  | 50   |     |     | ns    |
| Data In - Hold               | tDH    | 5V  | 400  |     |     | ns    |
| Chip Select - Setup to Clock | tcSS   | 5V  | 200  |     |     | ns    |
| Chip Select - Hold to Clock  | tCSH   | 5V  | 450  |     |     | ns    |
| Load - Setup to Clock        | tLS    | 5V  | 500  |     |     | ns    |
| Chip Select - Setup to Load  | tCSL   | 5V  | 300  |     |     | ns    |
| Load Pulse Width             | tLW    | 5V  | 500  |     |     | ns    |
| Chip Select - Hold to Load   | tLCS   | 5V  | 300  |     |     | ns    |
| Data Out Valid, from Clock   | tcDO   | 5V  |      |     | 800 | ns    |

## CASCADING - EXT. OSCILLATOR

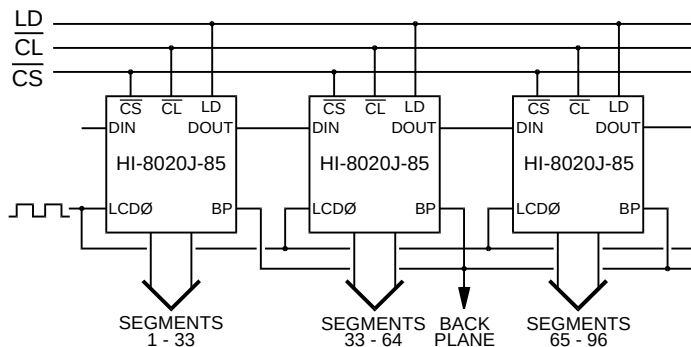


Figure 2

## CASCADING - RC OSCILLATOR

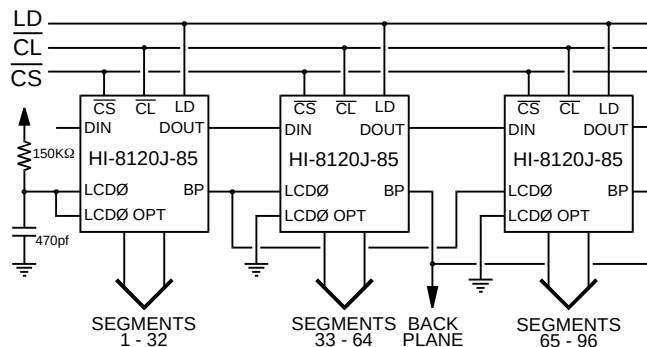


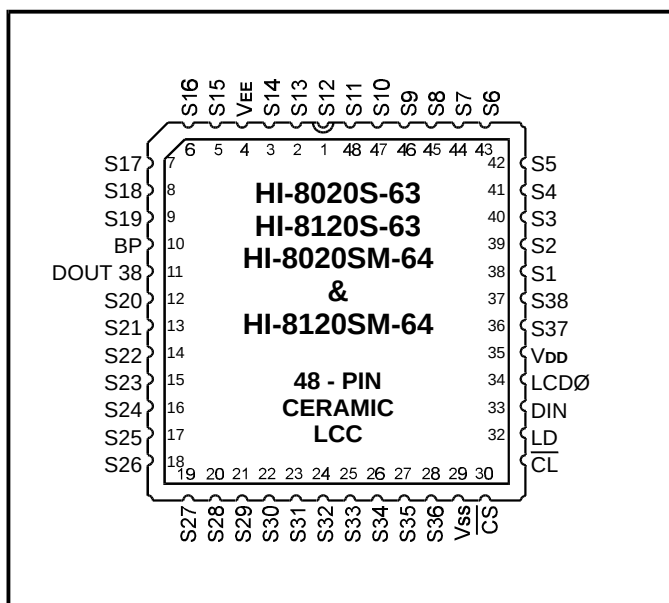
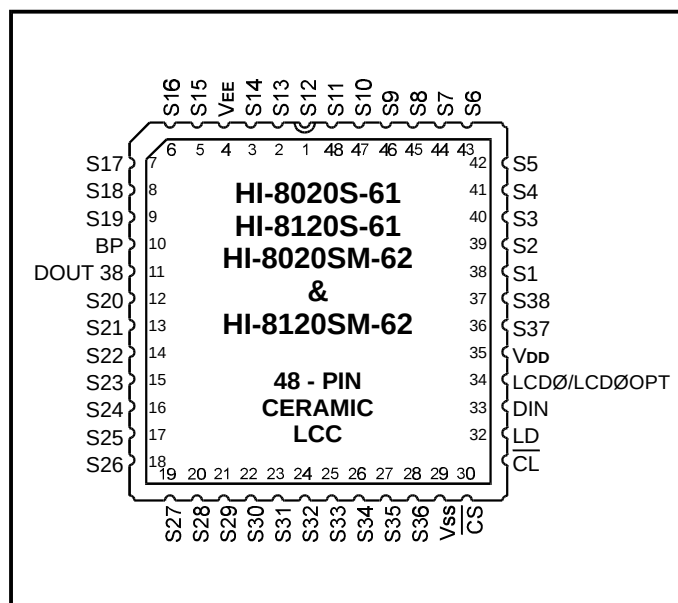
Figure 3

## PIN DESCRIPTIONS

| VSS                    | POWER  | 0 Volts              |                                                                                |
|------------------------|--------|----------------------|--------------------------------------------------------------------------------|
| $\overline{\text{CS}}$ | INPUT  | Logic input          | Chip select                                                                    |
| $\overline{\text{CL}}$ | INPUT  | Logic input          | Clocks shift register on negative edge and DOUT pins on positive edge          |
| LD                     | INPUT  | Logic input          | Segment outputs equal shift register data if Load is high                      |
| DIN                    | INPUT  | Logic input          | Shift register data input                                                      |
| LCD0                   | INPUT  | Analog input         | Display clock input and is always bonded out. Can swing from VEE to VDD        |
| LCD0OPT                | OUTPUT | Analog output        | Bonded out only if an RC oscillator is required                                |
| VDD                    | POWER  | 5 Volts              |                                                                                |
| VEE                    | POWER  | 0 Volts to -30 Volts |                                                                                |
| DOUT                   | OUTPUT | Logic output         | Selected pinout can provide shift register taps at positions 30, 32, 34, or 38 |
| BP                     | OUTPUT | Display drive output | Low resistance drive for the backplane and swings from VDD to VEE              |
| Segments               | OUTPUT | Display drive output | High resistance drive for each segment and swings from VDD to VEE              |

## ADDITIONAL HI-8020/HI-8120 PIN CONFIGURATIONS

(See page 3-9 for 44-Pin Plastic PLCC)



## ORDERING INFORMATION

| PART NUMBER             | NUMBER OF SEGMENTS | MASTER /SLAVE | PACKAGE DESCRIPTION                  | TEMPERATURE RANGE | FLOW | BURN IN | LEAD FINISH |
|-------------------------|--------------------|---------------|--------------------------------------|-------------------|------|---------|-------------|
| <b>TTL Input Logic</b>  |                    |               |                                      |                   |      |         |             |
| HI-8020J-85             | 32                 | BOTH          | 44 PIN PLASTIC J LEAD                | -40°C TO +85°C    | I    | NO      | SOLDER      |
| HI-8020S-61             | 38                 | MASTER        | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -40°C TO +85°C    | I    | NO      | GOLD        |
| HI-8020SM-62            | 38                 | MASTER        | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -55°C TO +125°C   | M    | YES     | SOLDER      |
| HI-8020S-63             | 38                 | SLAVE         | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -40°C TO +85°C    | I    | NO      | GOLD        |
| HI-8020SM-64            | 38                 | SLAVE         | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -55°C TO +125°C   | M    | YES     | SOLDER      |
| <b>CMOS Input Logic</b> |                    |               |                                      |                   |      |         |             |
| HI-8120J-85             | 32                 | BOTH          | 44 PIN PLASTIC J LEAD                | -40°C TO +85°C    | I    | NO      | SOLDER      |
| HI-8120S-61             | 38                 | MASTER        | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -40°C TO +85°C    | I    | NO      | GOLD        |
| HI-8120SM-62            | 38                 | MASTER        | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -55°C TO +125°C   | M    | YES     | SOLDER      |
| HI-8120S-63             | 38                 | SLAVE         | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -40°C TO +85°C    | I    | NO      | GOLD        |
| HI-8120SM-64            | 38                 | SLAVE         | 48 PIN CERAMIC LEADLESS CHIP CARRIER | -55°C TO +125°C   | M    | YES     | SOLDER      |

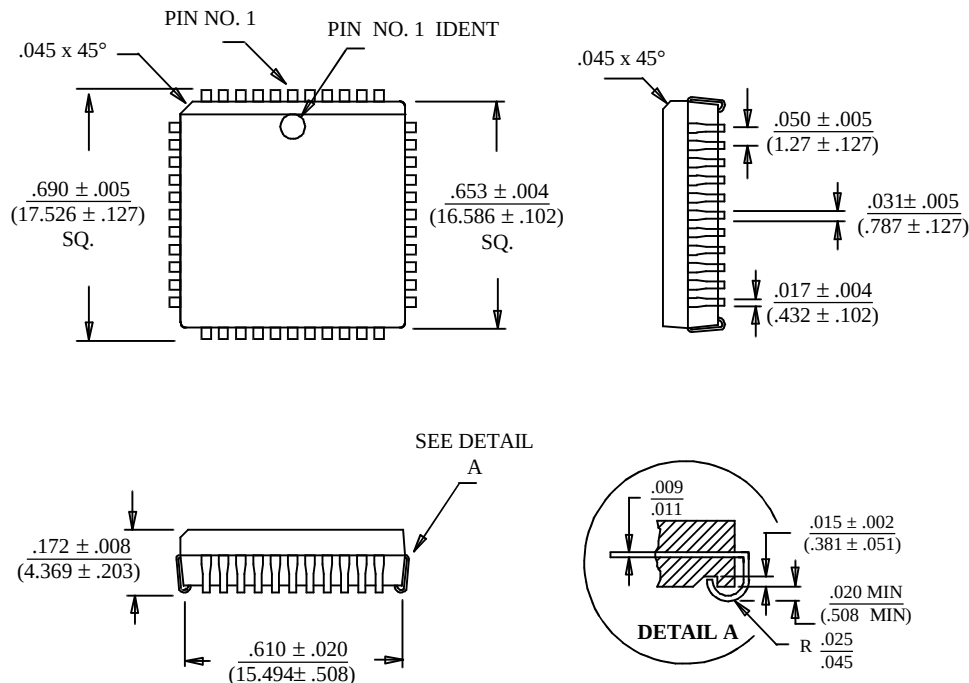
## SEMI-CUSTOM PACKAGING

The above part numbers represent some of the typical configurations of the HI-8020 & HI-8120 products. They can also be provided with a varied number of output segments (30, 32 and 38), with either industrial or military screening and in a wide variety of packages. Listed below are currently available packages. Please contact the Holt Sales Department for your specific requirements.

| PACKAGE DESCRIPTION                 | NO. LEADS |
|-------------------------------------|-----------|
| PLASTIC DUAL-IN-LINE (PDIP)         | 40        |
|                                     | 48        |
| PLASTIC QUAD FLAT PACK (PQFP)       | 52        |
| PLASTIC J-LEAD CHIP CARRIER (PLCC)  | 44        |
| CERAMIC DUAL-IN-LINE (CDIP)         | 40        |
|                                     | 48        |
| CERAMIC LEADLESS CHIP CARRIER (LCC) | 40        |
|                                     | 48        |
| CERAMIC J-LEAD CHIP CARRIER         | 44        |
|                                     | 48        |
| CERAMIC LEADED CHIP CARRIER         | 40        |
|                                     | 48        |

### 44-PIN PLASTIC PLCC

Package Type: 44J



### 48-PIN CERAMIC LEADLESS CHIP CARRIER

Package Type: 48S

