

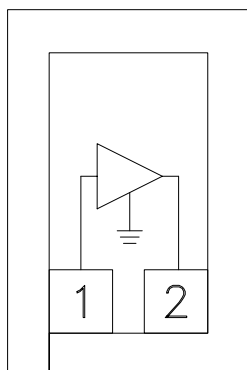
InGaP HBT GAIN BLOCK MMIC AMPLIFIER, DC - 10.0 GHz

Typical Applications

An excellent cascadable 50 Ohm Gain Block or LO Driver for:

- Microwave & VSAT Radios
- Test Equipment
- Military EW, ECM, C³I
- Space Telecom

Functional Diagram



Features

- Gain: 16 dB
- P1dB Output Power: +13 dBm
- Stable Gain Over Temperature
- 50 Ohm I/O's
- Small Size: 0.38 mm x 0.58 mm x 0.1 mm

General Description

The HMC405 die is a GaAs InGaP Heterojunction Bipolar Transistor (HBT) Gain Block MMIC DC to 10 GHz amplifier. This amplifier can be used as either a cascadable 50 Ohm gain stage or to drive the LO of HMC mixers with up to +17dBm output power. The HMC405 offers 16 dB of gain and an output IP3 of +32 dBm while requiring only 50 mA from a +5V supply. The Darlington feedback pair used results in reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring a minimal number of external bias components. The HMC405 can easily be integrated into Multi-Chip-Modules (MCMs) due to its small (0.22mm²) size. All data is with the chip in a 50 Ohm test fixture connected via 0.025mm (1 mil) diameter wire bonds of minimal length 0.5mm (20 mils).

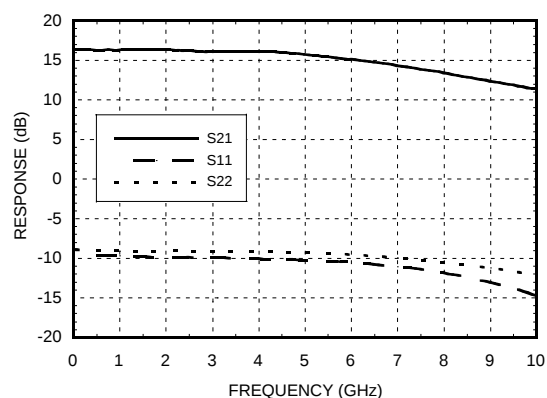
Electrical Specifications, $V_s = +5.0V$, $R_{bias} = 22\text{ Ohm}$, $T_A = +25^\circ\text{C}$

Parameter	Min.	Typ.	Max.	Units
Gain		DC - 3.0 GHz	16	dB
		3.0 - 7.0 GHz	15	dB
		7.0 - 10.0 GHz	13	dB
Gain Variation Over Temperature		DC - 3.0 GHz	0.004	dB/ °C
		3.0 - 7.0 GHz	0.015	dB/ °C
		7.0 - 10.0 GHz	0.02	dB/ °C
Input Return Loss		DC - 3.0 GHz	10	dB
		3.0 - 10.0 GHz	11	dB
Output Return Loss		DC - 3.0 GHz	9	dB
		3.0 - 10.0 GHz	10	dB
Reverse Isolation		DC - 7.0 GHz	20	dB
		7.0 - 10.0 GHz	17	dB
Output Power for 1 dB Compression (P1dB)		DC - 3.0 GHz	15	dBm
		3.0 - 7.0 GHz	13	dBm
		7.0 - 10.0 GHz	10	dBm
Output Third Order Intercept (IP3)		DC - 3.0 GHz	30	dBm
		3.0 - 7.0 GHz	25	dBm
		7.0 - 10.0 GHz	22	dBm
Noise Figure		DC - 7.0 GHz	4	dB
		7.0 - 10.0 GHz	4.5	dB
Supply Current (I _{cc})			50	mA

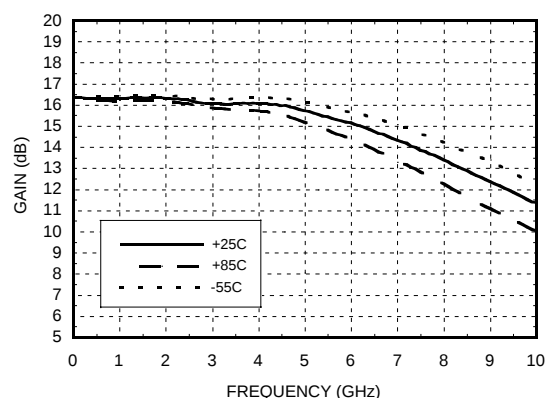
Note: Data taken with broadband bias tee on device output.

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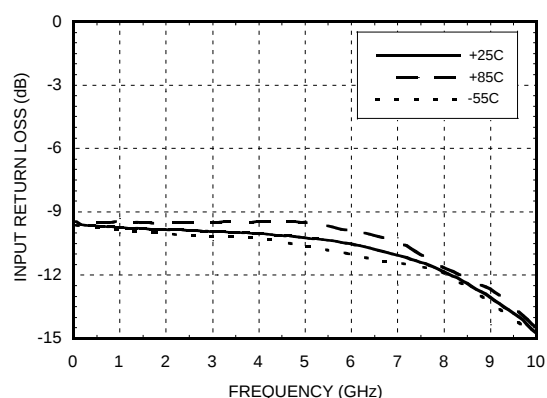
Gain & Return Loss



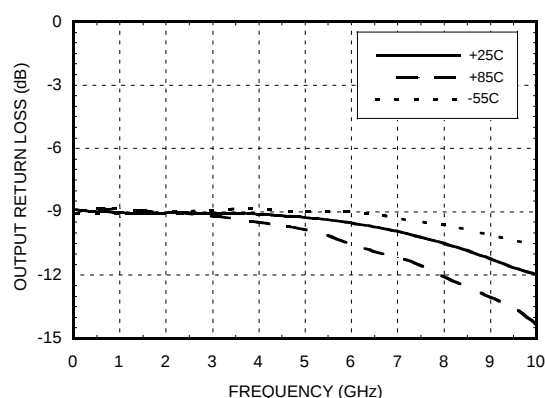
Gain vs. Temperature



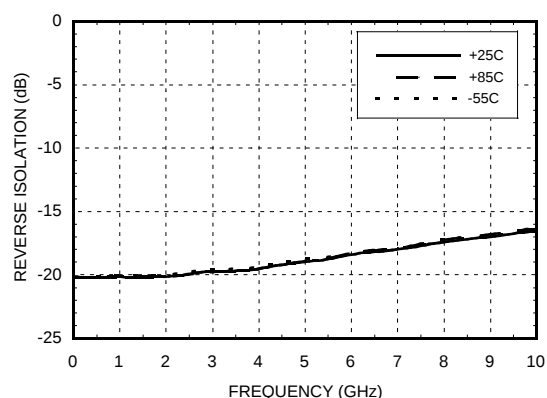
Input Return Loss vs. Temperature



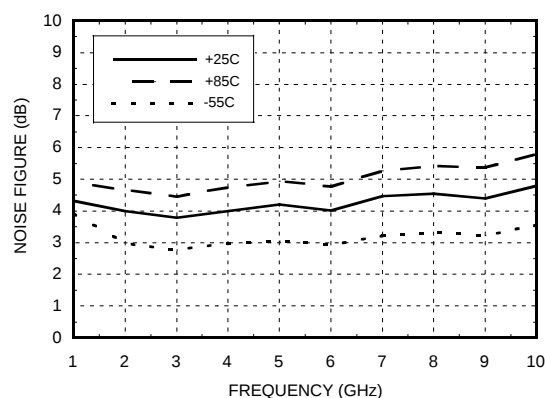
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



Noise Figure vs. Temperature

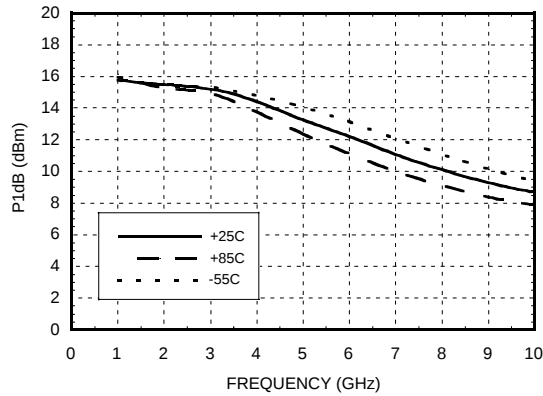


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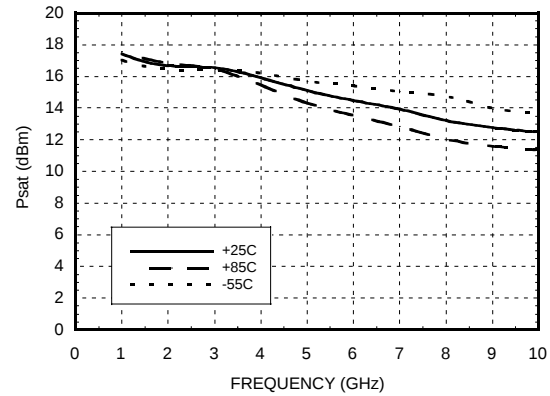
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AMPLIFIERS - CHIP

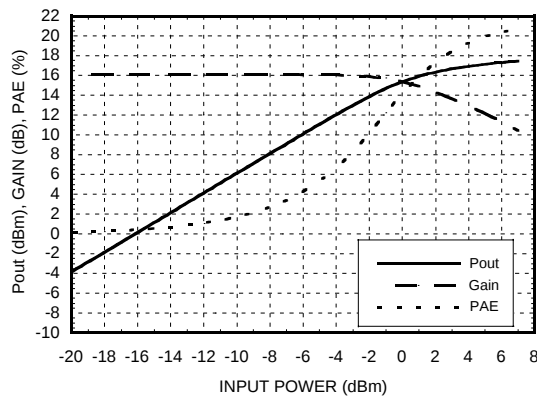
P1dB vs. Temperature



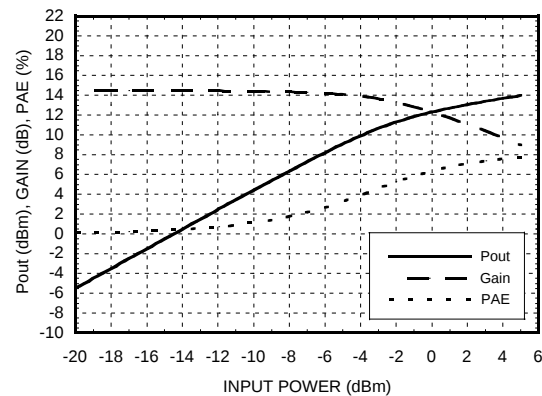
Psat vs. Temperature



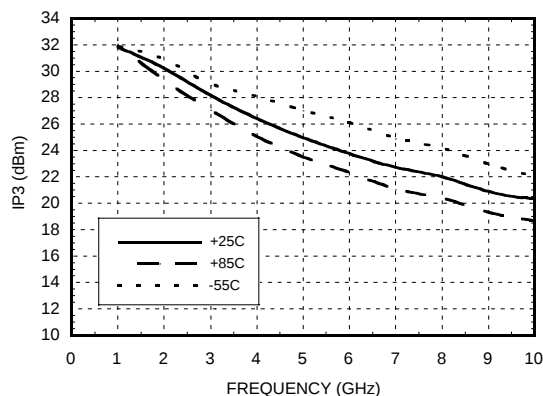
Power Compression @ 1 GHz



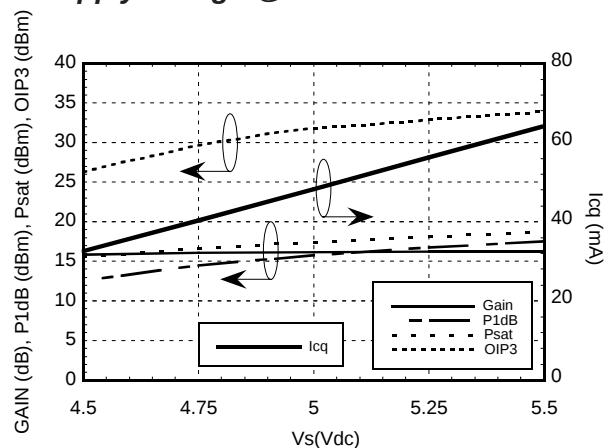
Power Compression @ 7 GHz



Output IP3 vs. Temperature



Gain, Power, OIP3 & Supply Current vs. Supply Voltage @ 1 GHz

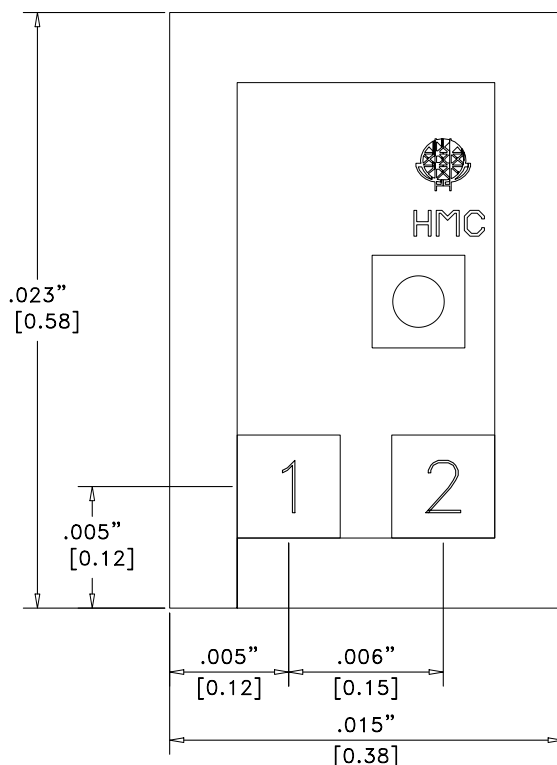


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Absolute Maximum Ratings

Collector Bias Voltage	+7.0 Vdc
RF Input Power (RFin)(Vcc = +5.0 Vdc)	+10 dBm
Junction Temperature	150 °C
Continuous P _{diss} (T= 85 °C) (derate 5.21 mW/°C above 85 °C)	0.339 W
Thermal Resistance (junction to die bottom)	192 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

Outline Drawing



NOTES:

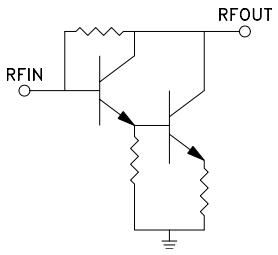
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. ALL TOLERANCES ARE ± 0.001 (0.025)
3. DIE THICKNESS IS 0.004 (0.100) BACKSIDE IS GROUND
4. BOND PADS ARE 0.004 (0.100) SQUARE
5. BOND PAD SPACING, CTR-CTR: 0.006 (0.150)
6. BACKSIDE METALLIZATION: GOLD
7. BOND PAD METALLIZATION: GOLD

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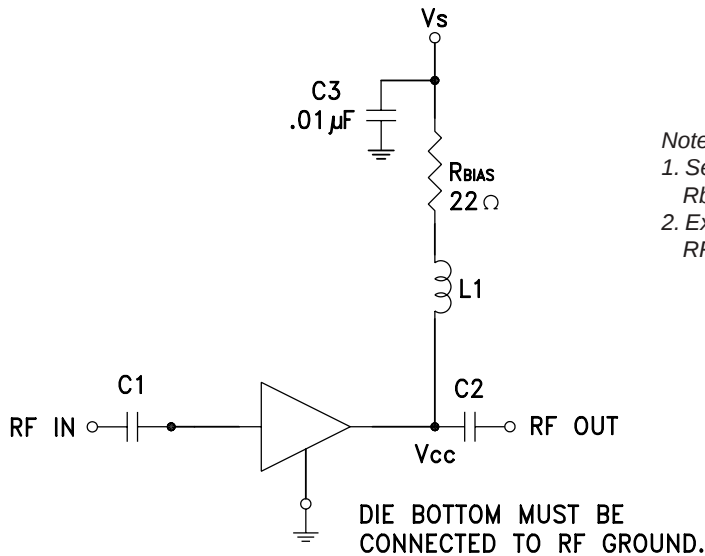
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AMPLIFIERS - CHIP

Pad Descriptions

Pin Number	Function	Description	Interface Schematic
1	RFIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
2	RFOUT	RF output and DC Bias for the output stage.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

Application Circuit



Note:

1. Select R_{bias} to achieve I_{cq} using equation below,
 $R_{bias} \geq 22 \text{ Ohm}$.
2. External blocking capacitors are required on
 R_{FIN} and R_{FOUT} .

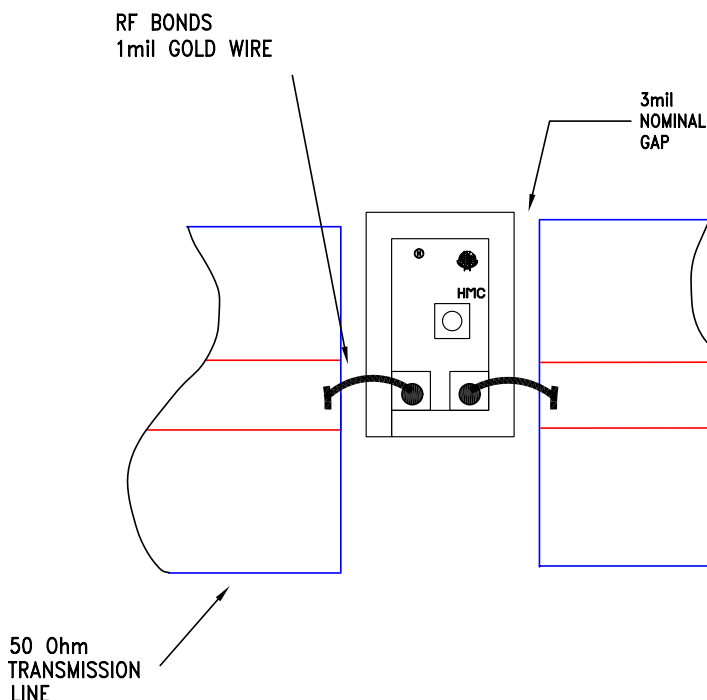
$$I_{cq} = \frac{V_s - 3.9}{R_{bias}}$$

Recommended Component Values

Component	Frequency (MHz)			
	50	1000	3000	7000
L1	270 nH	56 nH	8.2 nH	2.2 nH
C1, C2	0.01 μ F	100 pF	100 pF	100 pF

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Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against $\pm 250V$ ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 deg. C and a tool temperature of 265 deg. C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 deg. C. DO NOT expose the chip to a temperature greater than 320 deg. C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible $<0.31mm$ (12 mils).