

High Voltage, Internally Compensated Operational Amplifier

The MC1436, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage: ± 40 Vdc (MC1536)
- Output Voltage Swing:
 ± 30 Vpk(min) ($V_{CC} = +36$ V, $V_{EE} = -36$ V) (MC1536)
 ± 22 Vpk(min) ($V_{CC} = +28$ V, $V_{EE} = -28$ V)
- Input Bias Current: 20 nA max (MC1536)
- Input Offset Current: 3.0 nA max (MC1536)
- Fast Slew Rate: 2.0 V/ μ s typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Overvoltage Protection
- A_{VOL} : 500,000 typ
- Characteristics Independent of Power Supply Voltages:
(± 5.0 Vdc to ± 36 Vdc)

**Figure 1. Differential Amplifier with ± 20 V
Common Mode Input Voltage Range**

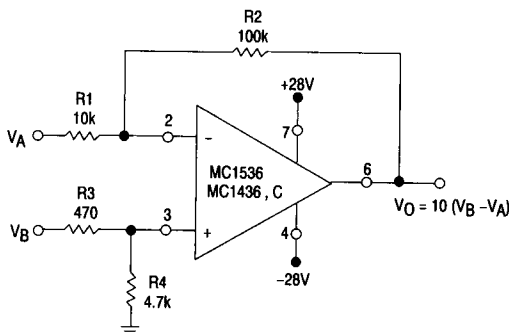
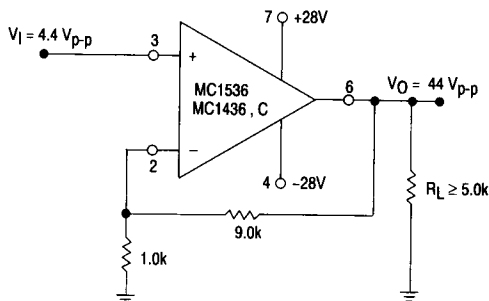


Figure 2. Typical Noninverting X10 Voltage Amplifier



MC1436, C
MC1536

OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

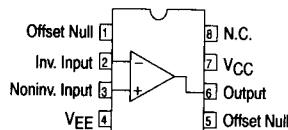


U SUFFIX
CERAMIC PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1436CD, D	0° to +70°C	SO-8
MC1436P1, CP1		Plastic DIP
MC1436CU, U		Ceramic DIP
MC1536U	-55° to +125°C	Ceramic DIP

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Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V _{CC} V _{EE}	+40 -40	+34 -34	+30 -30	V _{dc}
Input Differential Voltage Range	V _{IDR}	Note 3			V
Input Common Mode Voltage Range	V _{ICR}	Note 3			V
Output Short Circuit Duration (V _{CC} = V _{EE} = 28 V _{dc} , V _O = 0)	t _{SC}	5.0			sec
Power Dissipation (Package Limitation) Derate above T _A = +25°C	P _D	680 4.6			mW mW/°C
Operating Ambient Temperature Range	T _A	-55 to +125	0 to +70		°C
Storage Temperature Range	T _{sta}	-65 to +150			°C

Characteristics	Symbol	MC1536			MC1436			MC1436C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$ (See Note 1)	I_{IB}	—	8.0	20 35	—	15 —	40 55	—	25 —	90 —	nAdc
Input Offset Current $T_A = +25^\circ\text{C}$ $T_A = +25^\circ\text{C} \text{ to } T_{\text{high}}$ $T_A = T_{\text{low}} \text{ to } +25^\circ\text{C}$	I_{IO}	—	1.0	3.0 4.5 7.0	—	5.0 — —	10 14 14	—	10 — —	25 — —	nAdc
Input Offset Voltage $T_A = +25^\circ\text{C}$ $T_A = T_{\text{low}} \text{ to } T_{\text{high}}$	V_{IO}	—	2.0	5.0 7.0	—	5.0 —	10 14	—	5.0 —	12 —	mVdc
Differential Input Impedance (Open-loop, $f \leq 5.0 \text{ Hz}$) Parallel Input Resistance Parallel Input Capacitance	r_{p} C_{p}	—	10 2.0	—	—	10 2.0	—	—	10 2.0	—	M Ω pF
Common Mode Input Impedance ($f \leq 5.0 \text{ Hz}$)	z_{ic}	—	250	—	—	250	—	—	250	—	M Ω
Input Common Mode Voltage Range	V_{ICR}	± 24	± 25	—	± 22	± 25	—	± 18	± 20	—	Vpk
Equivalent Input Noise Voltage ($A_{\text{V}} = 100$, $R_{\text{S}} = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$, $\text{BW} = 1.0 \text{ Hz}$)	e_{n}	—	50	—	—	50	—	—	50	—	nV/(Hz) $^{1/2}$
Common Mode Rejection (dc)	CMR	80	110	—	70	110	—	50	90	—	dB
Large Signal DC Open-Loop Voltage Gain ($V_{\text{O}} = \pm 10 \text{ V}$, $R_{\text{L}} = 100 \text{ k}\Omega$) $\begin{cases} T_A = +25^\circ\text{C} \\ T_A = T_{\text{low}} \text{ to } T_{\text{high}} \end{cases}$ ($V_{\text{O}} = \pm 10 \text{ V}$, $R_{\text{L}} = 10 \text{ k}\Omega$, $T_A = +25^\circ\text{C}$)	A_{VOL}	100,000 50,000 —	500,000 — 200,000	— — —	70,000 50,000 —	500,000 — 200,000	— — —	50,000 — —	500,000 — 200,000	— — —	V/V
Power Bandwidth (Voltage Follower) ($A_{\text{V}} = 1$, $R_{\text{L}} = 5.0 \text{ k}\Omega$, $\text{THD} \leq 5\%$, $V_{\text{O}} = 40 V_{\text{p-p}}$)	BWp	—	23	—	—	23	—	—	23	—	kHz
Unity Gain Crossover Frequency (Open-loop)	f_{c}	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Phase Margin (Open-loop, Unity Gain)	ϕ_{m}	—	50	—	—	50	—	—	50	—	Degrees
Gain Margin	A_{M}	—	18	—	—	18	—	—	18	—	dB
Slew Rate (Unity Gain)	SR	—	2.0	—	—	2.0	—	—	2.0	—	V/ μs
Output Impedance ($f \leq 5.0 \text{ Hz}$)	z_{O}	—	1.0	—	—	1.0	—	—	1.0	—	k Ω
Short Circuit Output Current	I_{SC}	—	± 17	—	—	± 17	—	—	± 19	—	mA
Output Voltage Range ($R_{\text{L}} = 5.0 \text{ k}\Omega$) $V_{\text{CC}} = +28 \text{ Vdc}$, $V_{\text{EE}} = -28 \text{ Vdc}$ $V_{\text{CC}} = +36 \text{ Vdc}$, $V_{\text{EE}} = -36 \text{ Vdc}$	V_{O}	± 22 ± 30	± 23 ± 32	—	± 20 —	± 22 —	—	± 20 —	± 22 —	—	V_{pk}
Power Supply Rejection $V_{\text{EE}} = \text{Constant}$, $R_{\text{S}} \leq 10 \text{ k}\Omega$ $V_{\text{CC}} = \text{Constant}$, $R_{\text{S}} \leq 10 \text{ k}\Omega$	PSR + PSR —	— —	15 15	100 100	— —	35 35	200 200	— —	50 50	— —	$\mu\text{V/V}$
Power Supply Current (See Note 2)	I_{CC} I_{EE}	— —	2.2 2.2	4.0 4.0	— —	2.6 2.6	5.0 5.0	— —	2.6 2.6	5.0 5.0	mA
DC Quiescent Power Consumption ($V_{\text{O}} = 0$)	P_{C}	—	124	224	—	146	280	—	146	280	mW

MOTOROLA LINEAR/INTERFACE ICs DEVICE DATA

MC1436,C, MC1536

Figure 3. Low-Drift Sample and Hold

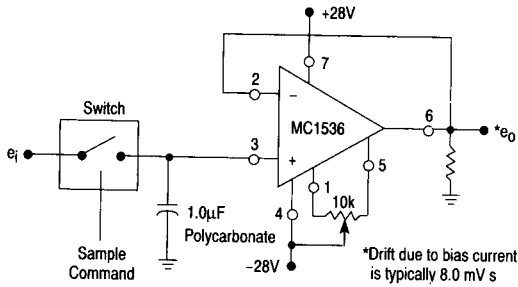


Figure 4. Power Bandwidth

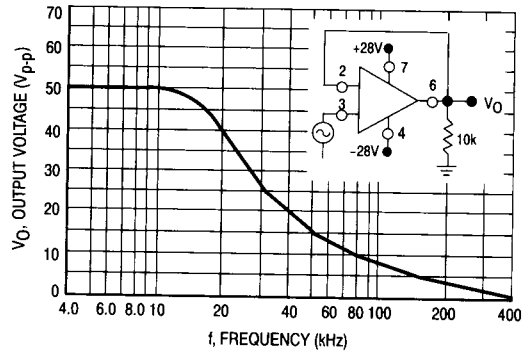


Figure 5. Peak Output Voltage Swing versus Power Supply Voltage

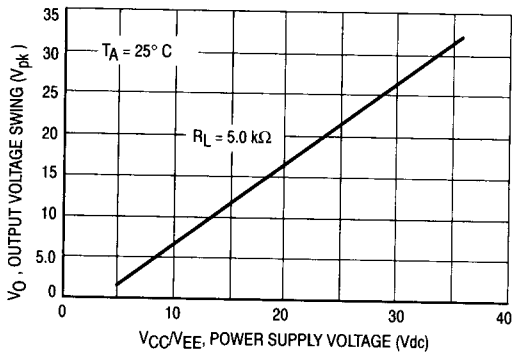


Figure 6. Open-Loop Frequency Response

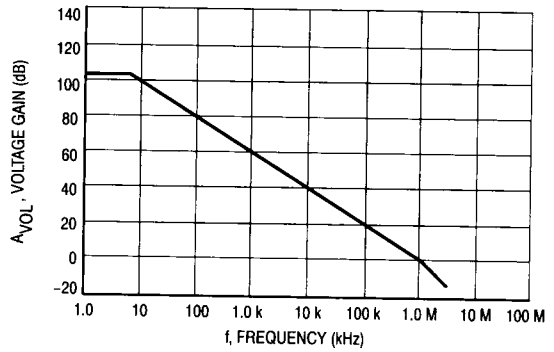


Figure 7. Output Short Circuit Current versus Temperature

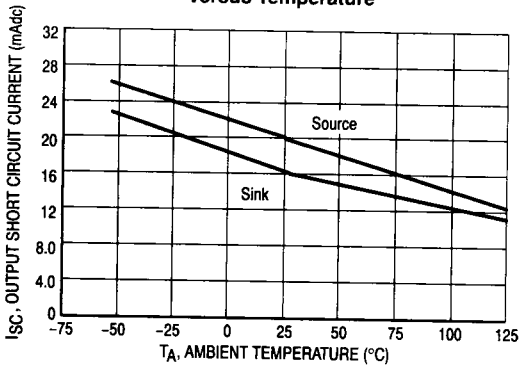
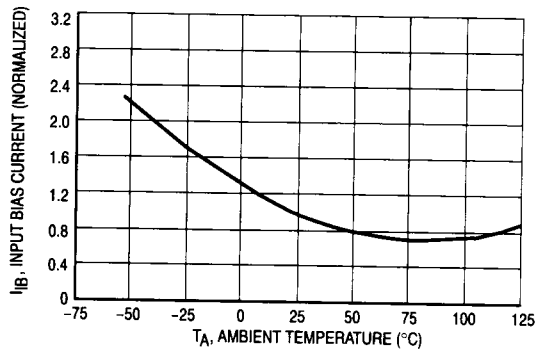


Figure 8. Input Bias Current versus Temperature



MC1436,C, MC1536

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Figure 9. Inverting Feedback Model

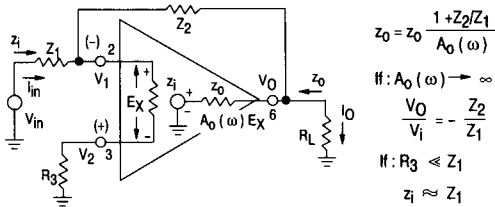


Figure 10. Noninverting Feedback Model

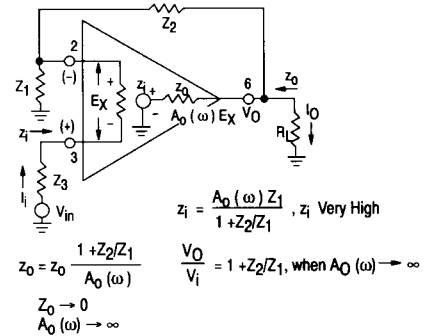


Figure 11. Audio Amplifier

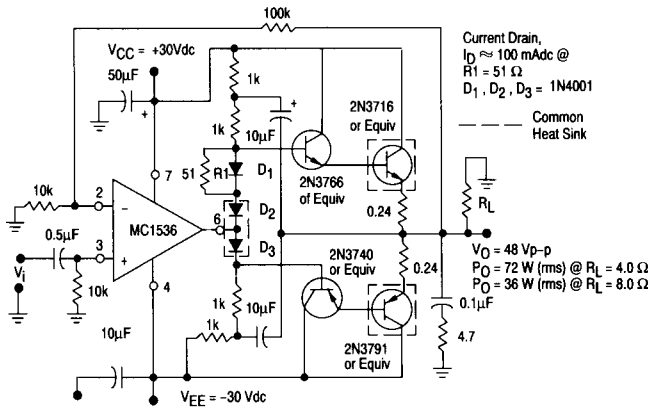


Figure 12. Voltage Controlled Current Source or Transconductance Amplifier with 0 V to 40 V Compliance

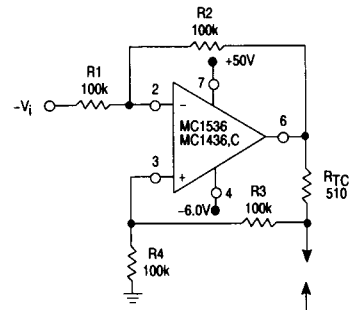


Figure 13. Representative Circuit Schematic

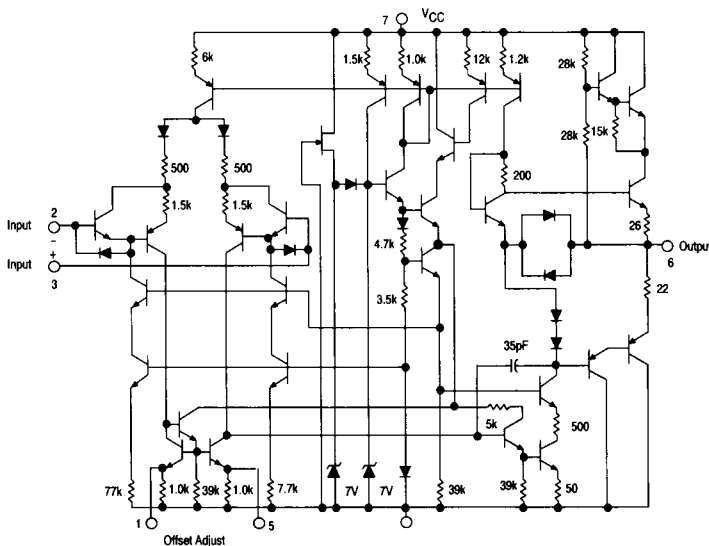


Figure 14. Equivalent Circuit

