# Cap-Free, NMOS, 150mA Low Dropout Regulator with Reverse Current Protection

## FEATURES

- **Stable with No Output Capacitor or Any Value or Type of Capacitor**
- **Input Voltage Range of 1.7V to 5.5V**
- **Ultralow Dropout Voltage: 30mV Typ**
- **Excellent Load Transient Response—with or without Optional Output Capacitor**
- **New NMOS Topology Provides Low Reverse Leakage Current**
- **Low Noise: 30μ$V_{RMS}$ Typ (10kHz to 100kHz)**
- **0.5% Initial Accuracy**
- **1% Overall Accuracy over Line, Load, and Temperature**
- **Less Than 1μA Max $I_Q$ in Shutdown Mode**
- **Thermal Shutdown and Specified Min/Max Current Limit Protection**
- **Available in Multiple Output Voltage Versions**
  - **Fixed Outputs of 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V, and 5.0V**
  - **Adjustable Outputs From 1.20V to 5.5V**
  - **Custom Outputs Available**

## APPLICATIONS

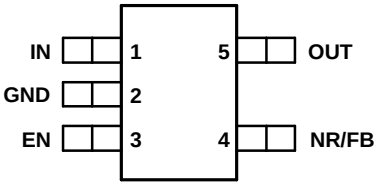
- **Portable/Battery-Powered Equipment**
- **Post-Regulation for Switching Supplies**
- **Noise-Sensitive Circuitry such as VCOs**
- **Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors**

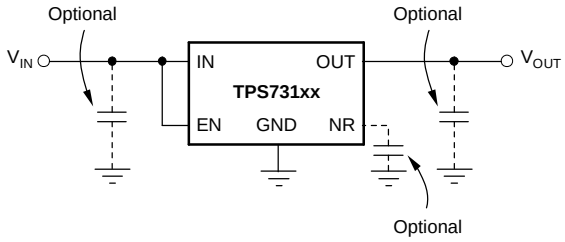
## DESCRIPTION

The TPS731xx family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS731xx uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1μA and ideal for portable applications. The extremely low output noise (30μ$V_{RMS}$ with 0.1μF $C_{NR}$) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

**DBV PACKAGE**
**SOT23**
**(TOP VIEW)**




**Typical Application Circuit for Fixed-Voltage Versions**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | $V_{OUT}$(1) | PACKAGE-LEAD (DESIGNATOR)(2) | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| TPS73101 | Adjustable or 1.2V(3) | SOT23-5 (DBV) | -40°C to +125°C | PWYQ | TPS73101DBVT | Tape and Reel, 250 |
| | | | | | TPS73101DBVR | Tape and Reel, 3000 |
| TPS73115 | 1.5V | SOT23-5 (DBV) | -40°C to +125°C | T31 | TPS73115DBVT | Tape and Reel, 250 |
| | | | | | TPS73115DBVR | Tape and Reel, 3000 |
| TPS73118 | 1.8V | SOT23-5 (DBV) | -40°C to +125°C | T32 | TPS73118DBVT | Tape and Reel, 250 |
| | | | | | TPS73118DBVR | Tape and Reel, 3000 |
| TPS73125 | 2.5V | SOT23-5 (DBV) | -40°C to +125°C | PHWI | TPS73125DBVT | Tape and Reel, 250 |
| | | | | | TPS73125DBVR | Tape and Reel, 3000 |
| TPS73130 | 3.0V | SOT23-5 (DBV) | -40°C to +125°C | T33 | TPS73130DBVT | Tape and Reel, 250 |
| | | | | | TPS73130DBVR | Tape and Reel, 3000 |
| TPS73132 | 3.2V | SOT23-5 (DBV) | -40°C to +125°C | T52 | TPS73132DBVT | Tape and Reel, 250 |
| | | | | | TPS73132DBVR | Tape and Reel, 3000 |
| TPS73133 | 3.3V | SOT23-5 (DBV) | -40°C to +125°C | T34 | TPS73133DBVT | Tape and Reel, 250 |
| | | | | | TPS73133DBVR | Tape and Reel, 3000 |
| TPS73150 | 5.0V | SOT23-5 (DBV) | -40°C to +125°C | T35 | TPS73150DBVT | Tape and Reel, 250 |
| | | | | | TPS73150DBVR | Tape and Reel, 3000 |

(1) Custom output voltages from 1.3V to 4V in 100mV increments are available on a quick-turn basis for prototyping. Minimum order quantities apply; contact factory for details and availability.
(2) For the most current specification and package information, refer to the Package Option Addendum located at the end of this datasheet.
(3) For fixed 1.2V operation, tie FB to OUT.

## ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)

| | TPS731xx | UNIT |
|---|---|---|
| $V_{IN}$ range | -0.3 to 6.0 | V |
| $V_{EN}$ range | -0.3 to 6.0 | V |
| $V_{OUT}$ range | -0.3 to 5.5 | V |
| Peak output current | Internally limited | |
| Output short-circuit duration | Indefinite | |
| Continuous total power dissipation | See Dissipation Ratings Table | |
| Junction temperature range, $T_J$ | -55 to +150 | °C |
| Storage temperature range | -65 to +150 | °C |
| ESD rating, HBM | 2 | kV |
| ESD rating, CDM | 500 | V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

## POWER DISSIPATION RATINGS(1)

| BOARD | PACKAGE | $R_{\Theta JC}$ | $R_{\Theta JA}$ | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A \le 25°C$ POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| Low-K(2) | DBV | 64°C/W | 255°C/W | 3.9mW/°C | 390mW | 215mW | 155mW |
| High-K (3) | DBV | 64°C/W | 180°C/W | 5.6mW/°C | 560mW | 310mW | 225mW |

(1) See *Power Dissipation* in the ***Applications*** section for more information related to thermal design.
(2) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch x 3 inch, two-layer board with 2-ounce copper traces on top of the board.
(3) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J$ = -40°C to +125°C), $V_{IN} = V_{OUT(nom)} + 0.5V$(1), $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range(1) | | | 1.7 | | 5.5 | V |
| $V_{FB}$ | Internal reference (TPS73101) | | $T_J$ = 25°C | 1.198 | 1.20 | 1.210 | V |
| $V_{OUT}$ | Output voltage range (TPS73101) | | | $V_{FB}$ | | 5.5 - $V_{DO}$ | V |
| | Accuracy(1) | Nominal | $T_J$ = 25°C | -0.5 | | +0.5 | % |
| | | $V_{IN}$, $I_{OUT}$, and T | $V_{OUT}$ + 0.5V ≤ $V_{IN}$ ≤ 5.5V; 10 mA ≤ $I_{OUT}$≤ 150mA | -1.0 | ±0.5 | +1.0 | |
| $\Delta V_{OUT}\%/\Delta V_{IN}$ | Line regulation(1) | | $V_{OUT(nom)}$ + 0.5V ≤ $V_{IN}$ ≤ 5.5V | | 0.01 | | %/V |
| $\Delta V_{OUT}\%/\Delta I_{OUT}$ | Load regulation | | 1mA ≤ $I_{OUT}$ ≤ 150mA | | 0.002 | | %/mA |
| | | | 10mA ≤ $I_{OUT}$ ≤ 150mA | | 0.0005 | | |
| $V_{DO}$ | Dropout voltage(2) ($V_{IN}$ = $V_{OUT}$ (nom) - 0.1V) | | $I_{OUT}$ = 150mA | | 30 | 100 | mV |
| $Z_O$(DO) | Output impedance in dropout | | 1.7 V ≤ $V_{IN}$ ≤ $V_{OUT}$ + $V_{DO}$ | | 0.25 | | Ω |
| $I_{CL}$ | Output current limit | | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | 150 | 360 | 500 | mA |
| $I_{SC}$ | Short-circuit current | | $V_{OUT}$ = 0V | | 200 | | mA |
| $I_{REV}$ | Reverse leakage current(3) (-$I_{IN}$) | | $V_{EN}$ ≤ 0.5V, 0V≤ $V_{IN}$ ≤ $V_{OUT}$ | | 0.1 | 10 | µA |
| $I_{GND}$ | Ground pin current | | $I_{OUT}$ = 10mA ($I_Q$) | | 400 | 550 | µA |
| | | | $I_{OUT}$ = 150mA | | 550 | 750 | |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | | $V_{EN}$ ≤ 0.5V, $V_{OUT}$ ≤ $V_{IN}$ ≤ 5.5 | | 0.02 | 1 | µA |
| $I_{FB}$ | FB pin current (TPS73101) | | | | 0.1 | 0.3 | µA |
| PSRR | Power-supply rejection ratio (ripple rejection) | | f = 100Hz, $I_{OUT}$ = 150 mA | | 58 | | dB |
| | | | f = 10kHz, $I_{OUT}$ = 150 mA | | 37 | | |
| $V_N$ | Output noise voltage BW = 10Hz - 100kHz | | $C_{OUT}$ = 10µF, No $C_{NR}$ | | 27 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | $C_{OUT}$ = 10µF, $C_{NR}$ = 0.01µF | | 8.5 × $V_{OUT}$ | | |
| $t_{STR}$ | Startup time | | $V_{OUT}$ = 3V, $R_L$ = 30Ω $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF | | 600 | | µs |
| $V_{EN}$(HI) | Enable high (enabled) | | | 1.7 | | $V_{IN}$ | V |
| $V_{EN}$(LO) | Enable low (shutdown) | | | 0 | | 0.5 | V |
| $I_{EN}$(HI) | Enable pin current (enabled) | | $V_{EN}$ = 5.5V | | 0.02 | 0.1 | µA |
| $T_{SD}$ | Thermal shutdown temperature | | Shutdown Temp increasing | | 160 | | °C |
| | | | Reset Temp decreasing | | 140 | | |
| $T_J$ | Operating junction temperature | | | -40 | | 125 | °C |

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.7V, whichever isgreater.
(2) $V_{DO}$ is not measured for the TPS73115 ($V_{O(nom)}$ = 1.5V) since minimum $V_{IN}$ = 1.7V.
(3) Fixed-voltage versions only; refer to the ***Applications*** section for more information.

## FUNCTIONAL BLOCK DIAGRAMS

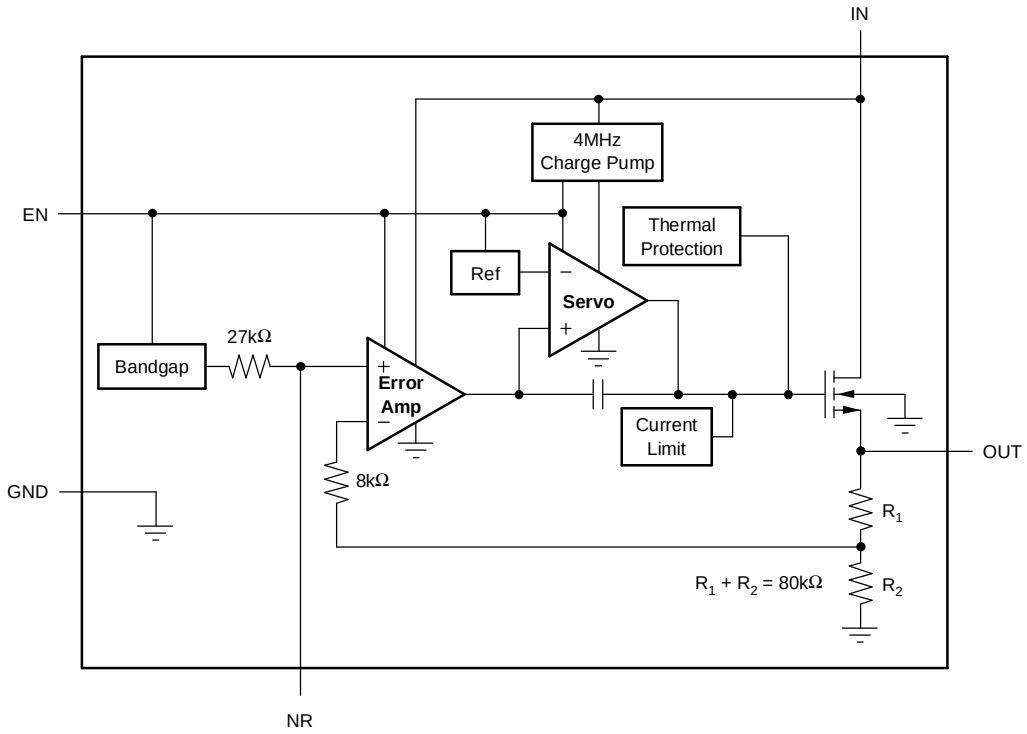



**Figure 1. Fixed Voltage Version**

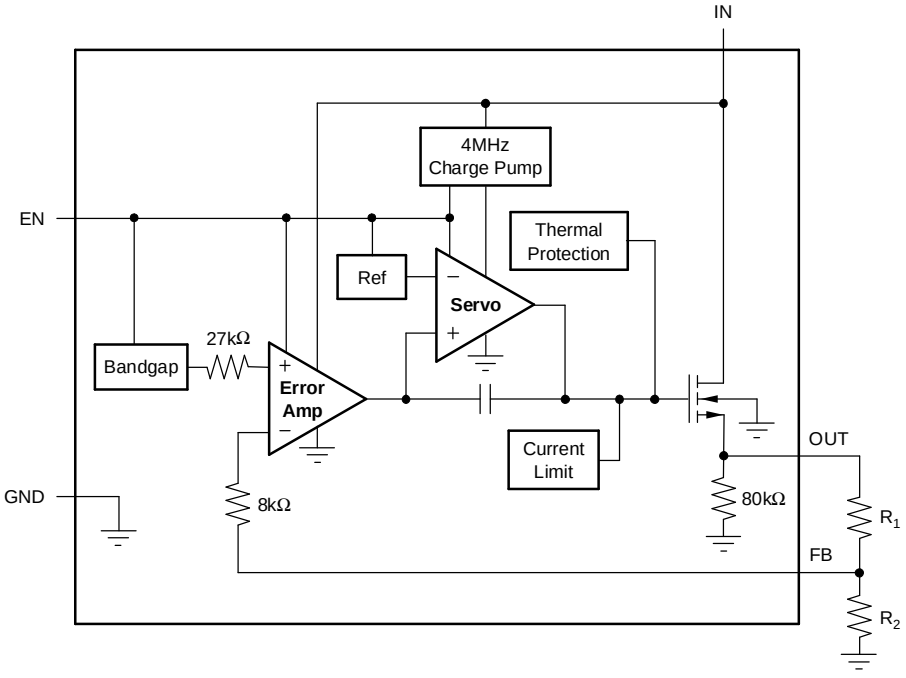



**Figure 2. Adjustable Voltage Version**

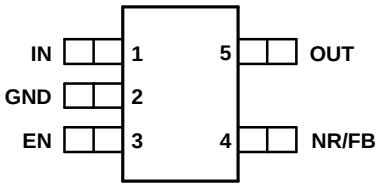
**Table 1. Standard 1% Resistor Values for Common Output Voltages**

| $V_O$ | $R_1$ | $R_2$ |
|---|---|---|
| 1.2V | Short | Open |
| 1.5V | 23.2kΩ | 95.3kΩ |
| 1.8V | 28.0kΩ | 56.2kΩ |
| 2.5V | 39.2kΩ | 36.5kΩ |
| 2.8V | 44.2kΩ | 33.2kΩ |
| 3.0V | 46.4kΩ | 30.9kΩ |
| 3.3V | 52.3kΩ | 30.1kΩ |
| 5.0V | 78.7kΩ | 24.9kΩ |

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

## PIN ASSIGNMENTS

**DBV PACKAGE**
**SOT23**
**(TOP VIEW)**




## TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | SOT23 (DBV) PIN NO. | |
| IN | 1 | Unregulated input supply |
| GND | 2 | Ground |
| EN | 3 | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the Shutdown section under Applications Information for more details. EN can be connected to IN if not used. |
| NR | 4 | Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels. |
| FB | 4 | Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device. |
| OUT | 5 | Output of the regulator. There are no output capacitor requirements for stability. |

## TYPICAL CHARACTERISTICS

For all voltage versions at $T_J$= 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.

**LOAD REGULATION**

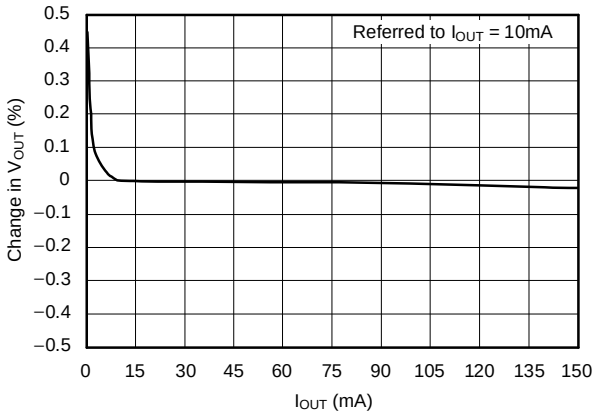



**Figure 3.**

**LINE REGULATION**

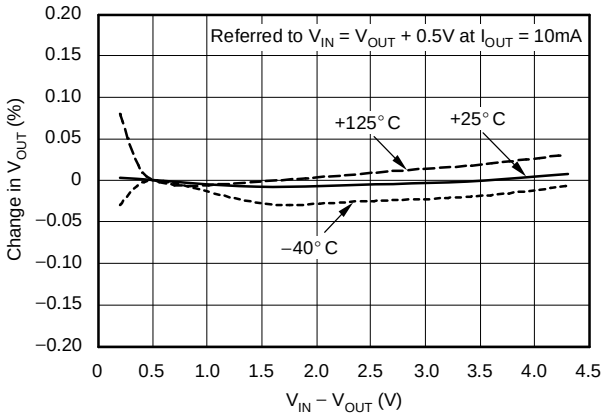



**Figure 4.**

**DROPOUT VOLTAGE vs OUTPUT CURRENT**

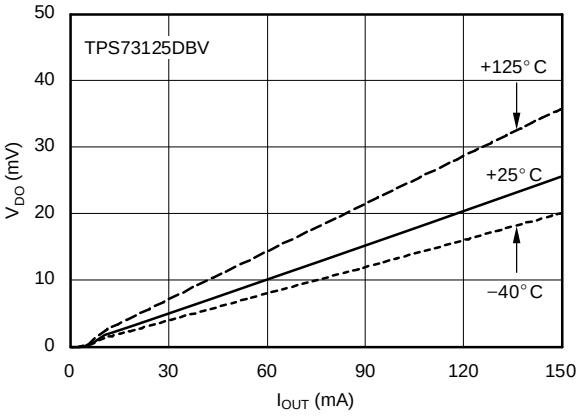



**Figure 5.**

**DROPOUT VOLTAGE vs TEMPERATURE**

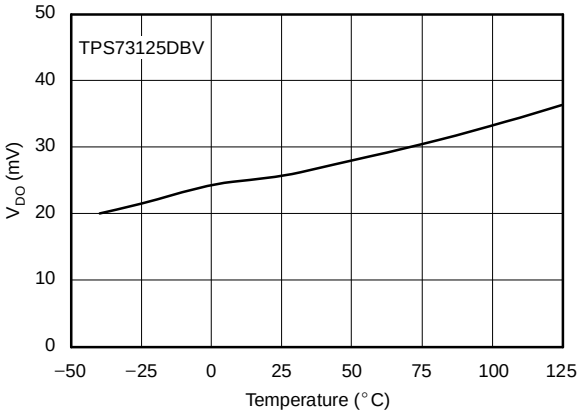



**Figure 6.**

**OUTPUT VOLTAGE ACCURACY HISTOGRAM**

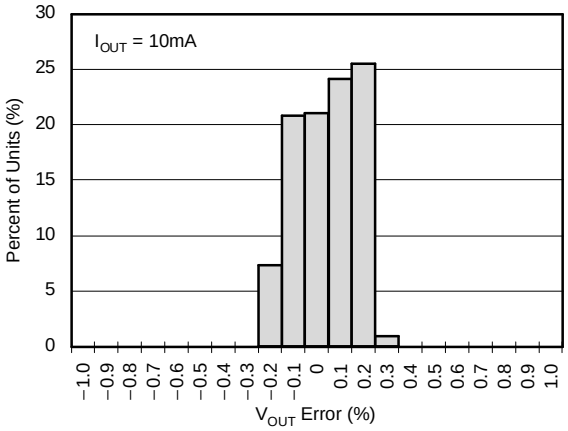



**Figure 7.**

**OUTPUT VOLTAGE DRIFT HISTOGRAM**

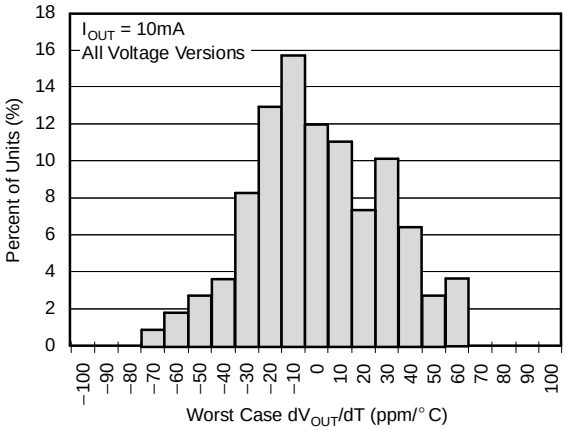



**Figure 8.**

## TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J$= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.

**GROUND PIN CURRENT vs OUTPUT CURRENT**

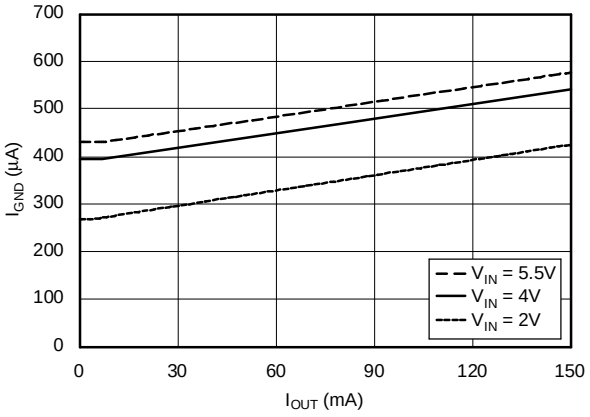



**Figure 9.**

**GROUND PIN CURRENT vs TEMPERATURE**

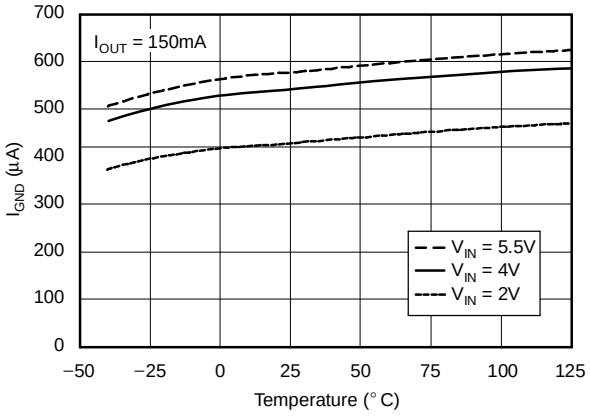



**Figure 10.**

**CURRENT LIMIT vs $V_{OUT}$ (FOLDBACK)**

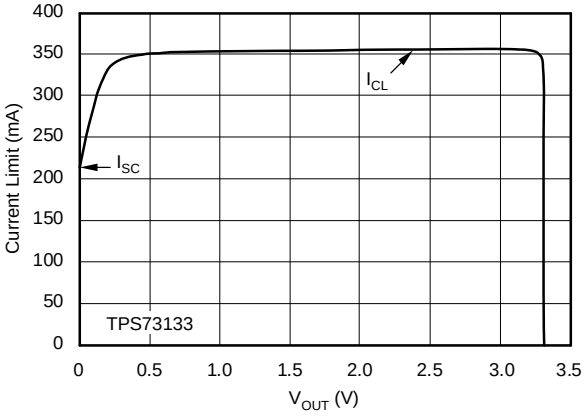



**Figure 11.**

**GROUND PIN CURRENT in SHUTDOWN vs TEMPERATURE**

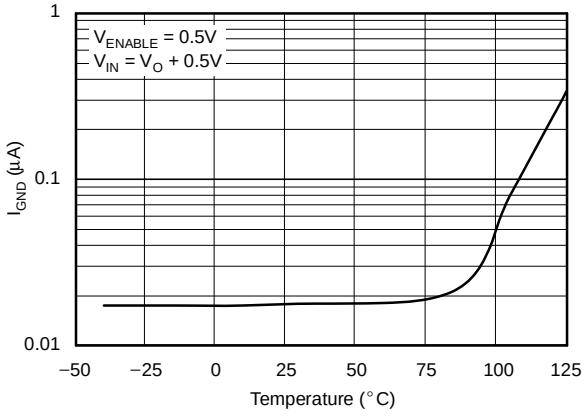



**Figure 12.**

**CURRENT LIMIT vs $V_{IN}$**

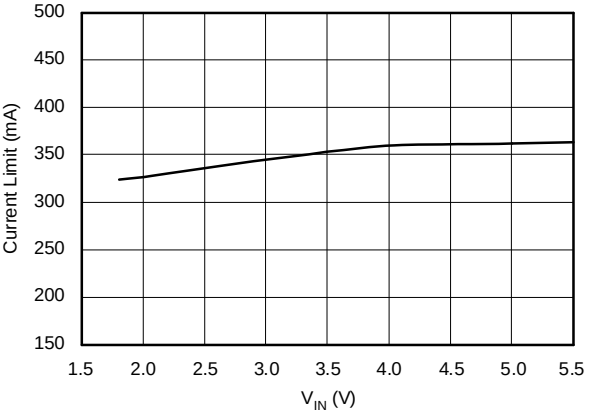



**Figure 13.**

**CURRENT LIMIT vs TEMPERATURE**

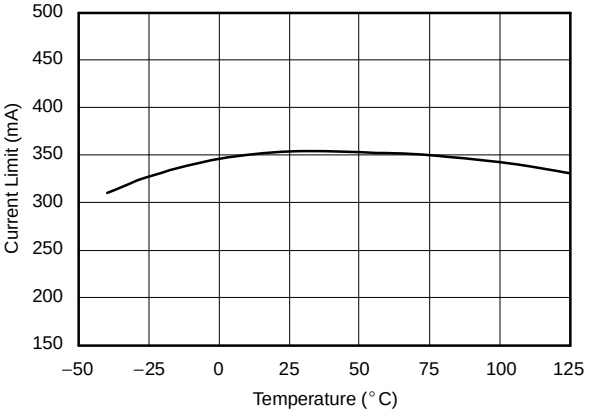



**Figure 14.**

## TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J$= 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.

**PSRR (RIPPLE REJECTION) vs FREQUENCY**

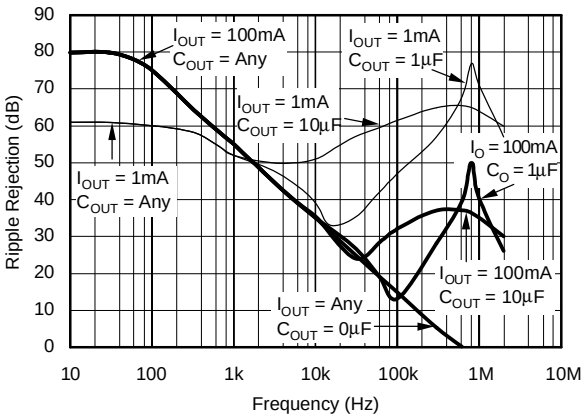



**Figure 15.**

**PSRR (RIPPLE REJECTION) vs $V_{IN}$ - $V_{OUT}$**

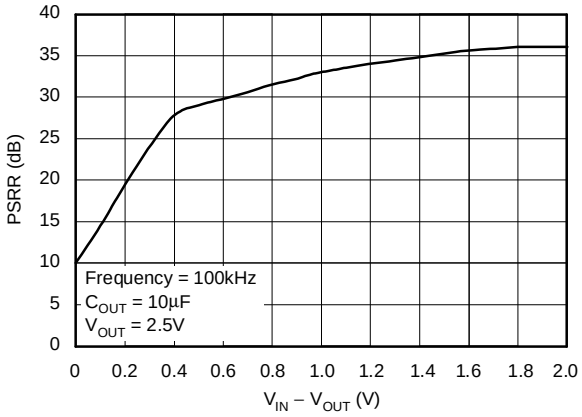



**Figure 16.**

**NOISE SPECTRAL DENSITY**
**$C_{NR}$ = 0µF**

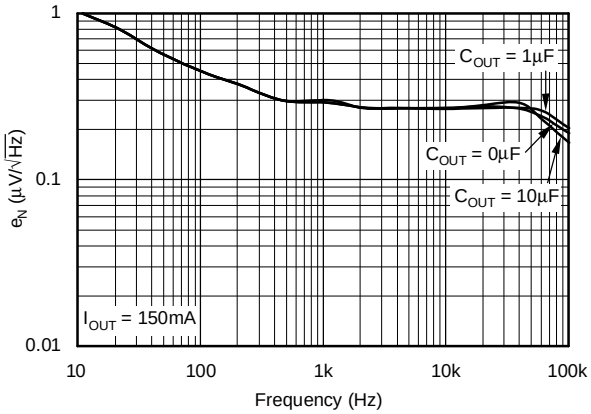



**Figure 17.**

**NOISE SPECTRAL DENSITY**
**$C_{NR}$ = 0.01µF**

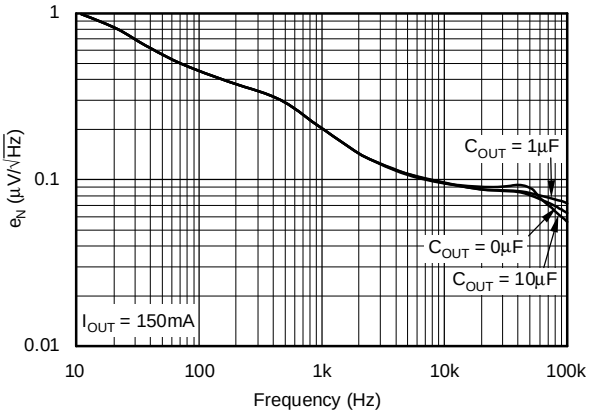



**Figure 18.**

**RMS NOISE VOLTAGE vs $C_{OUT}$**

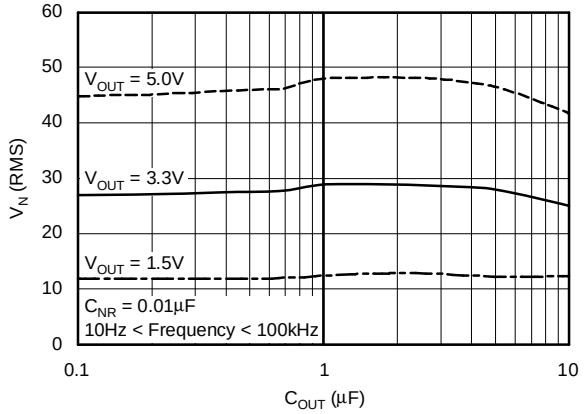



**Figure 19.**

**RMS NOISE VOLTAGE vs $C_{NR}$**

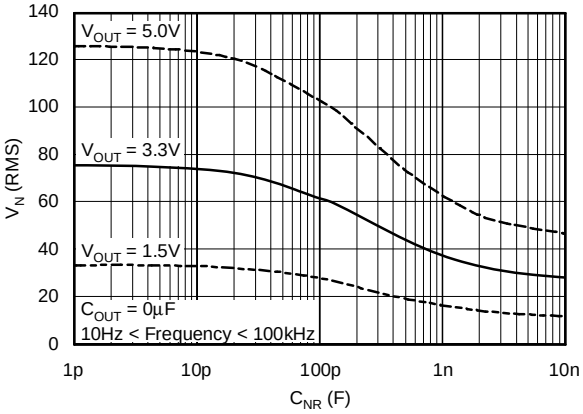



**Figure 20.**

## TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J$= 25°C, $V_{IN} = V_{OUT(nom)} + 0.5V$, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.

**TPS73133**
**LOAD TRANSIENT RESPONSE**

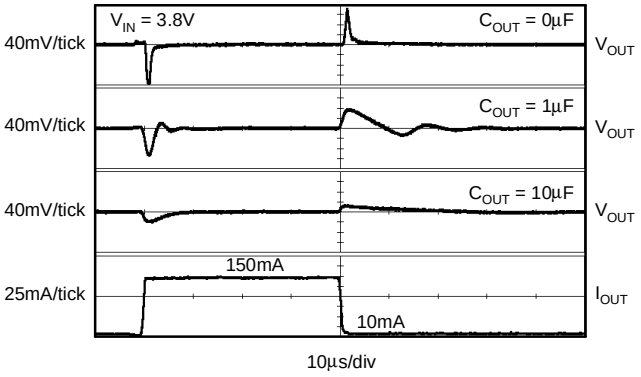



**Figure 21.**

**TPS73133**
**LINE TRANSIENT RESPONSE**

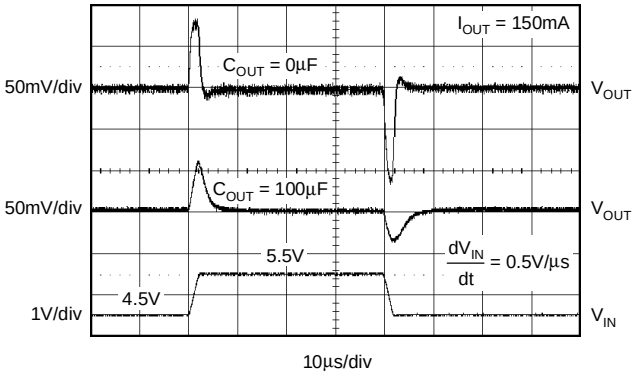



**Figure 22.**

**TPS73133**
**TURN-ON RESPONSE**

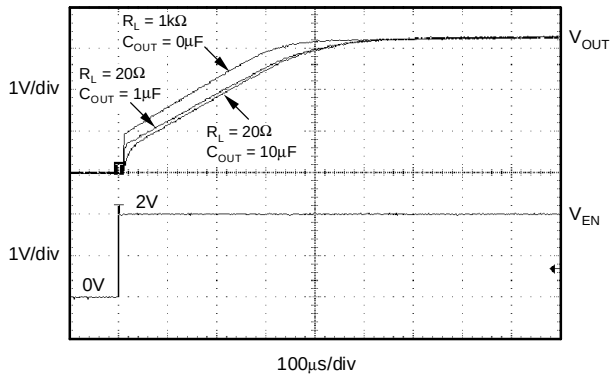



**Figure 23.**

**TPS73133**
**TURN-OFF RESPONSE**

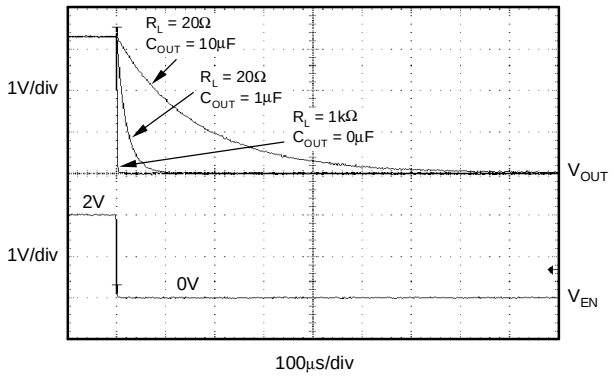



**Figure 24.**

**TPS73133**
**POWER UP / POWER DOWN**

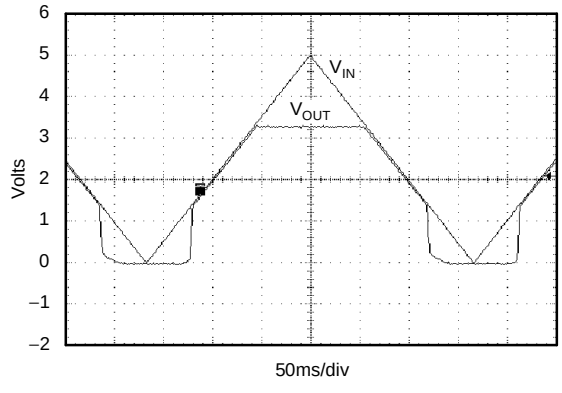



**Figure 25.**

**$I_{ENABLE}$ vs TEMPERATURE**

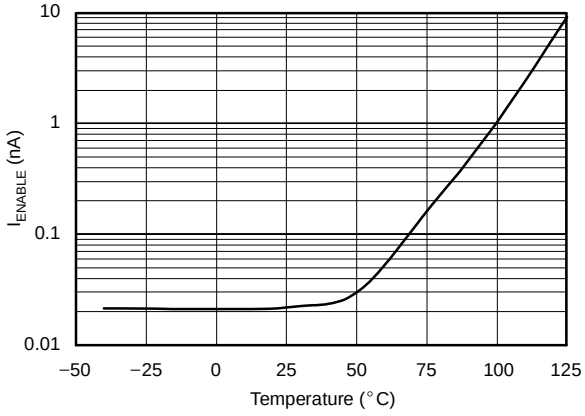



**Figure 26.**

## TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J$= 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V, $I_{OUT}$ = 10mA, $V_{EN}$ = 1.7V, and $C_{OUT}$ = 0.1µF, unless otherwise noted.

**TPS73101**
**RMS NOISE VOLTAGE vs $C_{ADJ}$**

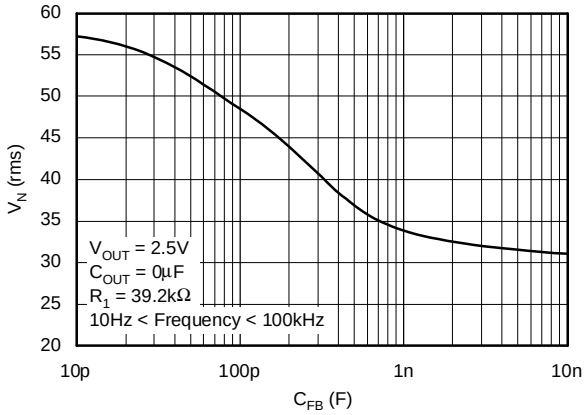



**Figure 27.**

**TPS73101**
**$I_{FB}$ vs TEMPERATURE**

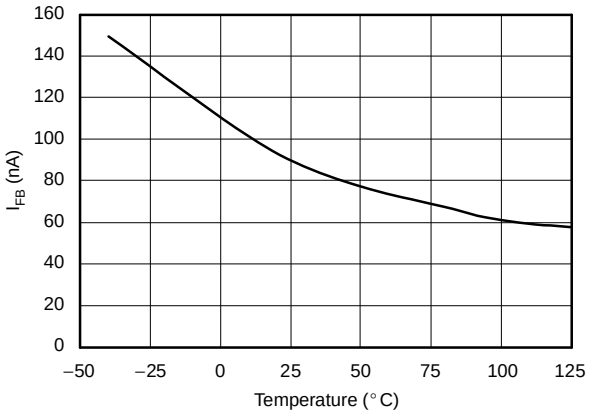



**Figure 28.**

**TPS73101**
**LOAD TRANSIENT, ADJUSTABLE VERSION**

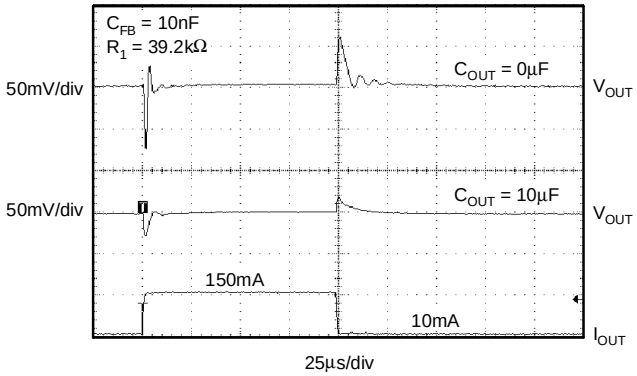



**Figure 29.**

**TPS73101**
**LINE TRANSIENT, ADJUSTABLE VERSION**

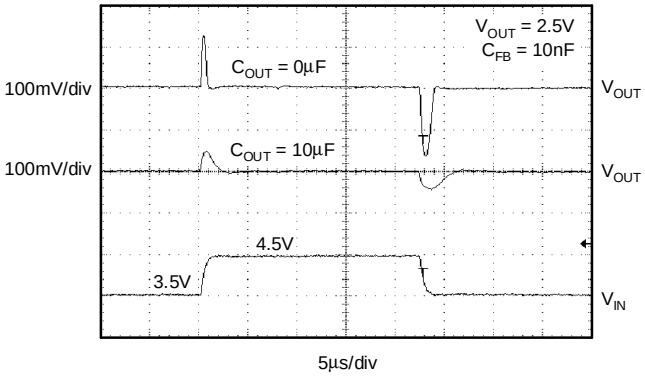



**Figure 30.**

## APPLICATION INFORMATION

The TPS731xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS731xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 31 shows the basic circuit connections for the fixed voltage models. Figure 32 gives the connections for the adjustable output version (TPS73101).

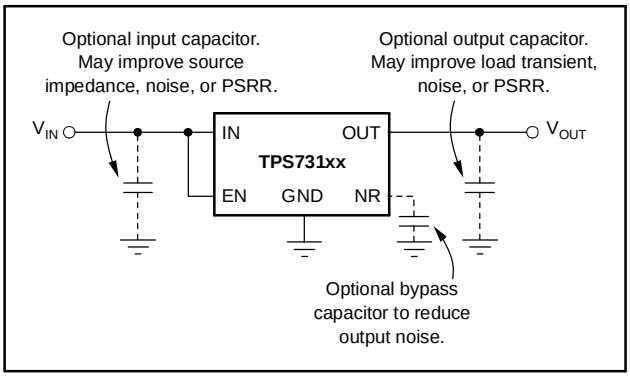



**Figure 31. Typical Application Circuit for Fixed-Voltage Versions**

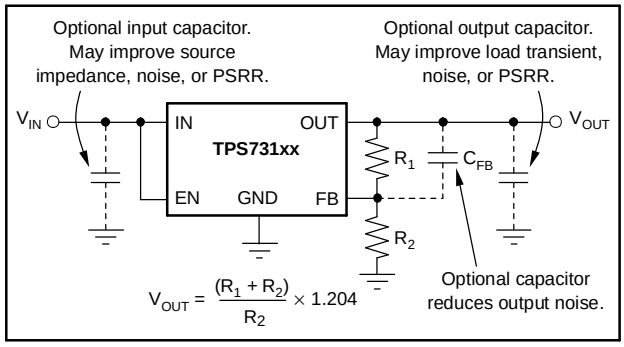



**Figure 32. Typical Application Circuit for Adjustable-Voltage Versions**

$R_1$ and $R_2$ can be calculated for any output voltage using the formula shown in Figure 32. Sample resistor values for common output voltages are shown in Figure 2. For best accuracy, make the parallel combination of $R_1$ and $R_2$ approximately 19kΩ.

### INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS731xx does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where $V_{IN}$ - $V_{OUT}$ < 0.5V and multiple low ESR capacitors are in parallel, ringing may occur when the product of $C_{OUT}$ and total ESR drops below 50nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

### OUTPUT NOISE

A precision band-gap reference is used to generate the internal reference voltage, $V_{REF}$. This reference is the dominant noise source within the TPS731xx and it generates approximately 32µVRMS (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of $V_{REF}$ is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no $C_{NR}$.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, $C_{NR}$, is connected from NR to ground. For $C_{NR}$ = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for $C_{NR}$ = 10nF.

This noise reduction effect is shown as *RMS Noise Voltage vs $C_{NR}$* in the Typical Characteristics section.

The TPS73101 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, $C_{FB}$, from the output to the FB pin will reduce output noise and improve load transient performance.

The TPS731xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above $V_{OUT}$. The charge pump generates ~250µV of switching noise at ~4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of $I_{OUT}$ and $C_{OUT}$.

## BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

## INTERNAL CURRENT LIMIT

The TPS731xx internal current limit helps protect the regulator during fault conditions. Foldback current helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when $V_{OUT}$ drops below 0.5V. See Figure 11 in the Typical Characteristics section for a graph of $I_{OUT}$ vs $V_{OUT}$.

## SHUTDOWN

The Enable pin is active high and is compatible with standard TTL-CMOS levels. $V_{EN}$ below 0.5V (max) turns the regulator off and drops the ground pin current to approximately 10nA. When shutdown capability is not required, the Enable pin can be connected to $V_{IN}$. When a pull-up resistor is used, and operation down to 1.8V is required, use pull-up resistor values below 50 kΩ.

## DROPOUT VOLTAGE

The TPS731xx uses an NMOS pass transistor to achieve extremely low dropout. When ($V_{IN}$ - $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS-ON}$ of the NMOS pass element.

For large step changes in load current, the TPS731xx requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN}$ - $V_{OUT}$ above this line insure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom ($V_{IN}$ to $V_{OUT}$ voltage drop). Under worst-case conditions [full-scale instantaneous load change with ($V_{IN}$ - $V_{OUT}$) close to dc dropout levels], the TPS731xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

## TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the output pin to ground will reduce undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, $C_{FB}$, from the output to the adjust pin will also improve the transient response.

The TPS731xx does not have active pull-down when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor $C_{OUT}$ and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega} \quad (4)$$

(Adjustable voltage version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2)} \quad (5)$$

## REVERSE CURRENT

The NMOS pass element of the TPS731xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see Figure 1 and Figure 2).

For the TPS73101, reverse current may flow when $V_{FB}$ is more than 1.0V above $V_{IN}$.

## THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS731xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS731xx into thermal shutdown will degrade device reliability.

## POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Power Dissipation Ratings table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element ($V_{IN}$ to $V_{OUT}$):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

### Package Mounting

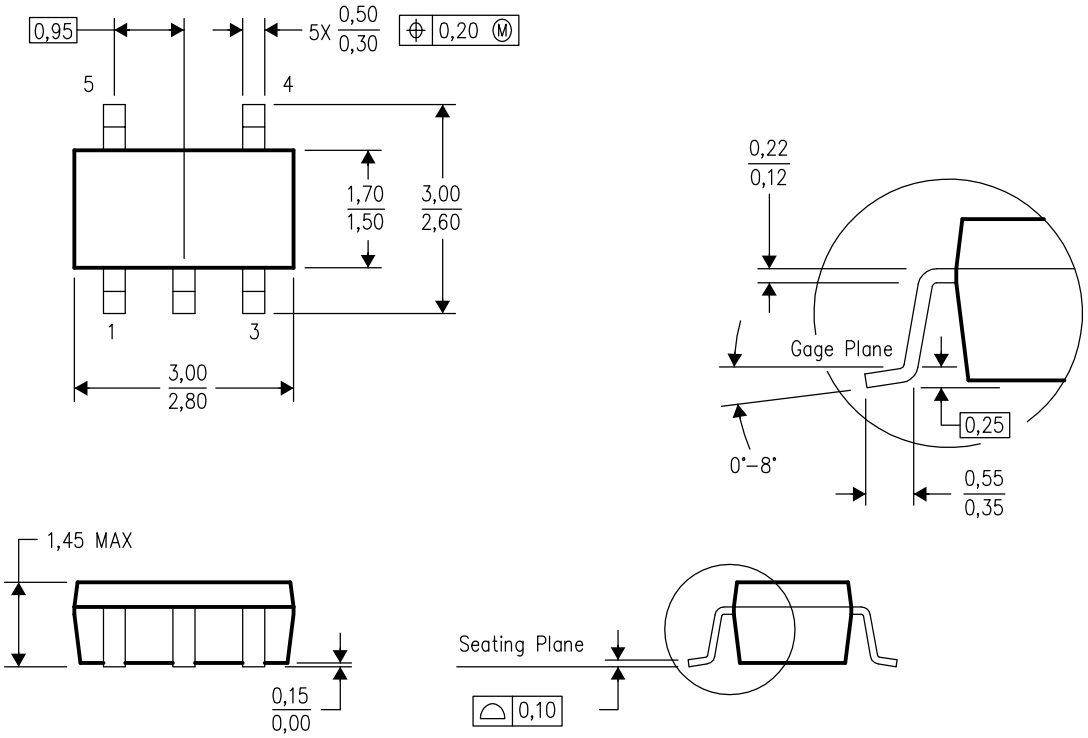
Solder pad footprint recommendations for the TPS731xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (AB-132), available from the Texas Instruments web site at www.ti.com.

## PACKAGING INFORMATION

| ORDERABLE DEVICE | STATUS(1) | PACKAGE TYPE | PACKAGE DRAWING | PINS | PACKAGE QTY |
|---|---|---|---|---|---|
| TPS73101DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73101DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73115DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73115DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73118DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73118DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73125DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73125DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73130DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73130DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73132DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73132DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73133DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73133DBVT | ACTIVE | SOP | DBV | 5 | 250 |
| TPS73150DBVR | ACTIVE | SOP | DBV | 5 | 3000 |
| TPS73150DBVT | ACTIVE | SOP | DBV | 5 | 250 |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

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