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# 2SK1772

Silicon N-Channel MOS FET

# HITACHI

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## Application

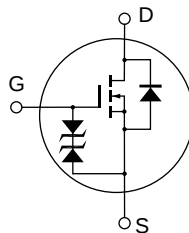
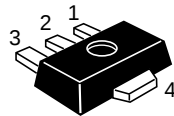
High speed power switching

## Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source.
- Suitable for DC-DC converter, motor drive, power switch, solenoid drive

## Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

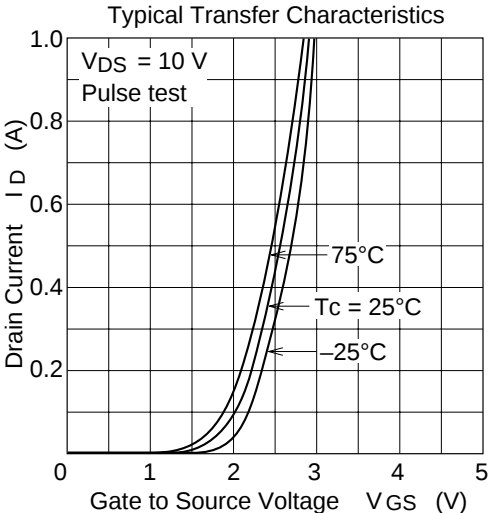
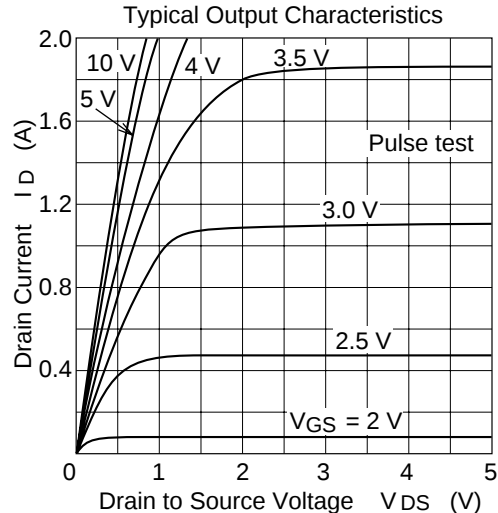
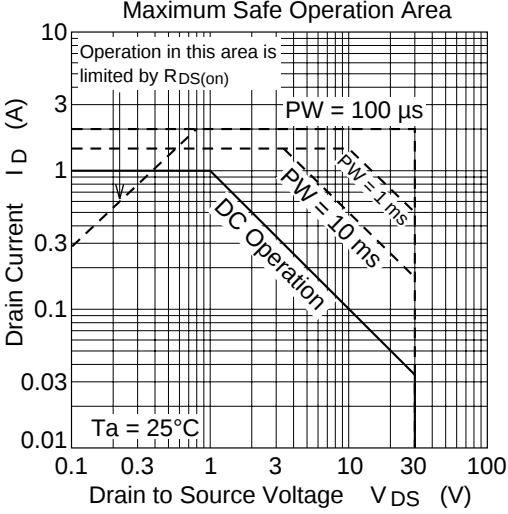
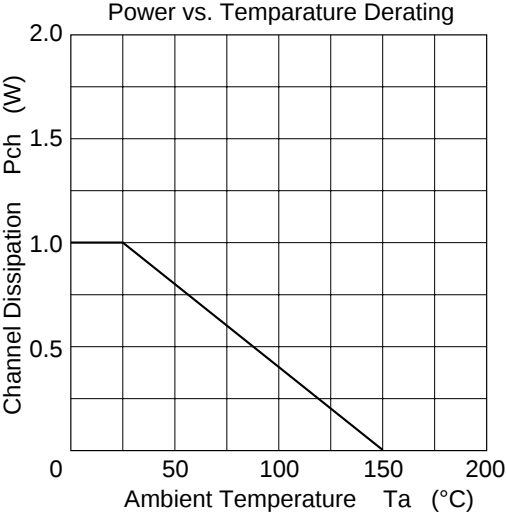
| Item                                      | Symbol                              | Ratings     | Unit |
|-------------------------------------------|-------------------------------------|-------------|------|
| Drain to source voltage                   | V <sub>DSS</sub>                    | 30          | V    |
| Gate to source voltage                    | V <sub>GSS</sub>                    | ±20         | V    |
| Drain current                             | I <sub>D</sub>                      | 1           | A    |
| Drain peak current                        | I <sub>D(pulse)</sub> <sup>*1</sup> | 2           | A    |
| Body to drain diode reverse drain current | I <sub>DR</sub>                     | 1           | A    |
| Channel dissipation                       | Pch <sup>*2</sup>                   | 1           | W    |
| Channel temperature                       | Tch                                 | 150         | °C   |
| Storage temperature                       | Tstg                                | −55 to +150 | °C   |

- Notes
- 1. PW ≤ 10 μs, duty cycle ≤ 1 %
  - 2. When using the alumina ceramic board (12.5 × 20 × 0.7mm)
  - 3. Marking is "HY".

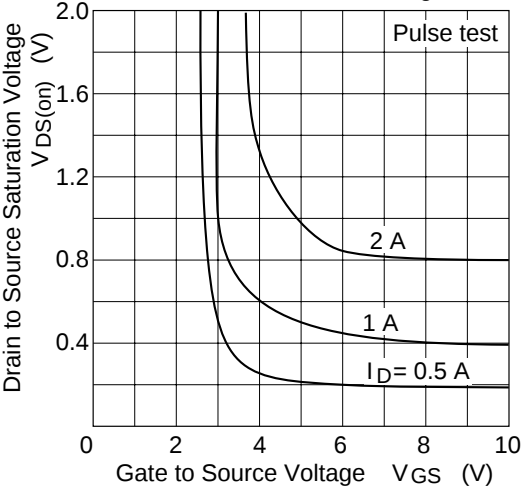
**Electrical Characteristics** (Ta = 25°C)

| Item                                       | Symbol        | Min      | Typ | Max      | Unit          | Test Conditions                                                              |
|--------------------------------------------|---------------|----------|-----|----------|---------------|------------------------------------------------------------------------------|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 30       | —   | —        | V             | $I_D = 10 \text{ mA}$ , $V_{GS} = 0$                                         |
| Gate to source breakdown voltage           | $V_{(BR)GSS}$ | $\pm 20$ | —   | —        | V             | $I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$                           |
| Gate to source leak current                | $I_{GSS}$     | —        | —   | $\pm 10$ | $\mu\text{A}$ | $V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$                                   |
| Zero gate voltage drain current            | $I_{DSS}$     | —        | —   | 50       | $\mu\text{A}$ | $V_{DS} = 25 \text{ V}$ , $V_{GS} = 0$                                       |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 1.0      | —   | 2.0      | V             | $I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$                               |
| Static drain to source on state resistance | $R_{DS(on)}$  | —        | 0.4 | 0.6      | $\Omega$      | $I_D = 0.5 \text{ A}$<br>$V_{GS} = 10 \text{ V}^{*1}$                        |
|                                            |               | —        | 0.6 | 0.85     | $\Omega$      | $I_D = 0.5 \text{ A}$<br>$V_{GS} = 4 \text{ V}^{*1}$                         |
| Forward transfer admittance                | $ y_{fs} $    | 0.6      | 1.0 | —        | S             | $I_D = 0.5 \text{ A}$<br>$V_{DS} = 10 \text{ V}^{*1}$                        |
| Input capacitance                          | $C_{iss}$     | —        | 85  | —        | pF            | $V_{DS} = 10 \text{ V}$                                                      |
| Output capacitance                         | $C_{oss}$     | —        | 65  | —        | pF            | $V_{GS} = 0$                                                                 |
| Reverse transfer capacitance               | $C_{rss}$     | —        | 20  | —        | pF            | $f = 1 \text{ MHz}$                                                          |
| Turn-on delay time                         | $t_{d(on)}$   | —        | 10  | —        | ns            | $I_D = 0.5 \text{ A}$                                                        |
| Rise time                                  | $t_r$         | —        | 15  | —        | ns            | $V_{GS} = 10 \text{ V}$                                                      |
| Turn-off delay time                        | $t_{d(off)}$  | —        | 40  | —        | ns            | $R_L = 60 \text{ }\Omega$                                                    |
| Fall time                                  | $t_f$         | —        | 30  | —        | ns            |                                                                              |
| Body to drain diode forward voltage        | $V_{DF}$      | —        | 1.2 | —        | V             | $I_F = 1 \text{ A}$ , $V_{GS} = 0$                                           |
| Body to drain diode reverse recovery time  | $t_{rr}$      | —        | 30  | —        | ns            | $I_F = 1 \text{ A}$ , $V_{GS} = 0$ ,<br>$di_F/dt = 50 \text{ A}/\mu\text{s}$ |

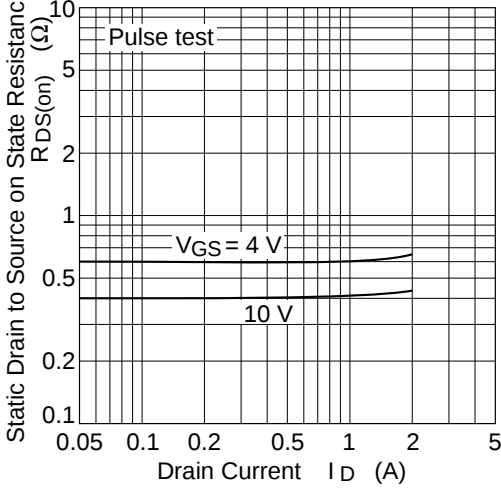
Note 1. Pulse Test



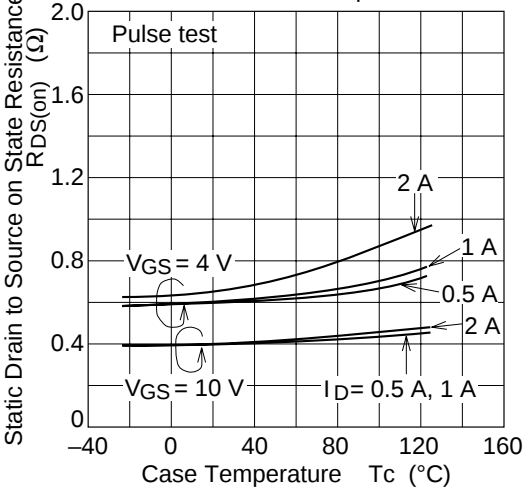
Drain to Source Saturation Voltage  
vs. Gate to Source Voltage



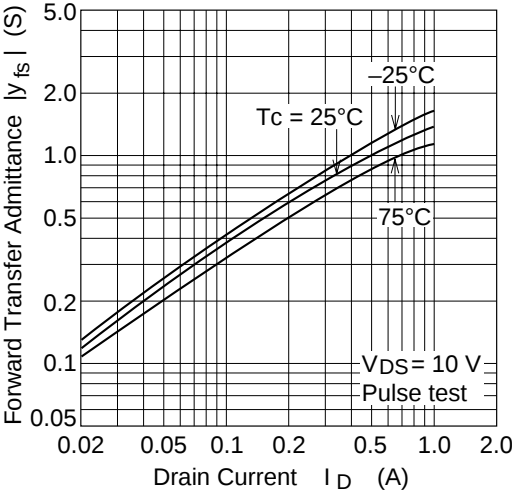
Static Drain to Source on State  
Resistance vs. Drain Current



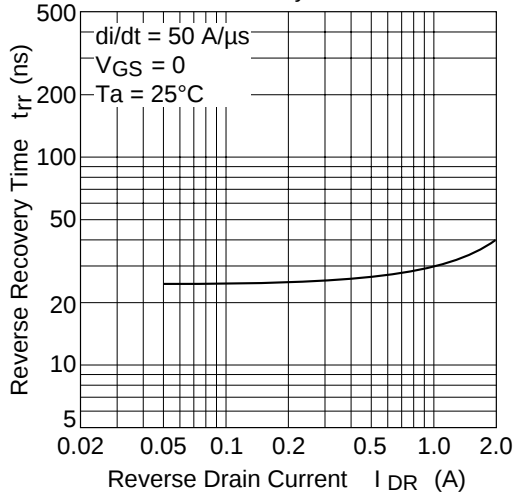
Static Drain to Source on State  
Resistance vs. Temperature



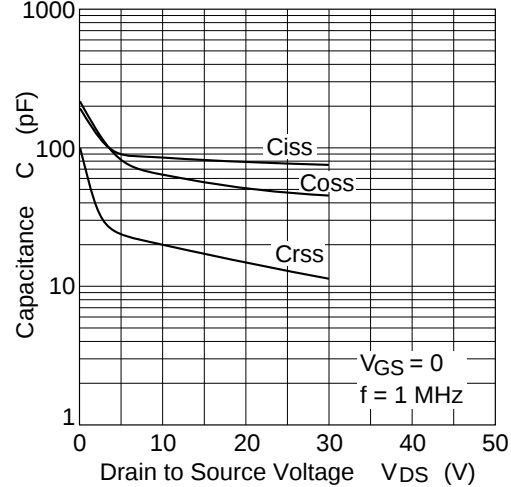
Forward Transfer Admittance vs.  
Drain Current



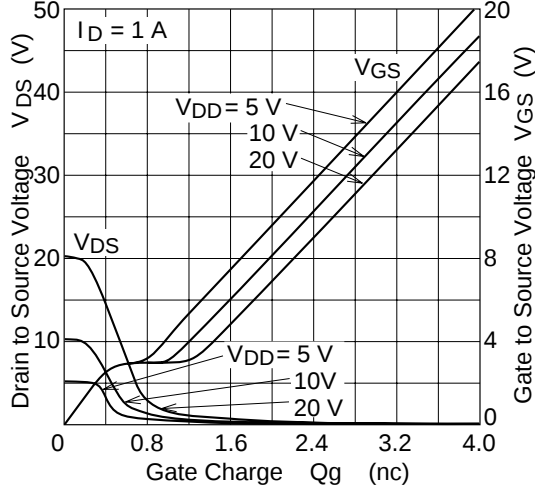
Body-Drain Diode Reverse Recovery Time



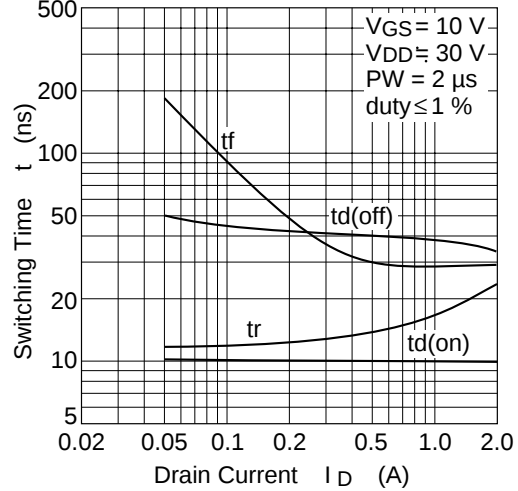
Typical Capacitance vs. Drain to Source Voltage

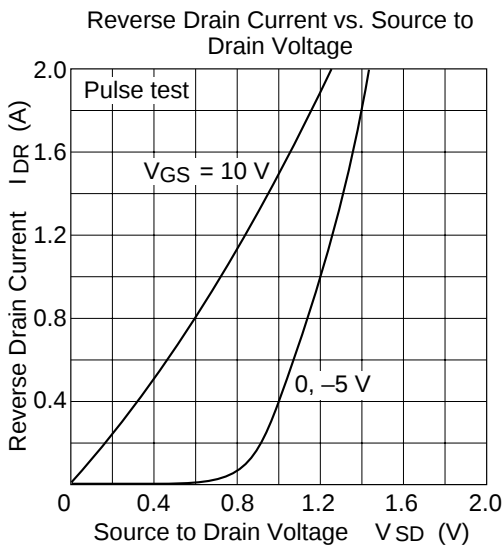


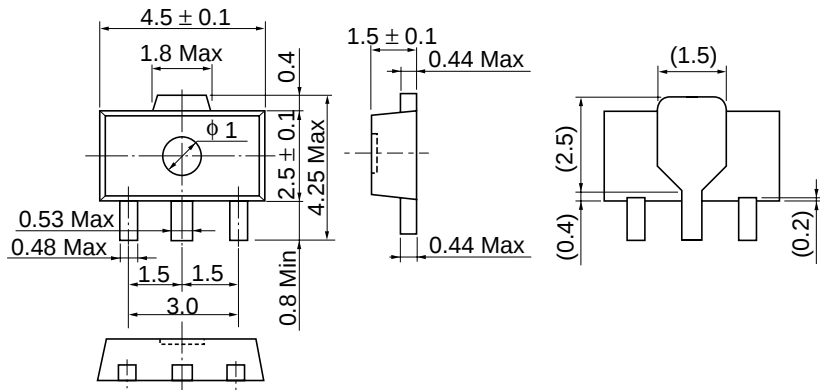
Dynamic Input Characteristics



Switching Characteristics







|                          |          |
|--------------------------|----------|
| Hitachi Code             | UPAK     |
| JEDEC                    | —        |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.050 g  |

## Cautions

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