

2SK3135(L),2SK3135(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

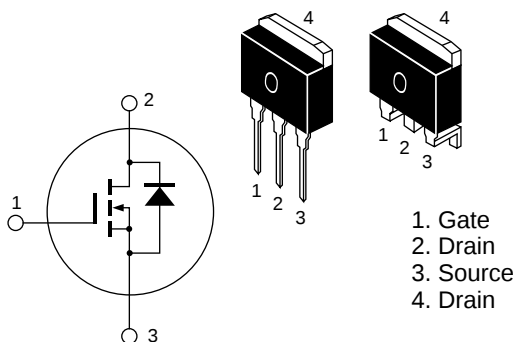
ADE-208-695B (Z)
3rd. Edition
February 1999

Features

- Low on-resistance
 $R_{DS(on)} = 6 \text{ m}\Omega$ typ.
- Low drive current
- 4 V gate drive device can be driven from 5 V source

Outline

LDBPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	75	A
Drain peak current	I _{D(pulse)} ^{Note 1}	300	A
Body-drain diode reverse drain current	I _{DR}	75	A
Avalanche current	I _{AP} ^{Note 3}	50	A
Avalanche energy	E _{AR} ^{Note 3}	214	mJ
Channel dissipation	P _{ch} ^{Note 2}	100	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

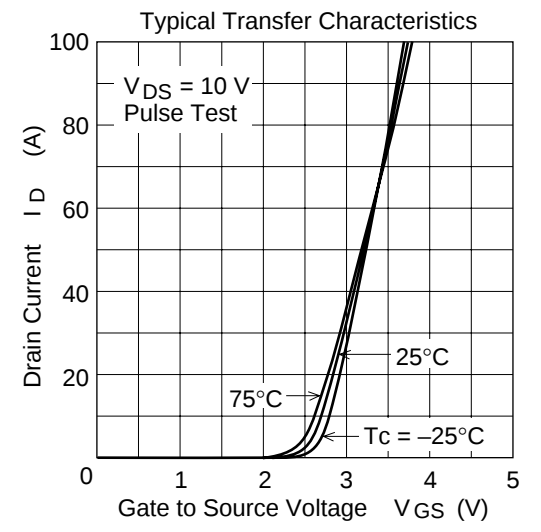
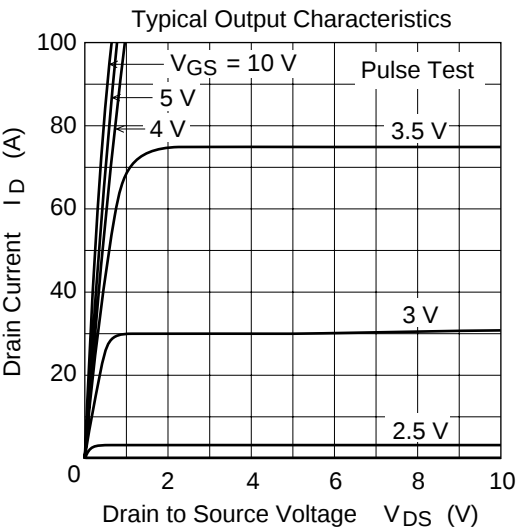
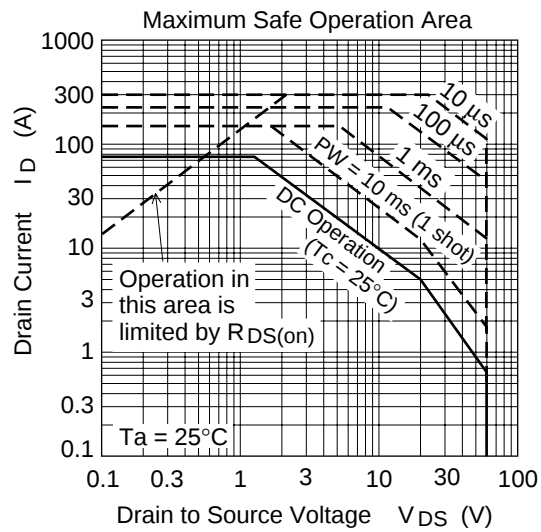
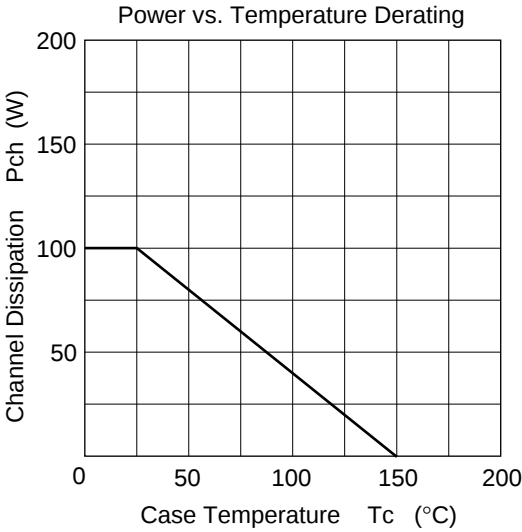
Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics (Ta = 25°C)

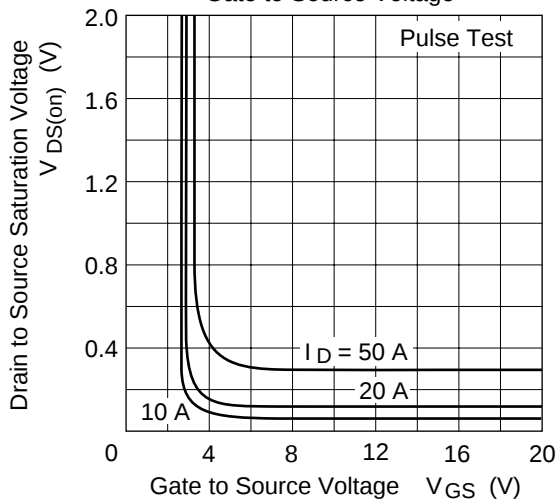
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1\text{ mA}$, $V_{DS} = 10\text{ V}$ Note 1
Static drain to source on state resistance	$R_{DS(on)}$	—	6.0	7.5	$\text{m}\Omega$	$I_D = 30\text{ A}$, $V_{GS} = 10\text{ V}$ Note 1
		—	8.0	12	$\text{m}\Omega$	$I_D = 30\text{ A}$, $V_{GS} = 4\text{ V}$ Note 1
Forward transfer admittance	$ y_{fs} $	50	80	—	S	$I_D = 30\text{ A}$, $V_{DS} = 10\text{ V}$ Note 1
Input capacitance	C_{iss}	—	7100	—	pF	$V_{DS} = 10\text{ V}$
Output capacitance	C_{oss}	—	1000	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	300	—	pF	$f = 1\text{ MHz}$
Total gate charge	Q_g	—	125	—	nc	$V_{DD} = 25\text{ V}$
Gate to source charge	Q_{gs}	—	25	—	nc	$V_{GS} = 10\text{ V}$
Gate to drain charge	Q_{gd}	—	25	—	nc	$I_D = 75\text{ A}$
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$
Rise time	t_r	—	300	—	ns	$R_L = 0.75\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	520	—	ns	
Fall time	t_f	—	330	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	$I_F = 75\text{ A}$, $V_{GS} = 0$
Body–drain diode reverse recovery time	t_{rr}	—	90	—	ns	$I_F = 75\text{ A}$, $V_{GS} = 0$ $di_F/dt = 50\text{ A}/\mu\text{s}$

Note: 1. Pulse test

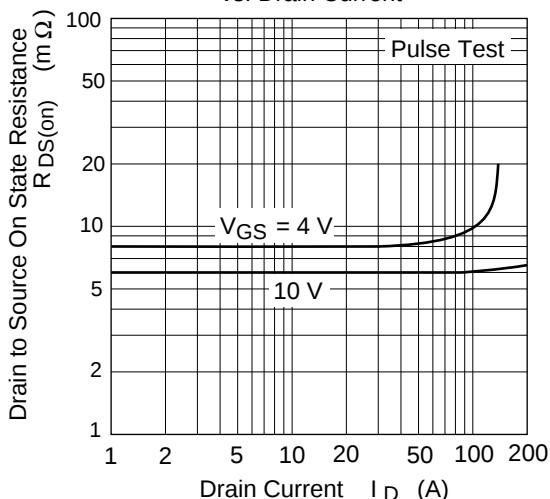
Main Characteristics



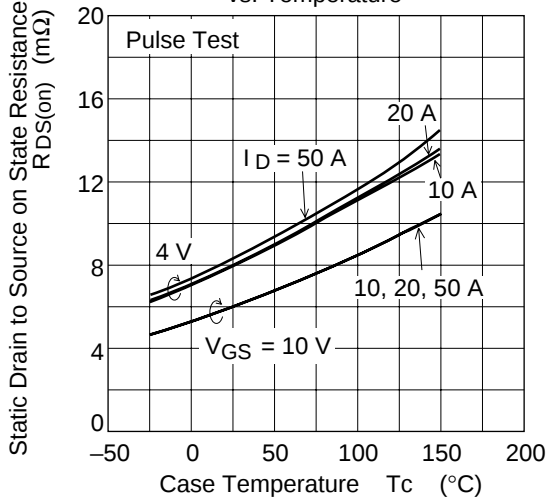
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



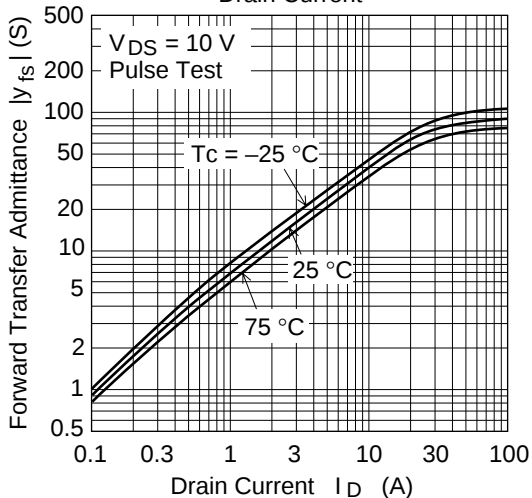
Static Drain to Source on State Resistance
vs. Drain Current

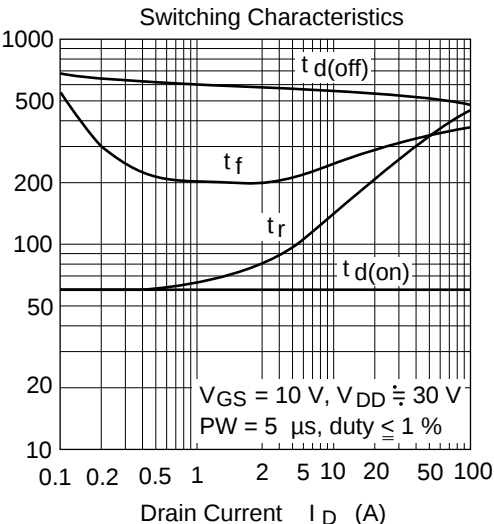
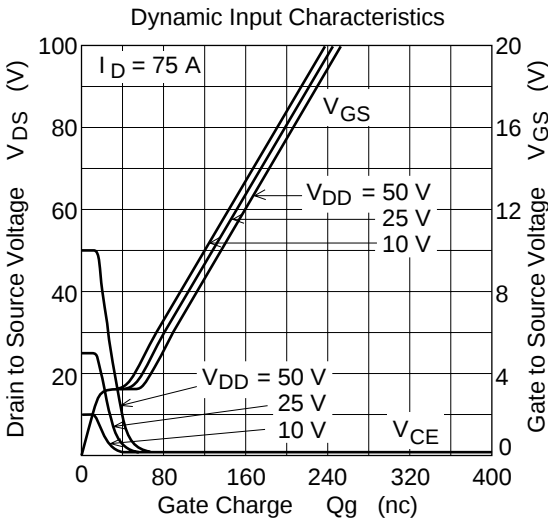
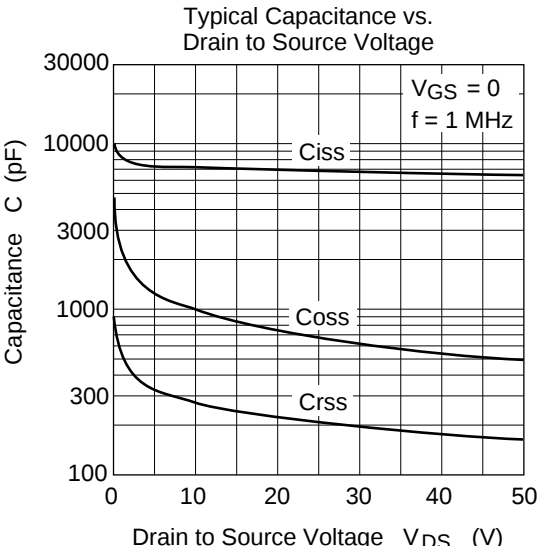
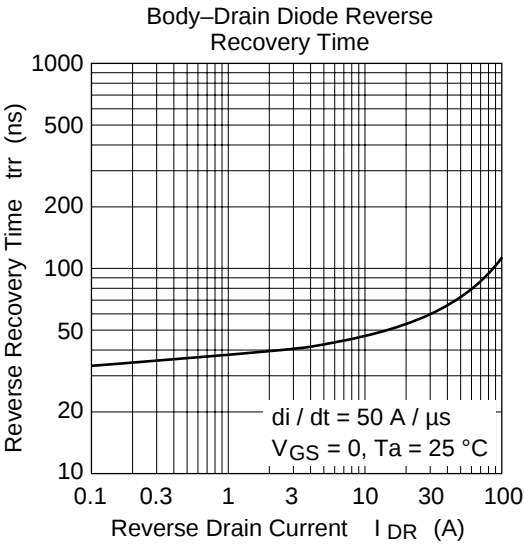


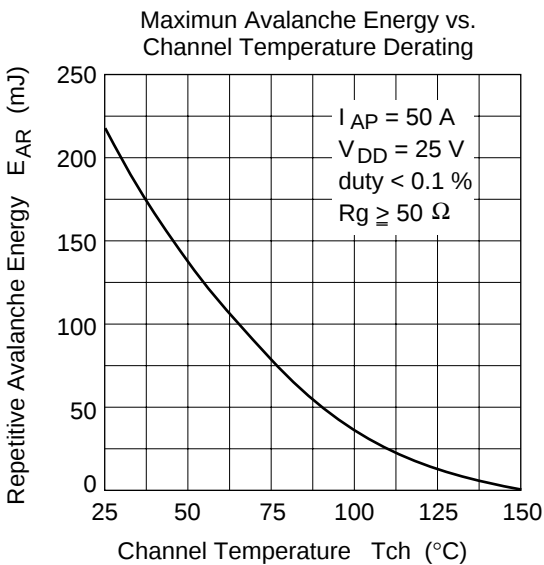
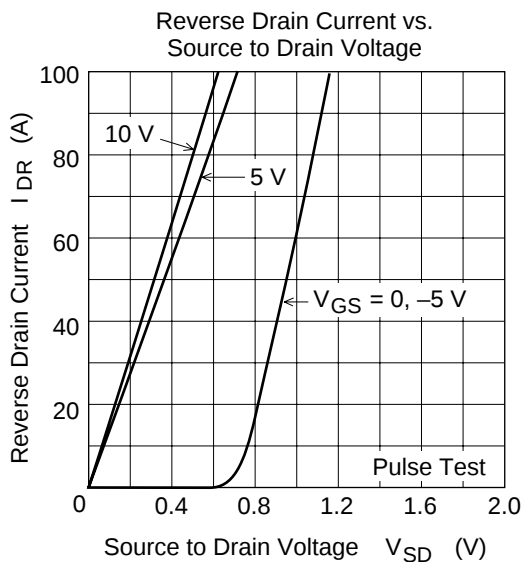
Static Drain to Source on State Resistance
vs. Temperature



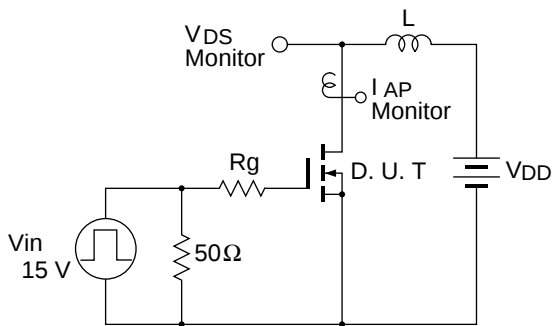
Forward Transfer Admittance vs.
Drain Current





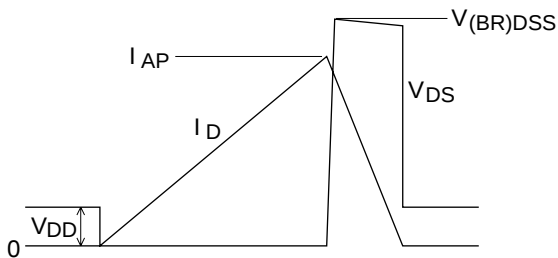


Avalanche Test Circuit

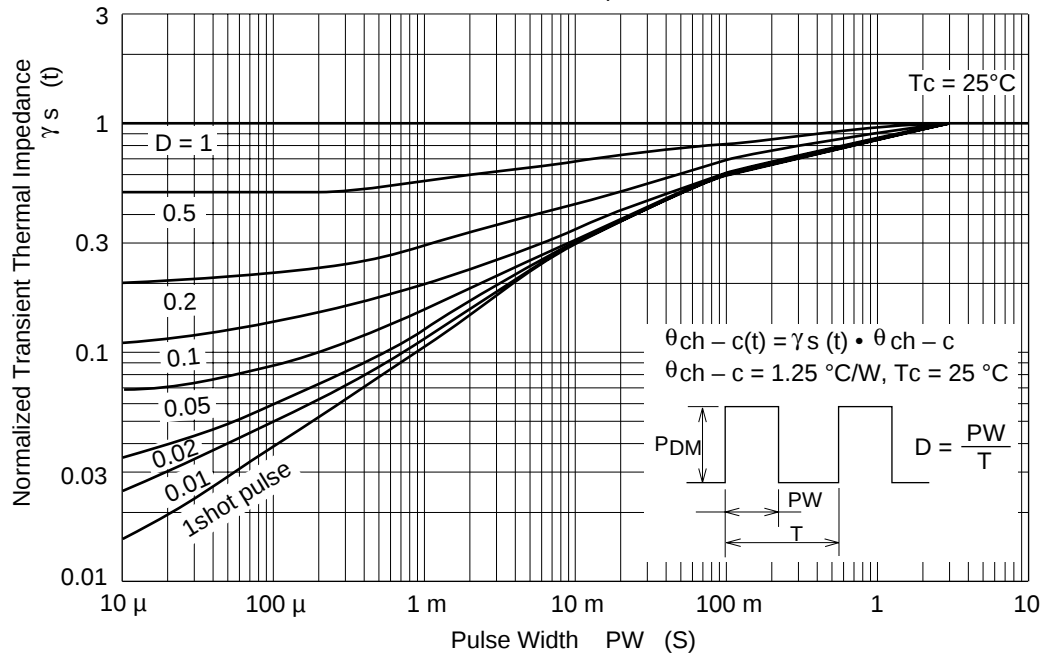


Avalanche Waveform

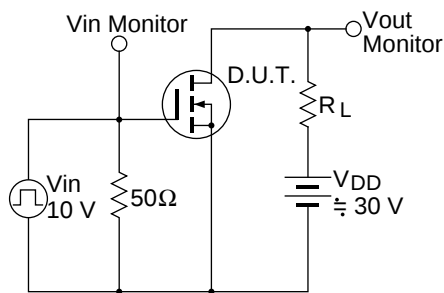
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



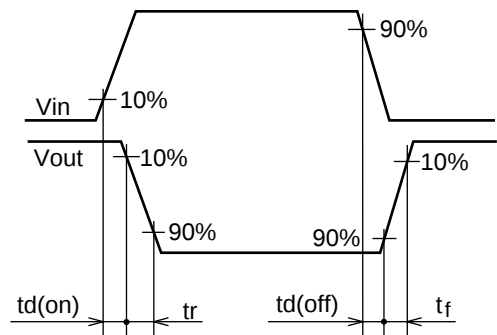
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

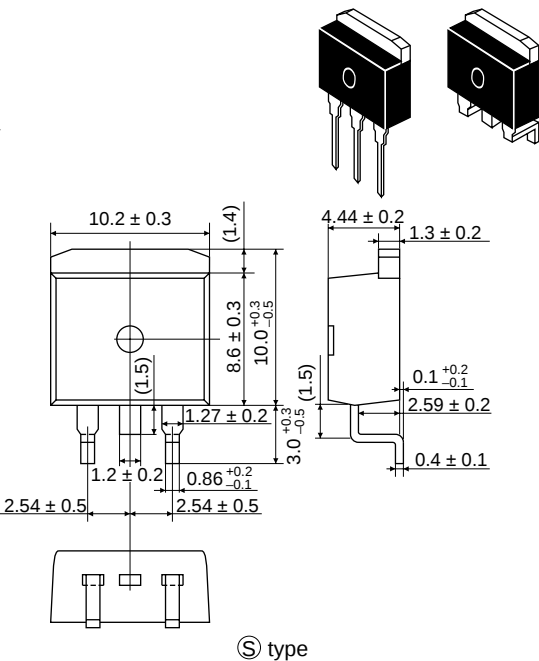
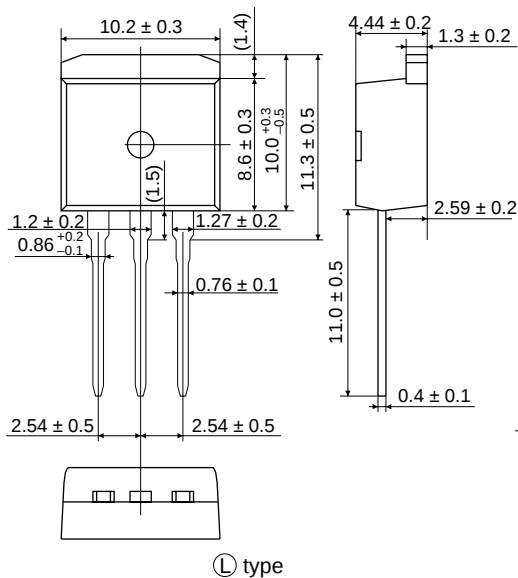


Waveform



Package Dimensions

Unit: mm



Hitachi Code	LDPAK
EIAJ	—
JEDEC	—

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