

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3507 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3507-ZK	TO-252 (MP-3ZK)

FEATURES

- 4.5 V drive available
- Low on-state resistance
 $R_{DS(on)1} = 45 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 11 \text{ A)}$
- Low gate charge
 $Q_G = 8.5 \text{ nC TYP. (} V_{DD} = 24 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 22 \text{ A)}$
- Built-in G-S protection diode
- Surface mount package available

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 16	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 22	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 45	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation ^{Note2}	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	10	A
Single Avalanche Energy ^{Note3}	E_{AS}	10	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on glass epoxy board of 1 inch x 1 inch x 1.6 mm

3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

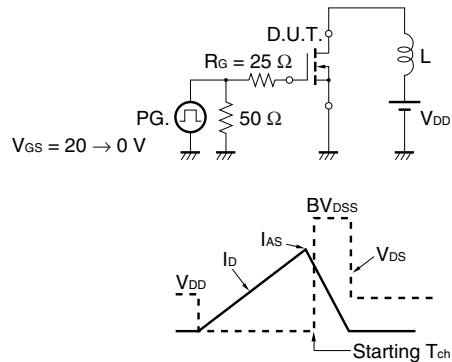
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

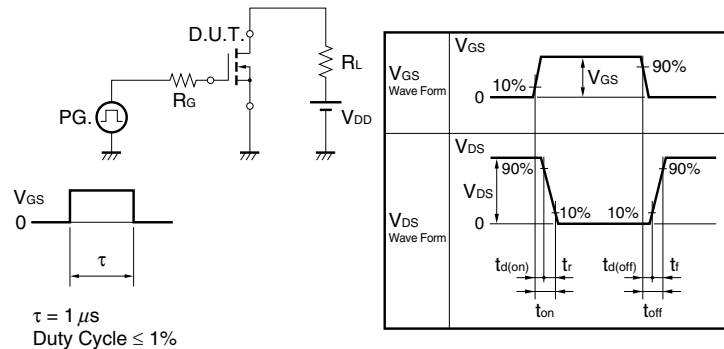
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 4.0 V, I _D = 11 A	6			S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 11 A		28	45	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 11 A		46	76	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		360		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		125		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		65		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 11 A		6.6		ns
Rise Time	t _r	V _{GS} = 10 V		3.6		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		16		ns
Fall Time	t _f			5.3		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		8.5		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		2		nC
Gate to Drain Charge	Q _{GD}	I _D = 22 A		2.1		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 22 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 22 A, V _{GS} = 0 V		31		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		26		nC

Note Pulsed

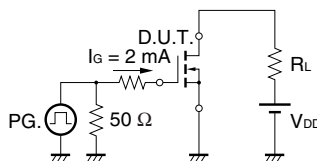
TEST CIRCUIT 1 AVALANCHE CAPABILITY



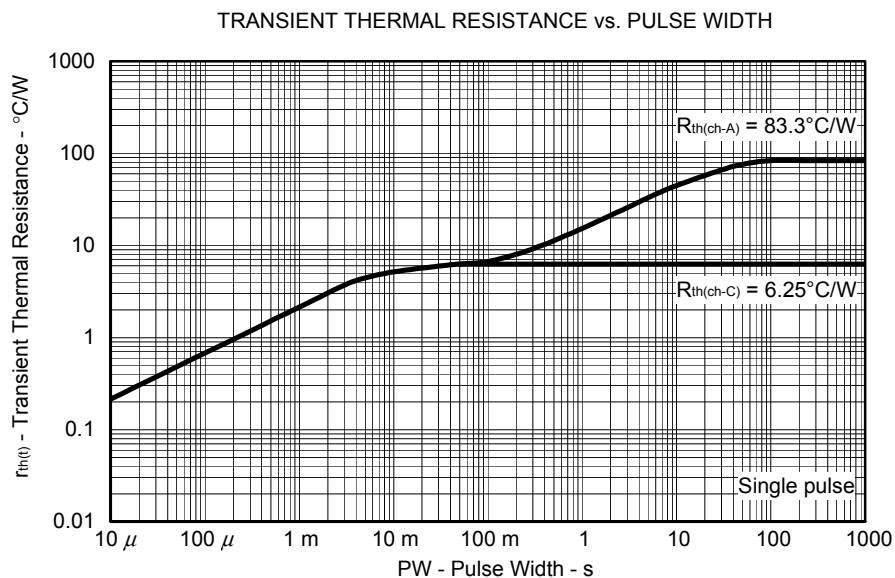
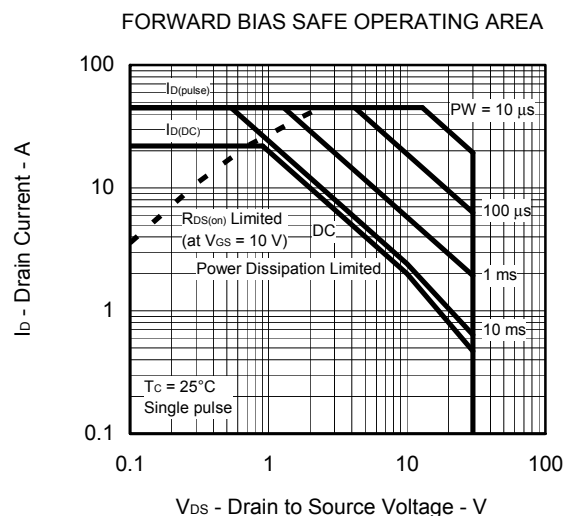
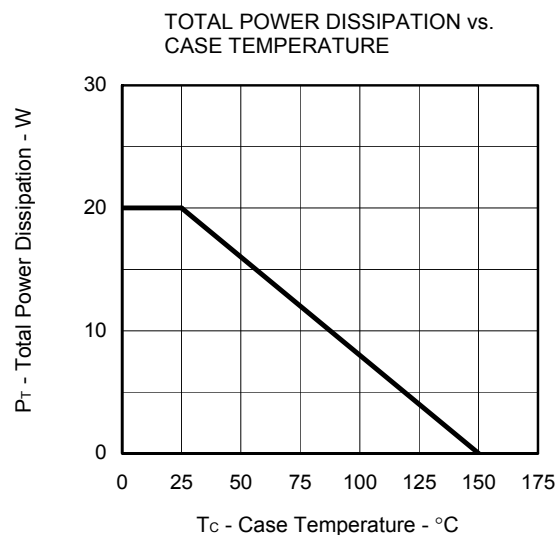
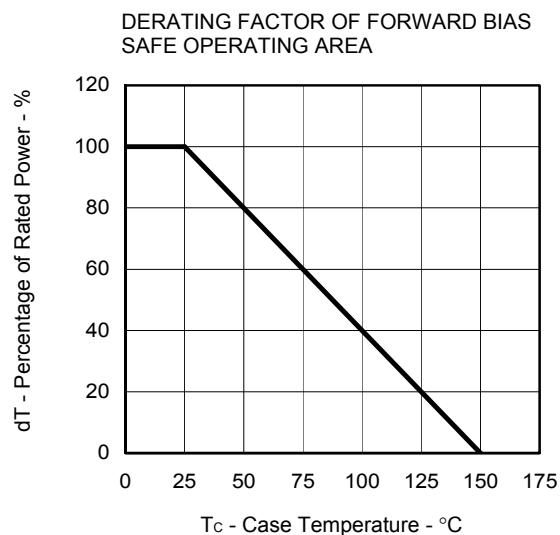
TEST CIRCUIT 2 SWITCHING TIME



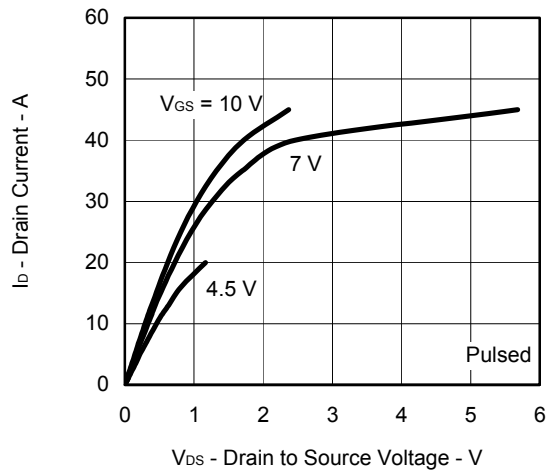
TEST CIRCUIT 3 GATE CHARGE



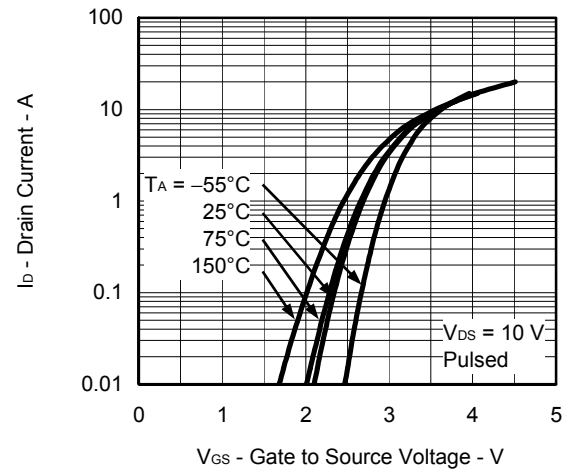
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



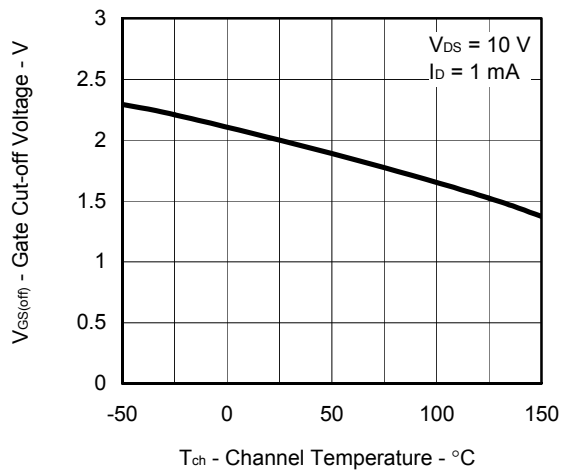
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



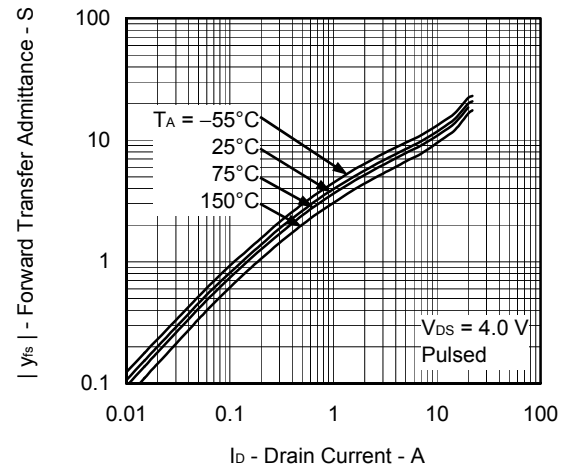
FORWARD TRANSFER CHARACTERISTICS



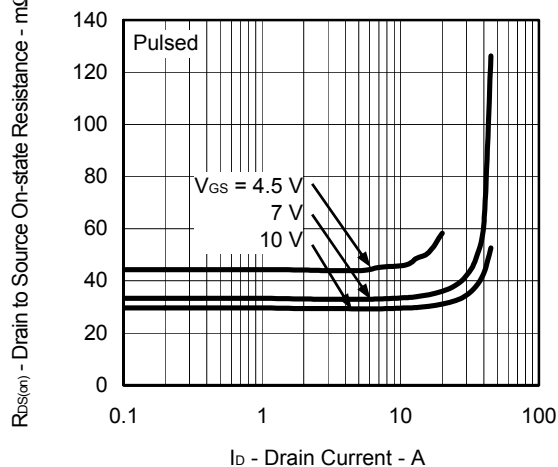
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



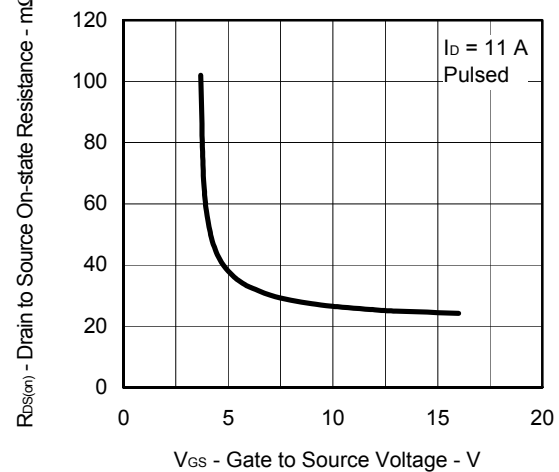
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



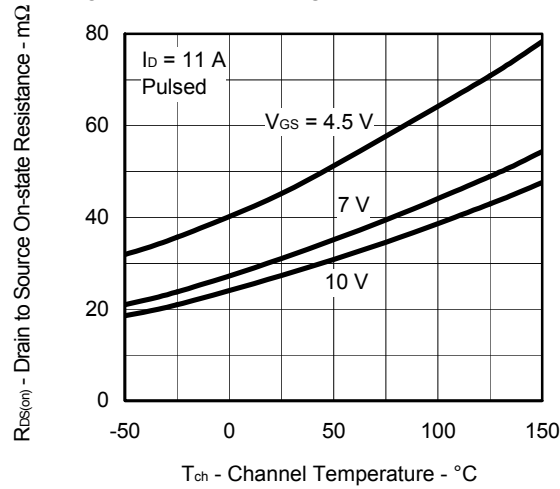
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



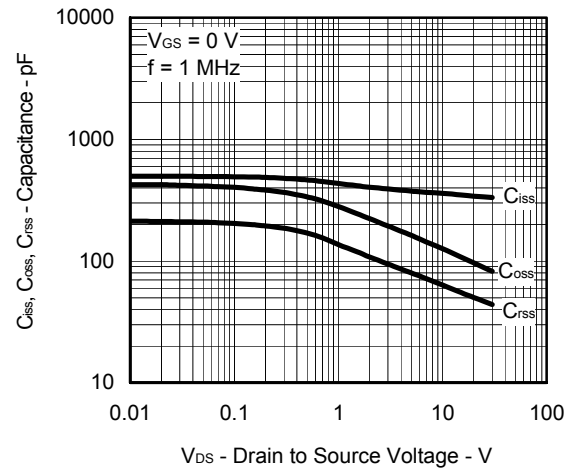
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



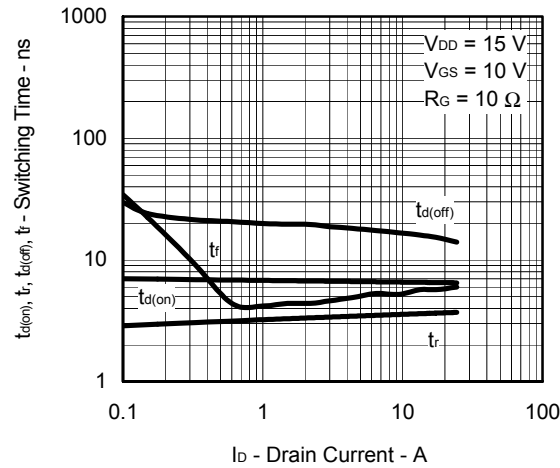
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



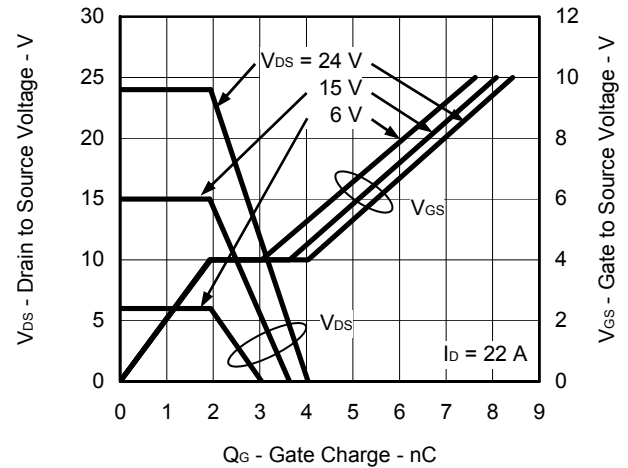
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



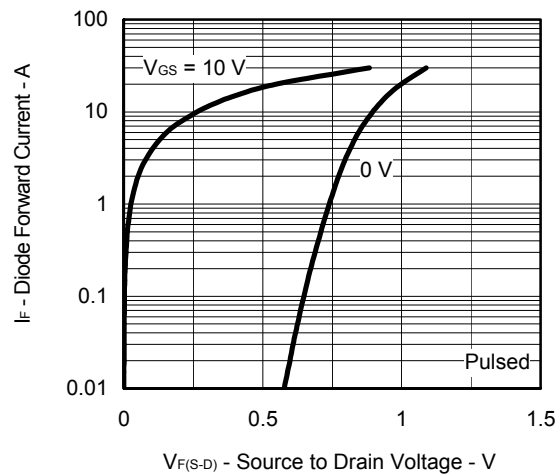
SWITCHING CHARACTERISTICS



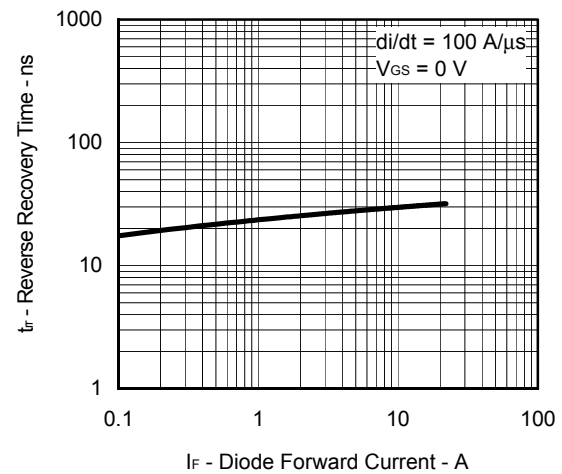
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

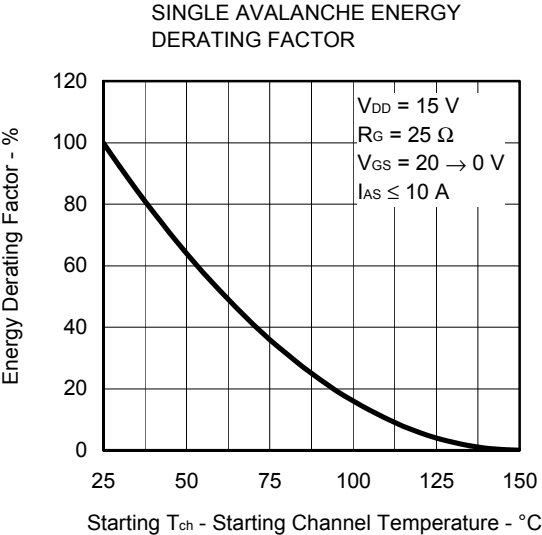
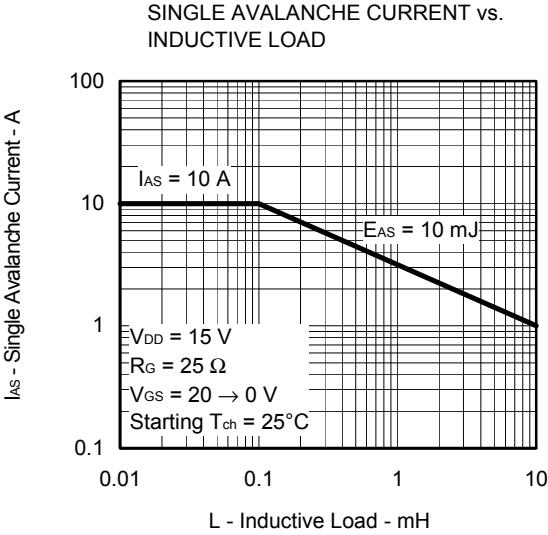


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



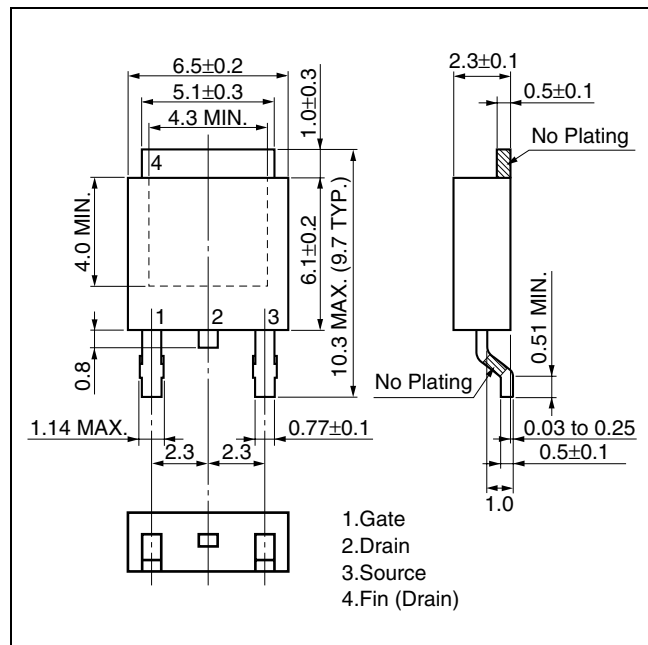
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



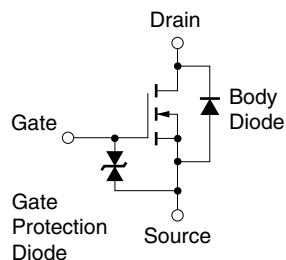


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Caution Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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