

MOS FIELD EFFECT TRANSISTOR 2SK3716

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3716 is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3716	TO-251 (MP-3)		
2SK3716-Z	TO-252 (MP-3Z)		

FEATURES

• Super low on-state resistance:

 $R_{DS(on)1} = 6.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, ID} = 30 \text{ A)}$

 $R_{DS(on)2} = 9.1 \text{ m}\Omega \text{ MAX.} \text{ (Vgs = 4.5 V, ID = 30 A)}$

- Low Ciss: Ciss = 2700 pF TYP.
- Built-in gate protection diode

(TO-251)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±60	Α
Drain Current (pulse) Note1	ID(pulse)	±240	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	84	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Repetitive Avalanche Current Note2	las	32	Α
Repetitive Avalanche Energy Note2	Eas	100	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. VDD = 20 V, RG = 25 Ω , VGS = 20 \rightarrow 0 V, Tch(peak) \leq 150°C

(TO-252)



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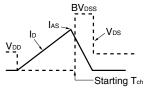


ELECTRICAL CHARACTERISTICS (TA = 25°C)

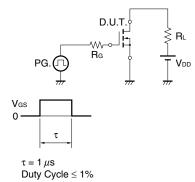
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			10	μА
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μА
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 30 A	22	43		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 30 A		5.2	6.5	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 30 A		6.6	9.1	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		2700		pF
Output Capacitance	Coss	V _{GS} = 0 V		770		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		290		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 30 A		11		ns
Rise Time	tr	V _{GS} = 10 V		13		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 0 \Omega$		69		ns
Fall Time	tf			14		ns
Total Gate Charge	QG	V _{DD} = 32 V		50		nC
Gate to Source Charge	Qgs	V _{GS} = 10 V		9		nC
Gate to Drain Charge	Q _{GD}	I _D = 60 A		13		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 60 A, V _{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	trr	I _F = 60 A, V _{GS} = 0 V		40		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		42		nC

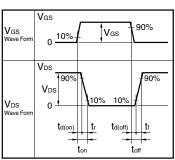
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME





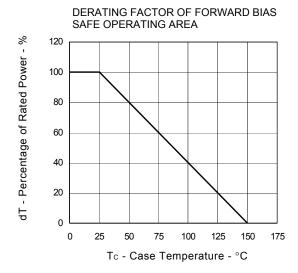
TEST CIRCUIT 3 GATE CHARGE

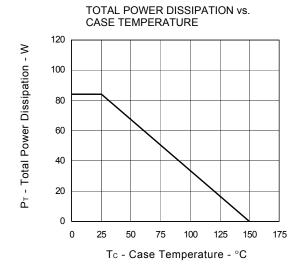
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline \end{array}$$

$$\begin{array}{c|c} PG. & \begin{array}{c} \\ \\ \end{array} & \begin{array}{c} \\ \end{array} & \begin{array}{c} \\ \\ \end{array} & \begin{array}{c$$

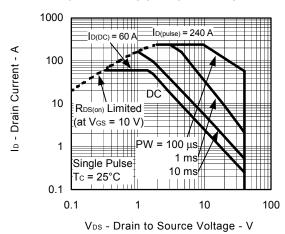


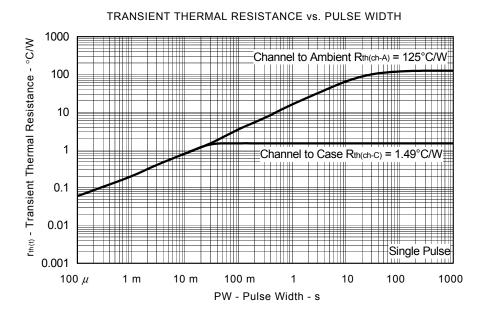
TYPICAL CHARACTERISTICS (TA = 25°C)





FORWARD BIAS SAFE OPERATING AREA



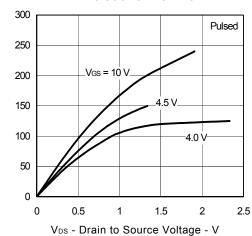


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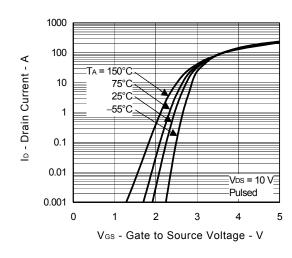


Ip - Drain Current - A

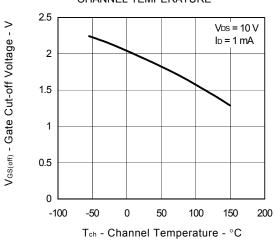
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



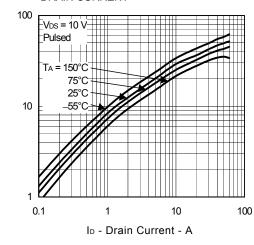
FORWARD TRANSFER CHARACTERISTICS



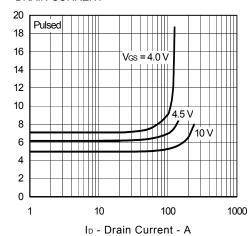
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



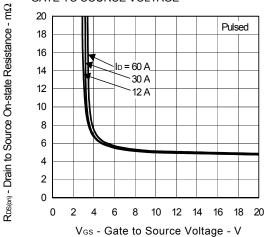
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



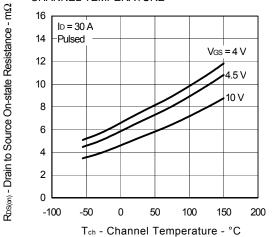
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



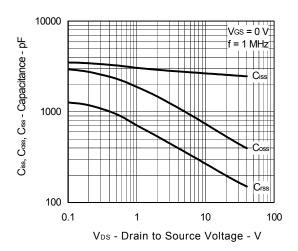
R_{DS(m)} - Drain to Source On-state Resistance - mΩ

y_{fs} | - Forward Transfer Admittance - S

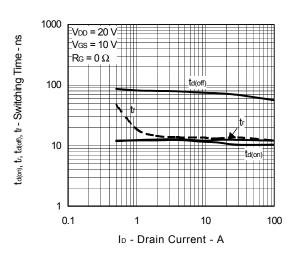
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



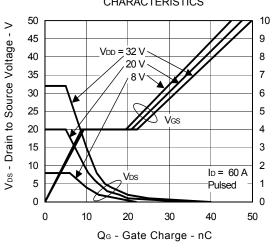
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



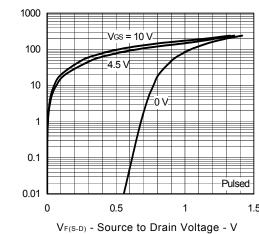
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

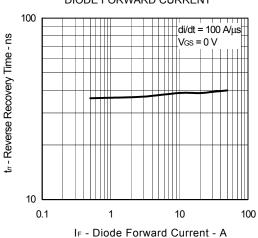


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



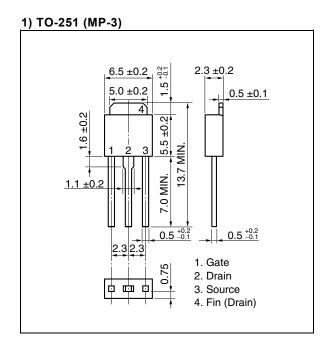
IF - Diode Forward Current - A

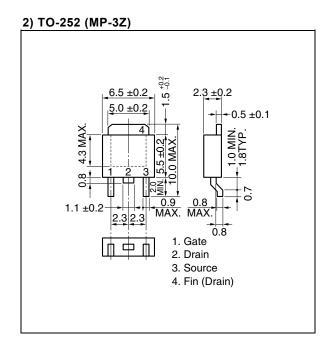
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



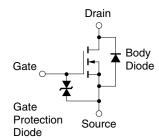


★ PACKAGE DRAWINGS (Unit: mm)





EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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