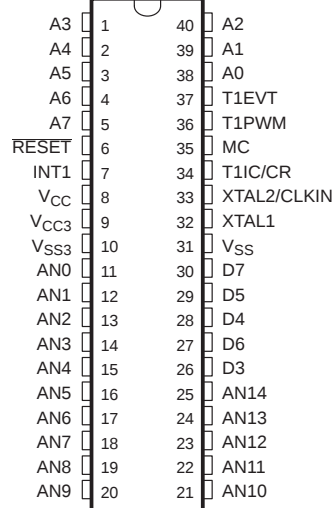


- FN AND FZ PACKAGES
(TOP VIEW)**
-
- Pinout details for FN and FZ packages (top view):
- Top Edge (Pins 1-16): A7, A6, A5, A4, A3, NC, A2, A1, A0, T1EVT, T1PWM, MC, T1IC/CR, XTAL2/CLKIN, NC, XTAL1.
 - Right Edge (Pins 39-48): VSS, D7, D5, D4, D6, D3, AN5, AN6, AN7, AN8, AN9, NC, AN10, AN11, AN12, AN13, AN14.
 - Bottom Edge (Pins 47-32): RESET, INT1, VCC, VCC3, VSS3, AN0, AN1, AN2, AN3, AN4, NC, 18, 19, 20, 21.
 - Left Edge (Pins 31-17): 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17.



- **CMOS/Package/TTL-Compatible I/O Pins**
 - 40- and 44-Pin Plastic and Ceramic Shrink Dual-In-Line and Leaded Chip Carrier Packages /16 Bidirectional; 9 Input Pins
 - All Peripheral Function Pins Are Software Configurable for Digital I/O
- **Workstation/PC-Based Software Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



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**TEXAS
INSTRUMENTS**

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TMS370Cx9x 8-BIT MICROCONTROLLER

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Pin Descriptions

PIN			I/O†	DESCRIPTION‡
NAME	SDIP (40)	LCC (44)		
A0 A1 A2 A3 A4 A5 A6 A7	38 39 40 01 02 03 04 05	42 43 44 02 03 04 05 06	I/O	Port A is a general-purpose bidirectional I/O port.
D3/SYSCLK D4 D5 D6 D7	26 28 29 27 30	29 31 32 30 33	I/O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
AN0/E0 AN1/E1 AN2/E2 AN3/E3 AN4/E4 AN5/E5 AN6/E6 AN7/E7	11 12 13 14 15 16 17 18	12 13 14 15 16 18 19 20	I	ADC3 analog input (AN0–AN7) or positive reference pins (AN6–AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC3 analog input. Only AN6 and AN7 can be software-configured as positive reference input.
AN8 AN9 AN10 AN11 AN12 AN13 AN14	19 20 21 22 23 24 25	21 22 24 25 26 27 28	I	ADC3 analog input pins
INT1	7	8	I	External (nonmaskable or maskable) interrupt/general-purpose input pin
T1IC/CR T1PWM T1EVT	34 36 37	38 40 41	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 PWM output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
RESET	6	7	I/O	System-reset bidirectional pin. RESET, as an input, initializes the microcontroller; as open-drain output, RESET indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC	35	39	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM V _{PP}
XTAL2/CLKIN XTAL1	33 32	37 35	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC}	8	9		Positive supply voltage for digital logic
V _{SS}	31	34		Ground reference for digital logic
V _{CC3}	9	10		Positive supply voltage for ADC3
V _{SS3}	10	11		Ground reference for ADC3
NC	—	1, 17, 23, 36		These pins have no connection to the internal die.

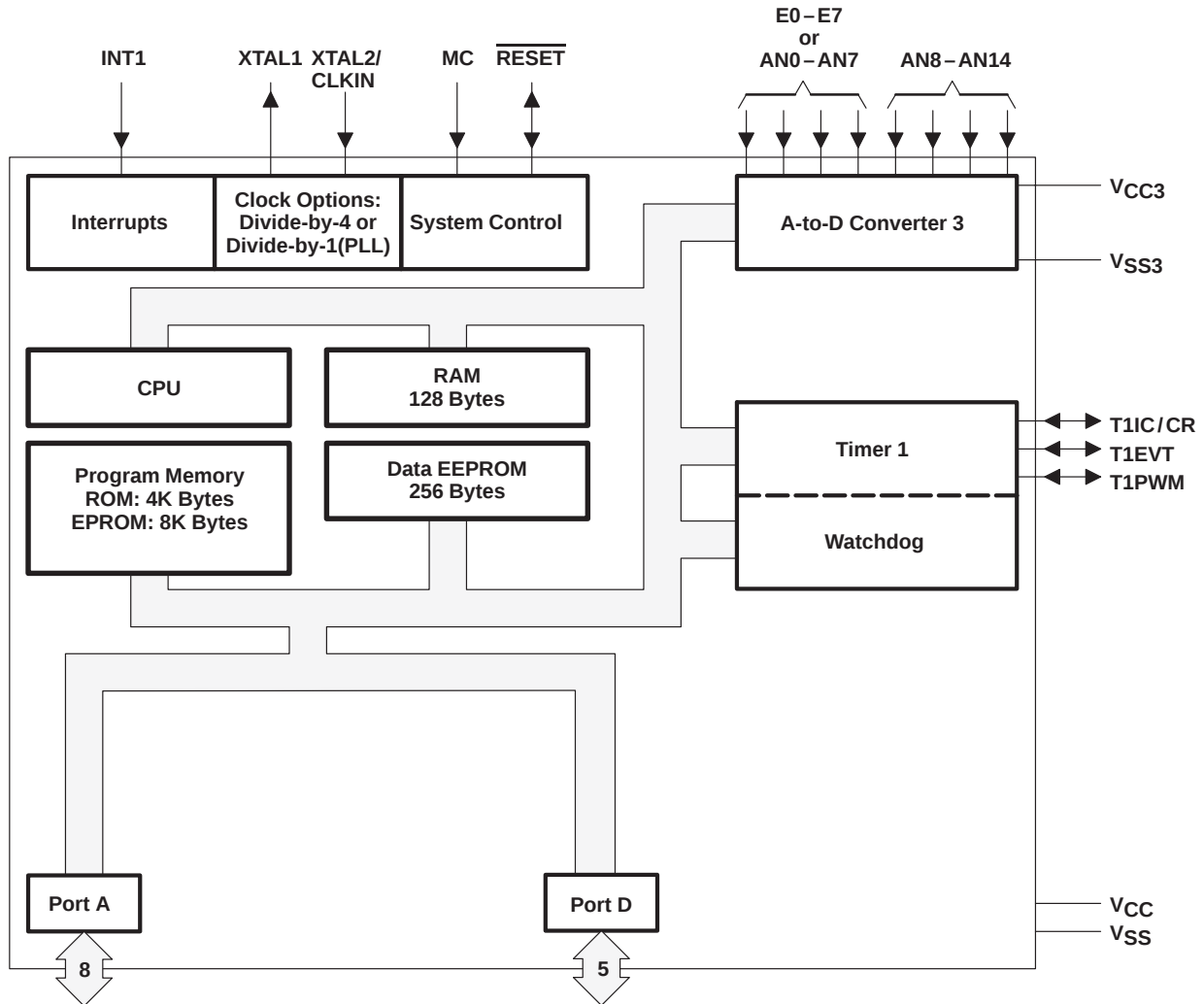
† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



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functional block diagram



description

The TMS370C090A, TMS370C792, and SE370C792 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx9x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx9x family is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx9x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application.

All TMS370Cx9x devices contain the following on-chip peripheral modules:

- Fifteen-channel, 8-bit analog-to-digital converter 3 (ADC3)
- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx9x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 44 PIN PLCC/CLCC, OR 40 PIN PSDIP/CSDIP
	ROM	EPROM	RAM	EEPROM	
TMS370C090A	4K	—	128	256	FN – PLCC / NJ [‡] – PSDIP
TMS370C792	—	8K	128	256	FN – PLCC / NJ [‡] – PSDIP
SE370C792 [†]	—	8K	128	256	FZ – CLCC / JC – CSDIP

[†] System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

[‡] The NJ designator for the 40-pin plastic shrink DIP package was formerly known as N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

The suffix letter A appended to the device names shown in the device column of Table 1 indicates the configuration of the device. ROM and EPROM devices have a different configuration as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [§]	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM without A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

[§] Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 4K bytes of mask-programmable ROM in the associated TMS370Cx9x device are replaced with 8K bytes of EPROM in the TMS370C792 while all other available memory and on-chip peripherals are identical. A one-time-programmable device (OTP) (TMS370C792) and a reprogrammable device (SE370C792) are available.

The TMS370C792 OTP device is available in a plastic package. This microcontroller is effective for use as an immediate production update for the TMS370Cx9x ROM device or for low-volume production runs when the mask charge or cycle time for the low-cost mask-ROM device is not practical.

The SE370C792 has a windowed ceramic package that allows reprogramming of the program EPROM memory during the development/prototyping design phase. The SE370C792 device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx9x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx9x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx9x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.



description (continued)

The TMS370Cx9x family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family compact development tool (CDT™) solves the challenge of efficiently developing the software and hardware required to design the TMS370Cx9x into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family CDT development tool can communicate through a standard RS-232-C interface with a personal computer. This allows the use of personal-computer editors and software utilities already familiar to the designer. The TMS370 family CDT emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370Cx9x family together with the TMS370 family CDT370 PACT, software tools, the SE370C792 reprogrammable device, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

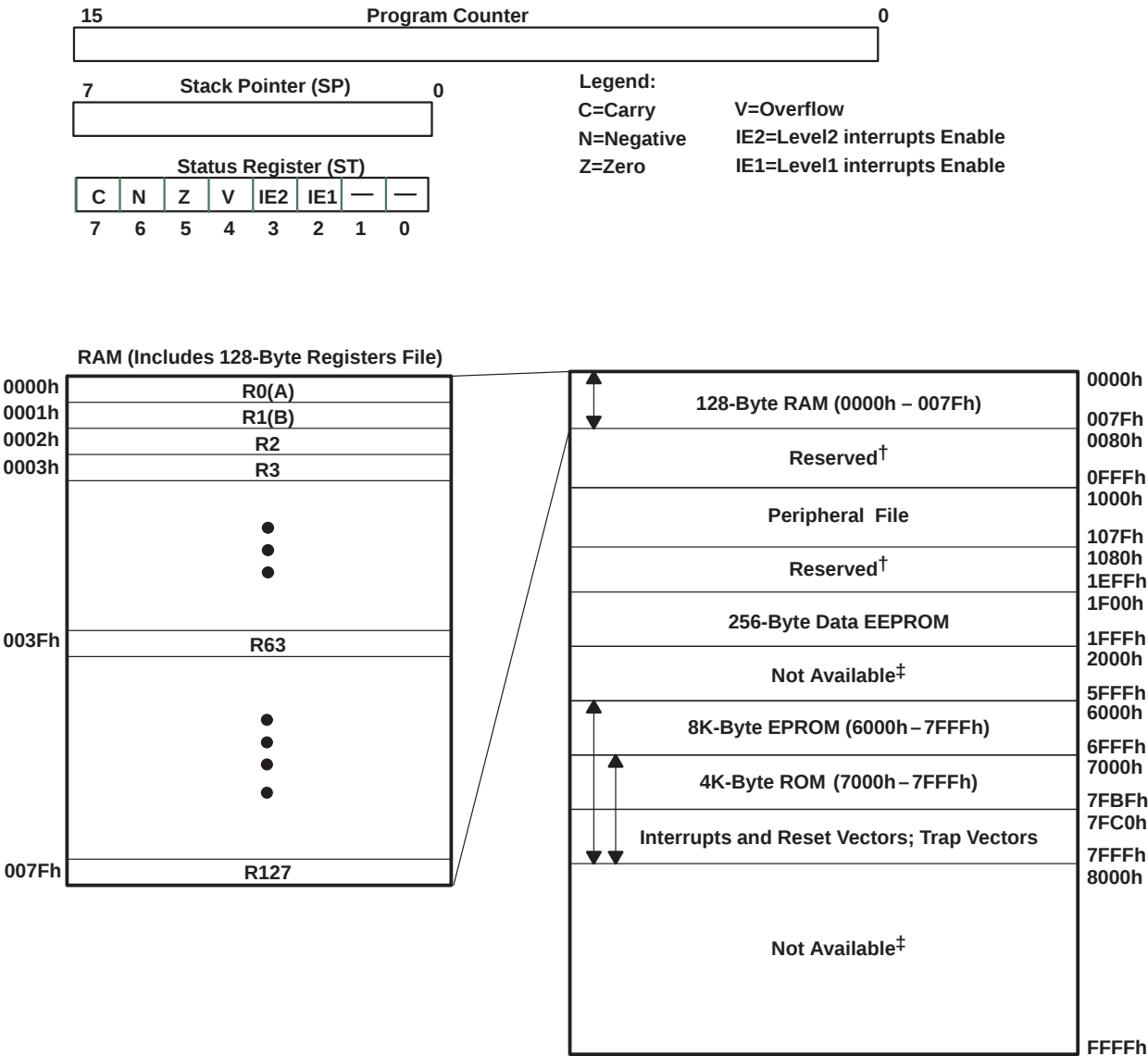
CPU

The CPU used on TMS370Cx9x devices is the high-performance 8-bit TMS370 CPU module. The 'x9x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x9x instruction set is summarized in Table 21. Figure 1 illustrates the CPU registers and memory blocks.

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CPU (continued)



† Reserved means that the address space is reserved for future expansion.

‡ Not available means that the address space is not accessible.

Figure 1. Programmer's Model

CPU (continued)

The 'x9x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes :
 - 128 bytes of general-purpose RAM that can be data memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 128 bytes)
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - A 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 4K bytes of ROM or 8K bytes of EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 128 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register and status bit notation are shown in Table 3.

Table 3. Status Register

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

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CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

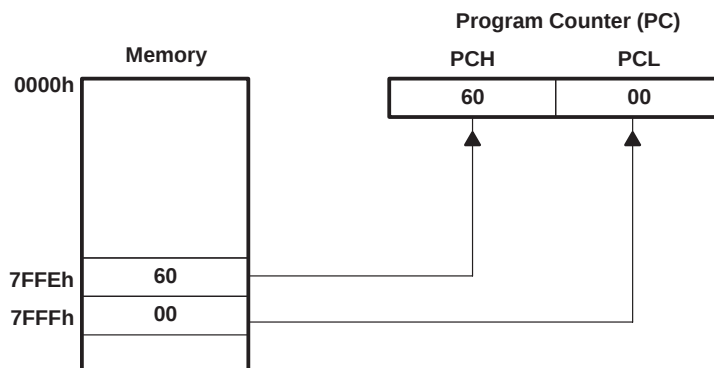


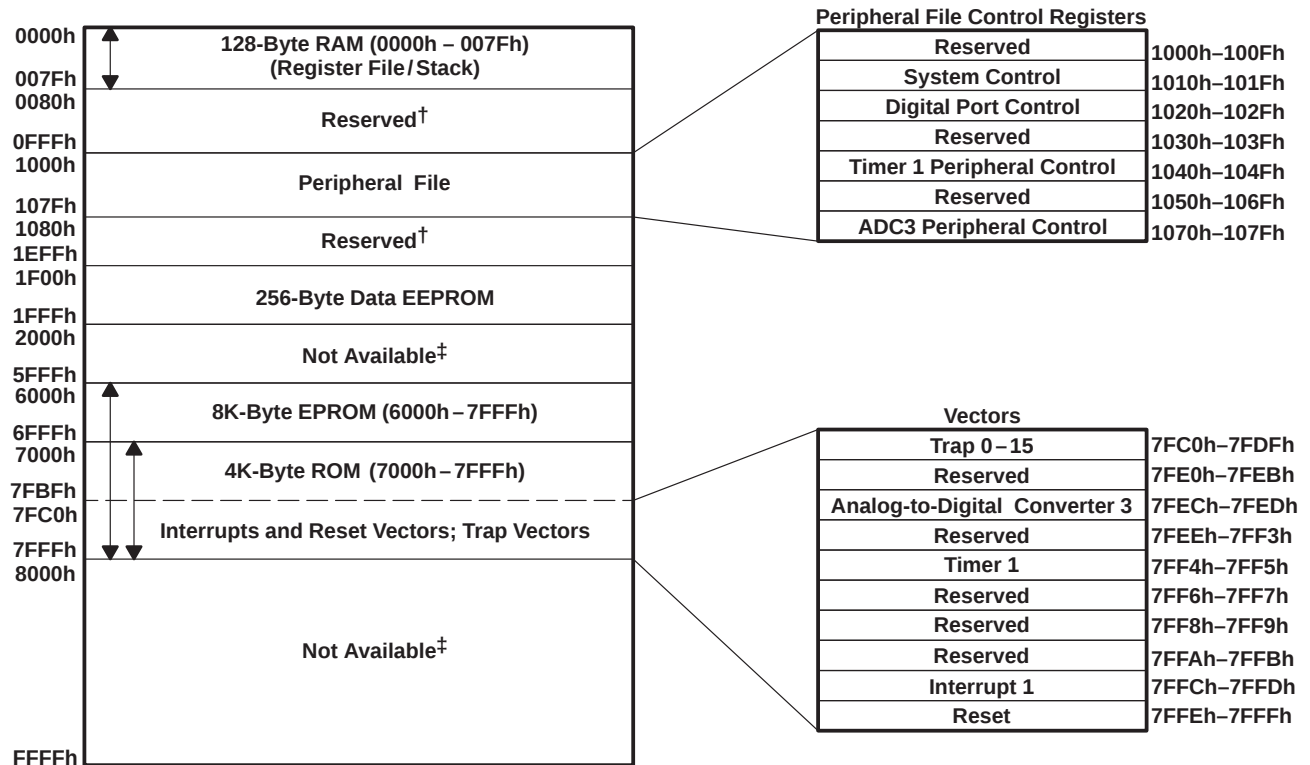
Figure 2. Program Counter After Reset

memory map

The TMS370Cx9x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx9x provides a memory-mapped RAM, ROM, data EEPROM, EPROM, input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 107Fh and logically divided into seven peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx9x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

CPU (continued)



† Reserved = the address space is reserved for future expansion.

‡ Not available = address space is unavailable in the mode illustrated.

Figure 3. TMS370Cx9x Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as the register file, general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx9x device contains 128 bytes of internal RAM mapped beginning at location 0000h (R0) and continuing through location 007Fh (R127) which is shown in Figure 3.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx9x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the peripheral file (PF) directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx9x peripheral files address map.

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peripheral file (PF) (continued)

Table 4. TMS370Cx9x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved
1010h–101Fh	P010–P01F	System and EEPROM/EPROM control registers
1020h–103Fh	P020–P03F	Digital I/O port control registers
1030h–103Fh	P030–P03F	Reserved
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–106Fh	P050–P06F	Reserved
1070h–107Fh	P070–P07F	Analog-to-digital converter 3 registers
1080h–10FFh	P080–P0FF	Reserved

data EEPROM

The TMS370Cx9x devices contain 256 bytes of data EEPROM and have a memory map beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127), or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit, byte, and block write/erase modes
 - Internal charge pump circuitry: No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
 - In-circuit programming capability: There is no need to remove the device to program.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
 - Reset: All programming of the data EEPROM module is halted.
 - Write protection active: there is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to the MC pin.

Table 5 shows the memory map of the control registers.

Table 5. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
101Ah (P01A)	DEECTL	Data EEPROM control register
101Bh (P01B)	—	Reserved
101Ch (P01C)	EPCTL	Program EPROM control register

program EPROM

The TMS370C792 contains 8K bytes of program EPROM memory mapped beginning at location 6000h and continuing through location 7FFFh as shown in Figure 3. Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™) and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the program EPROM control register (EPCTL). The program EPROM modules' features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to the MC pin
 - Control register: Program EPROM programming is controlled by the program EPROM control registers EPCTL located at the addresses in PF frame 1 as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program ROM consists of 4K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Memory addresses 7FE0h through 7FEBh are reserved for TI and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx9x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To assure a reset, the external signal should be held low for one SYSCLK cycle (it is possible, however, that a signal of less than one SYSCLK could cause a reset). See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x9x device to reset external system components. Additionally, if a cold start condition (V_{CC} is off for several hundred milliseconds), oscillator failure occurs, or $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 6 depicts the reset sources.

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system reset (continued)

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT NAME	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external-interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 4. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

interrupts (continued)

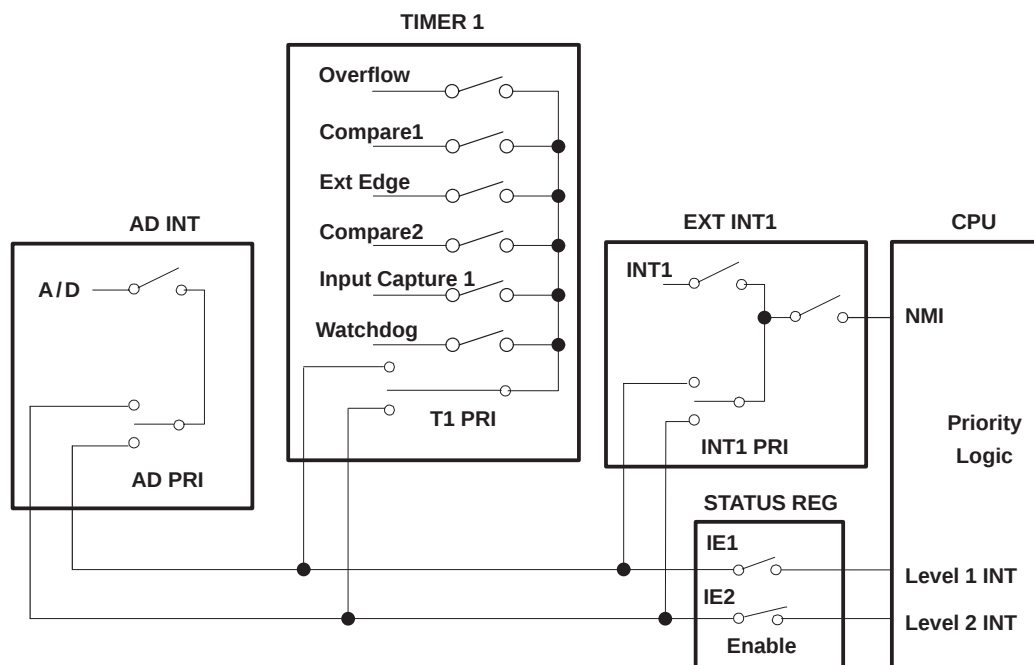


Figure 4. Interrupt Control

The TMS370Cx9x has three hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated PF. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Two of the system interrupts are generated by on-chip peripheral functions, and one external interrupt is supported. Software configuration of the external interrupt is performed through the INT1 control registers in peripheral file frame 1. The external is software-configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software-configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupt INT1 can be software-configured as a general-purpose input pin if the interrupt function is not required.

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interrupts (continued)

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External $\overline{\text{RESET}}$ Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}^{\ddagger}$	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	3
A/D conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	4

[†] Relative priority within an interrupt level.

[‡] Releases microcontroller from STANDBY and HALT low-power modes.

[§] Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx9x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx9x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to one to enter the nonprivileged mode; disabling write operations to specific configuration control bits within the peripheral file. Table 8 displays the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 8. Privilege Bits

REGISTER [¶]		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.6 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

[¶] The privilege bits are shown in a bold typeface in the system configuration registers section.

privileged operation and EEPROM write-protection override (continued)

The write-protect override (WPO) mode provides an external hardware method of overriding the write-protection registers of data EEPROM on the TMS370Cx9x. Applying a 12-V input to the MC pin after the $\overline{\text{RESET}}$ input goes high (logic 1) enters the WPO mode. The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of the data EEPROM while the device remains in the application, but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx9x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the idle instruction when the PWRDWN/IDLE bit in register SCCR2 has been set to one. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and timer 1 remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on INT1, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx9x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$ or an external interrupt on INT1) is detected. The low-power mode selection bits are summarized in Table 9.

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is always generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

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clock modules

The '370Cx9x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The '370C090A ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on the ROM device while the EPROM device '792 has only the divide-by-4 clock.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows:

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is that EMI is reduced. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 10 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded.

Table 10. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/ STANDBY	PWRDWN/ IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018 to P019	Reserved								
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 displays the specific addresses, registers, and control bits within this peripheral file frame.

Table 11. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 [†] (must be 0)					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0–7	Data out q	Data in y
D	3–7	Data out q	Data in y
a = Port x control register 1 b = Port x control register 2 c = Data d = Direction			

timer 1 module

The programmable timer 1 (T1) module of the TMS370Cx9x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent) or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 5.

timer 1 module (continued)

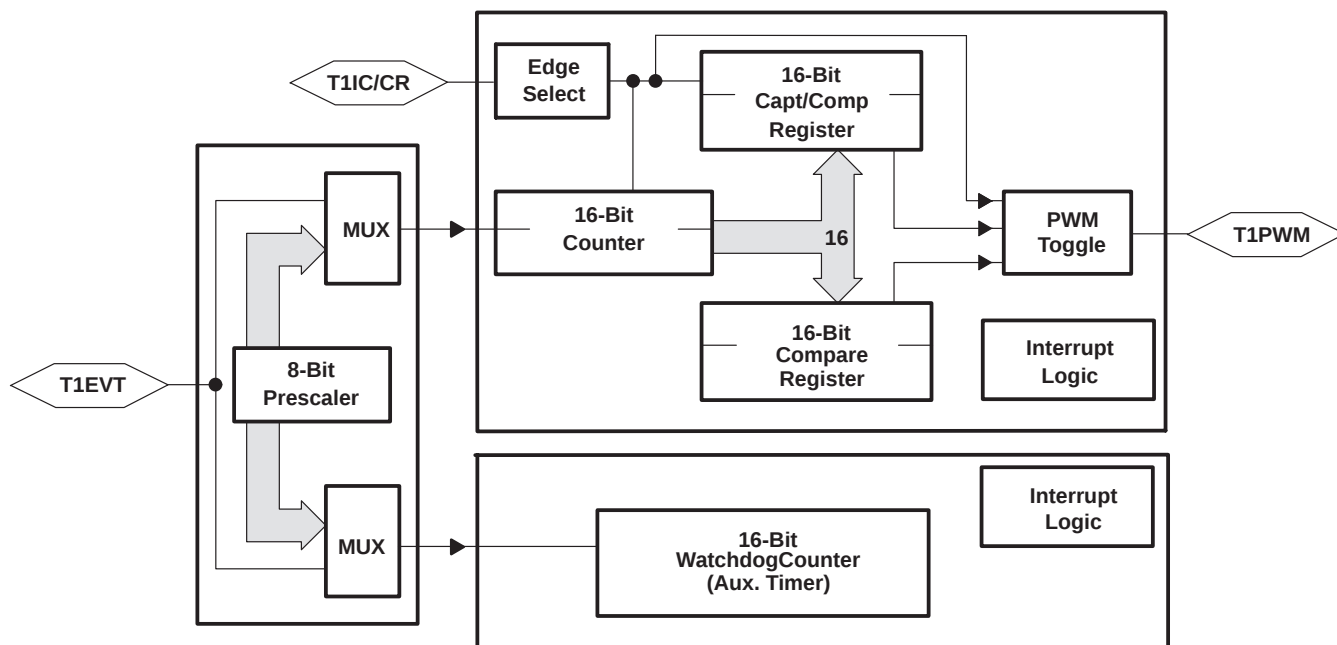


Figure 5. Timer 1 Block Diagram

- Three T1 I/O pins:
 - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal.
 - Capture/compare mode: Provides input capture pin.
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare registers.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determines one of eight clock sources for general-purpose timer
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR).

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timer 1 module (continued)

- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers: Located in the PF frame beginning at address P040.

Table 13 lists the T1 module control registers.

Table 13. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Capture/Compare and Dual-Compare									
P040	Bit 15			T1 Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 7			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.



timer 1 module (continued)

The T1 capture/compare mode block diagram is illustrated in Figure 6. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

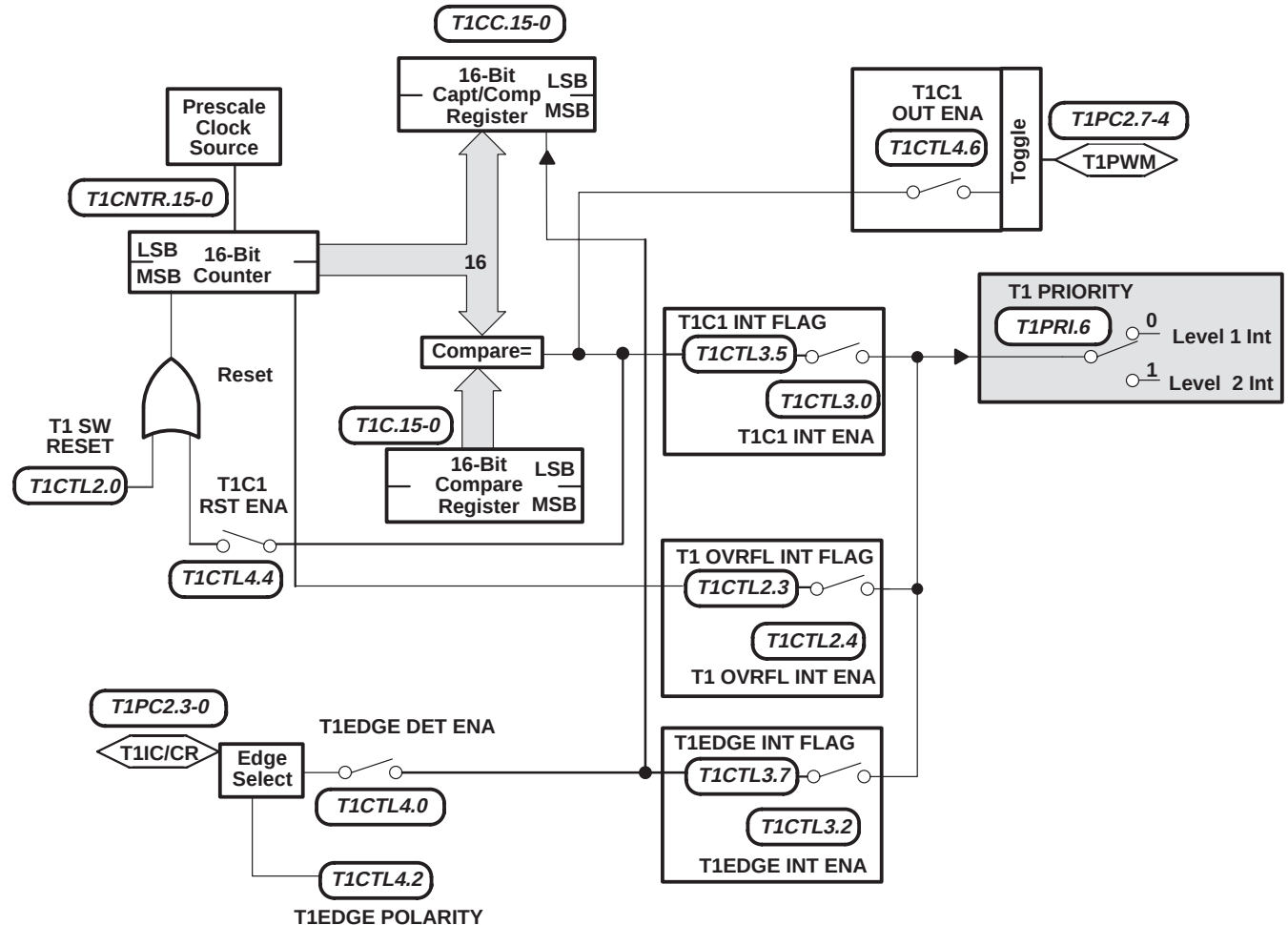


Figure 6. Capture/Compare Mode

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timer 1 module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

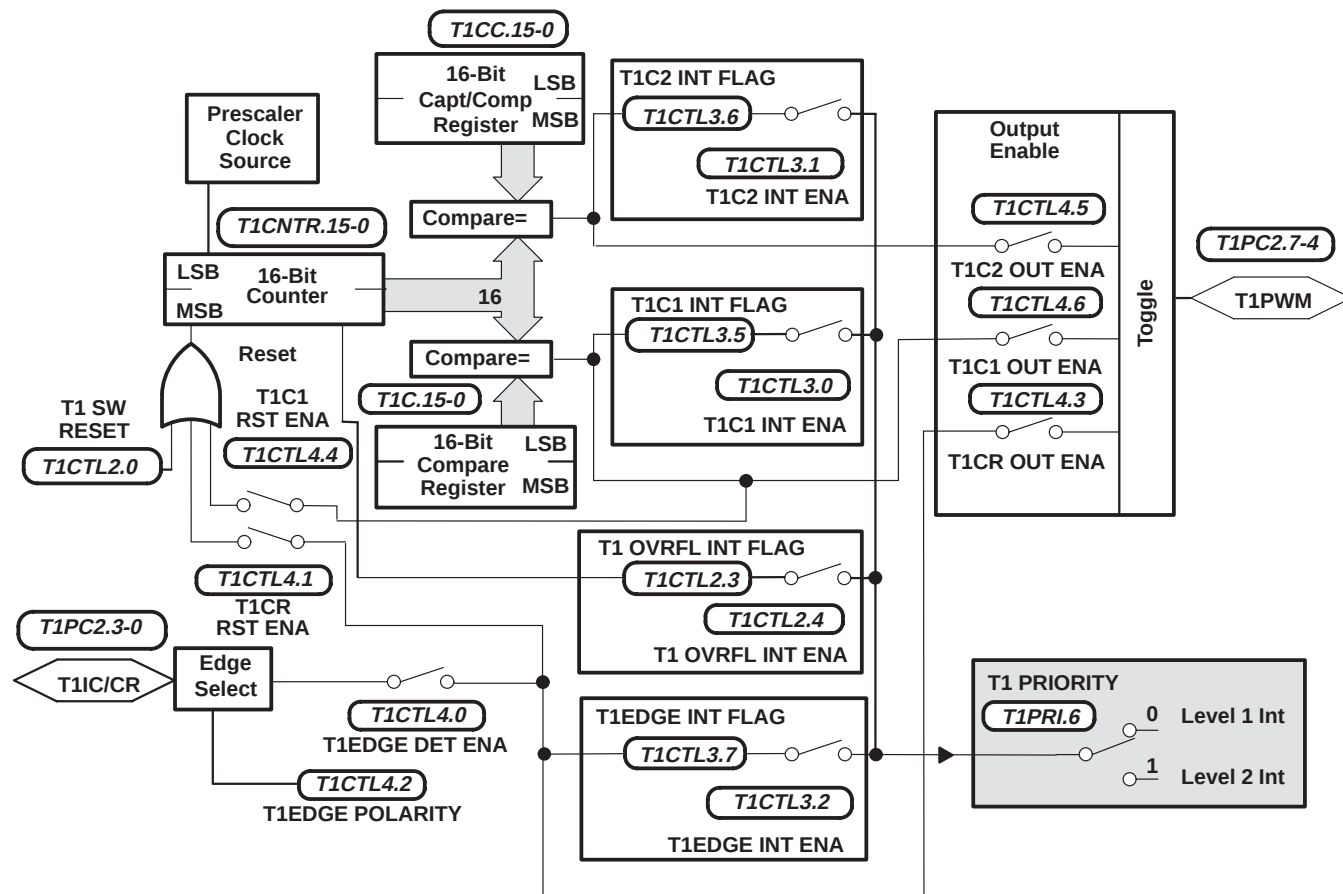


Figure 7. Dual-Compare Mode

timer 1 module (continued)

The TMS370Cx9x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation and implement a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard WD, hard WD, or simple counter.

- Standard watchdog configuration for EPROM and mask-ROM devices (see Figure 8)
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

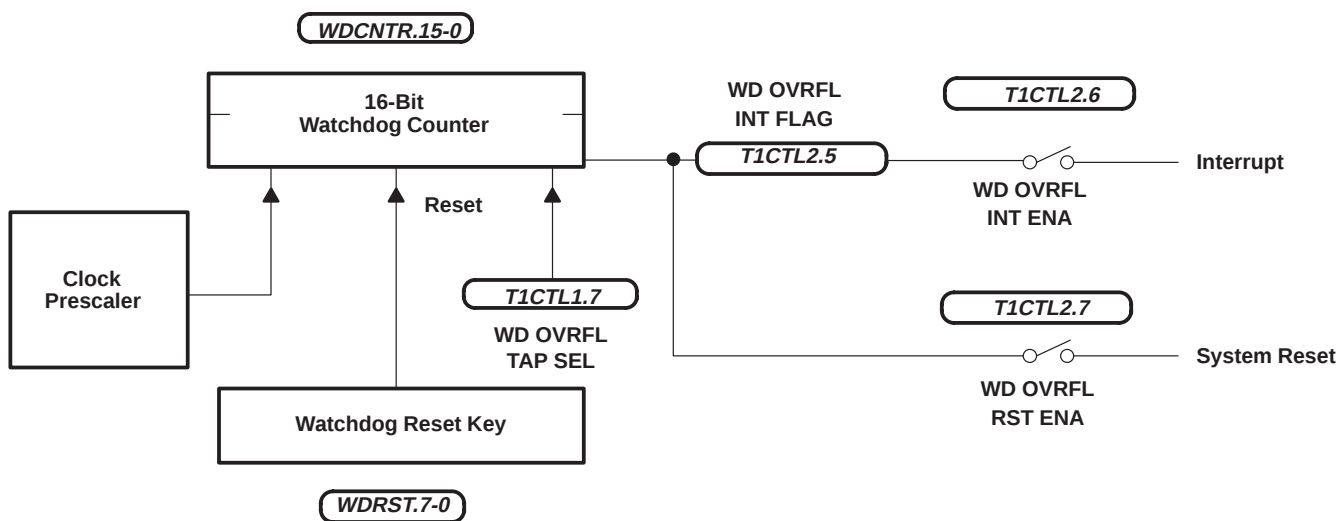


Figure 8. Standard Watchdog

timer 1 module (continued)

- Hard watchdog configuration for mask-ROM device only (see Figure 9)
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as nonmaskable interrupt during low-power modes
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset.

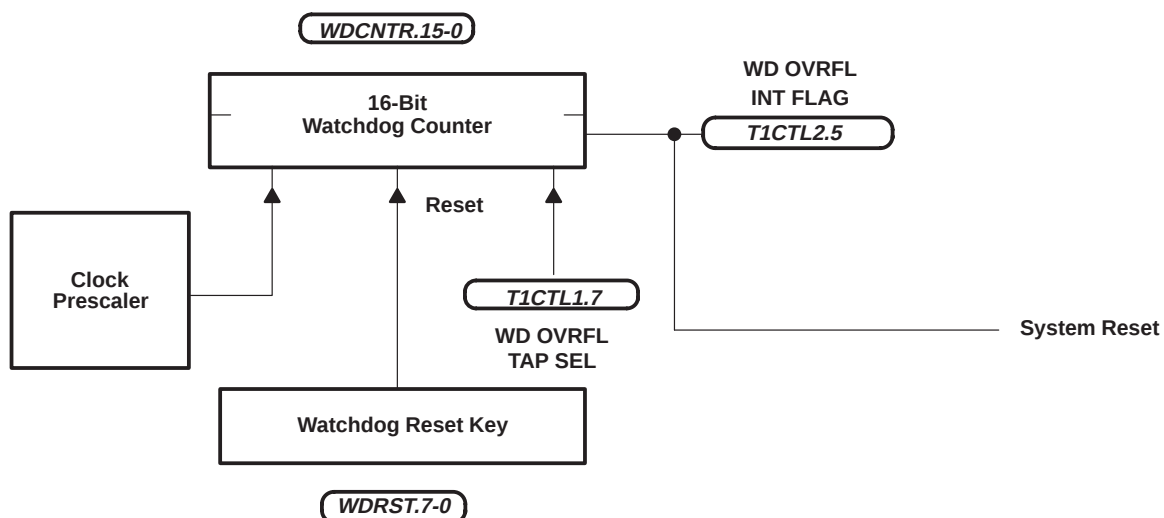


Figure 9. Hard Watchdog

timer 1 module (continued)

- Simple-counter configuration for mask-ROM devices only (see Figure 10)
 - Simple counter can be configured as an event counter, pulse accumulator, or an interval timer.

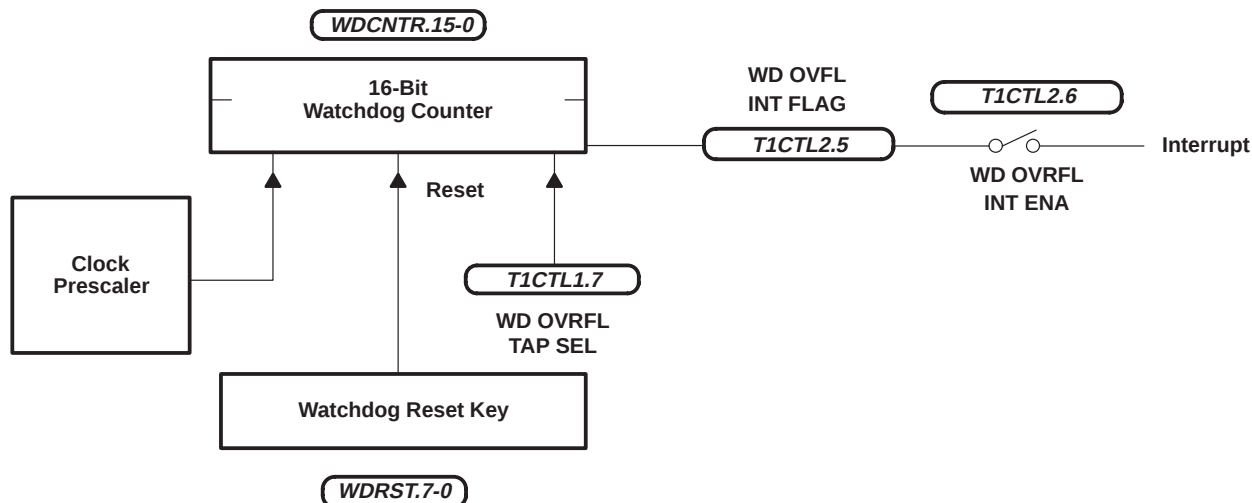


Figure 10. Simple Counter

analog-to-digital converter 3 module

The analog-to-digital converter 3 module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has fifteen analog input channels – eight of the channels are multiplexed with port E – that allow the processor to convert the voltage levels from up to fifteen different sources. The ADC3 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Seventeen external pins:
 - Fifteen analog input channels (AN0–AN14), eight (AN0–AN7) of which can be software configured as digital inputs (E0–E7) if not needed as analog channels
 - AN6–AN7 can also be configured as positive input voltage reference
 - V_{CC3}: ADC3 module high-voltage reference input
 - V_{SS3}: ADC3 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last ADC3 conversion
- ADC3 operations can be accomplished through either interrupt driven or polled algorithms
- Six ADC3 module control registers are located in the ADC3 peripheral control register frame beginning at address 1070h.

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analog-to-digital converter 3 module (continued)

The ADC3 module control registers are illustrated in Table 14.

Table 14. ADC3 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT3	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	AD RATE SELECT1	AD RATE SELECT0	ADPRI

The A/D module block diagram is illustrated in Figure 11.



analog-to-digital converter 3 module (continued)

Table 15. ADC3 Peripheral Control Register (ADCTL)

Bit #	7	6	5	4	3	2	1	0
P070	CONVERT START	SAMPLE START	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT3	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R = read, W = write, –n = value of the bit after the register is reset

BIT 0–3 AD INPUT SELECT 0–3 (Analog Input Channel Select Bits 0–3)

These bits select the channel used for conversion. Channels should be changed only after the ADC3 has cleared the SAMPLE START and CONVERT START bits. Changing the channel while either SAMPLE START or CONVERT START is 1 invalidates the conversion in progress.

AD INPUT SELECT 3	AD INPUT SELECT 2	AD INPUT SELECT 1	AD INPUT SELECT 0	AD INPUT CHANNEL
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14

BIT 4–5 REF VOLT SELECT 4–5 (Reference Voltage (+V_{REF}) Select Bits 4–5)

These bits select the channel the ADC3 uses for the positive voltage reference. These bits must not change during the entire conversion.

REF VOLT SELECT 1	REF VOLT SELECT 0	+V _{REF} SOURCE
0	0	VCC3
0	1	AN6
1	0	AN7

BIT 6 SAMPLE START (Sample Start)

Setting this bit stops any ongoing conversion and starts sampling the selected input channel to begin a new conversion. This bit is cleared by the ADC3. Entering HALT or STANDBY mode clears this bit and aborts any sampling in progress.

BIT 7 CONVERT START (Conversion Start)

Setting this bit starts the conversion. This bit is cleared by the ADC3. Entering HALT or STANDBY mode clears this bit and aborts any conversion in progress.

analog-to-digital converter 3 module (continued)

Table 16. ADC3 Peripheral Control Register (ADSTAT)

Bit #	7	6	5	4	3	2	1	0
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA
						R–0	RC–0	RW–0

R = read, W = write, C = clear only, –n = value of the bit after the register is reset

BIT 0 AD INT ENA (ADC3 Interrupt Enable)

This bit controls the ADC3 module's ability to generate an interrupt.

0 = Disable ADC3 interrupt.

1 = Enable ADC3 interrupt.

BIT 1 AD INT FLAG (ADC3 Interrupt Flag)

The ADC3 module sets this bit at the end of an A/D conversion. If this bit is set while the AD INT ENA bit is set, an interrupt request is generated. Clearing this flag clears pending ADC3 interrupt requests. This bit is cleared by the system reset or by entering HALT or STANDBY mode. Software cannot set this bit.

BIT 2 AD READY (ADC3 Converter Ready)

The ADC3 module sets this bit whenever a conversion is not in progress and the ADC3 is ready for a new conversion to start. Writing to this bit has no effect on its state.

0 = Conversion in process.

1 = Converter ready.

BIT 3–7 Reserved (Read data is indeterminate)

Table 17. ADC3 Conversion Data Register (DATA)

Bit #	7	6	5	4	3	2	1	0
P072	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
	R–0	R–0	R–0	R–0	R–0	R–0	R–0	R–0

R = read, –n = value of the bit after the register is reset

The analog-to-digital conversion data is loaded into this register at the end of a conversion and remains until replaced by another conversion

Table 18. AN0–AN7 Data Input Register (ADIN)

Bit #	7	6	5	4	3	2	1	0
P07D	PORT E DATA IN AN7	PORT E DATA IN AN6	PORT E DATA IN AN5	PORT E DATA IN AN4	PORT E DATA IN AN3	PORT E DATA IN AN2	PORT E DATA IN AN1	PORT E DATA IN AN0
	R–0	R–0	R–0	R–0	R–0	R–0	R–0	R–0

R = read, –n = value of the bit after the register is reset

analog-to-digital converter 3 module (continued)

The ADIN register shows the data present at the pins configured for general-purpose input instead of ADC3 channels. A bit is configured as general-purpose input if the corresponding bit of the port-enable register is a 1. Pins configured as ADC3 channels are read as 0's. Writing to this address has no effect.

Table 19. AN0–AN7 Input-Enable Register (ADENA)

Bit #	7	6	5	4	3	2	1	0
P07E	INPUT ENA 7	INPUT ENA 6	INPUT ENA 5	INPUT ENA 4	INPUT ENA 3	INPUT ENA 2	INPUT ENA 1	INPUT ENA 0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R = read, –n = value of the bit after the register is reset

The ADENA register individually configures the pins AN0–AN7 as either analog input channels or as general-purpose input pins

0 = The pin becomes an analog-input channel for the ADC3. When the bit is 0, the corresponding bit in the ADIN register reads a 0.

1 = Enables the pin as a general-purpose input pin and its digital value can be read from the corresponding bit in the ADIN register.

Table 20. Analog Interrupt Priority/Conversion Rate Register (ADPRI)

Bit #	7	6	5	4	3	2	1	0
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	AD RATE SELECT1	AD RATE SELECT0
	RP–0	RP–0	RP–0				RW–0	RW–0

R = read, W = write, P = privileged write, –n = value of the bit after the register is reset

BIT 0–1 AD RATE SELECT 0–1 (ADC3 Conversion Rate Select Bits 0–1)

These bits determine the conversion rate of the ADC3 as a function of the system-clock frequency. Note that only the default selection (0,0) provides full XTAL2/CLKIN frequency range together with 8-bit precision. Other selections allow maintaining minimum conversion time at lower system-clock rates.

AD RATE SELECT 1	AD RATE SELECT 0	CONVERSION TIME (NUMBER OF SYSTEM CLOCK CYCLES)	MAXIMUM SYSCLK FREQUENCY
0	0	164	5 MHz ≥ SYSCLK > 2.5 MHz
0	1	84	2.5 MHz ≥ SYSCLK > 1.25 MHz
1	0	44	1.25 MHz ≥ SYSCLK > 0.625 MHz
1	1	22	0.625 MHz ≥ SYSCLK ≥ 0.5 MHz

NOTE: If selections different from (0,0) are used at XTAL2/CLKIN frequencies higher than specified in this table, the 8-bit precision of the ADC3 is not assured.

BIT 2–4 RESERVED (Read data is indeterminate)

analog-to-digital converter 3 module (continued)

- | | |
|-------|---|
| BIT 5 | <p>AD ESPEN (Emulator Suspend Enable)</p> <p>Normally this bit has no effect. However, when using the XDS emulator to debug a program, this bit determines what happens to the ADC3 when the program is suspended by an action such as a hardware or software breakpoint.</p> <p>0 = When the emulator is suspended, the ADC3 continues to run until the conversion is complete.</p> <p>1 = When the emulator is suspended, the ADC3 is frozen so that its state can be examined at the point that the emulator was suspended. The conversion data is indeterminate upon restart.</p> |
| BIT 6 | <p>AD PRIORITY (ADC3 interrupt priority select)</p> <p>This bit selects the priority level of the ADC3 interrupt.</p> <p>0 = ADC3 Interrupt is a higher priority (level 1) request.</p> <p>1 = ADC3 Interrupt is a lower priority (level 2) request.</p> |
| BIT 7 | <p>AD STEST (This bit must be cleared to ensure proper operation)</p> |

instruction set overview

Table 21 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx9x instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

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Table 21. TMS370 Family Opcode/Instruction Map†

		MSN																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0		JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1		JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7					MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2		JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7	
3		JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4		JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5		JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6		JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7		JNC ra 2/5	BTJZ Rs,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8		JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9		JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A		JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV A,lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A,lab 3/10	MOV A,*Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 21. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = Register file
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, CDT, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Provides format conversion utilities for popular formats
- ANSI C compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™, or Sun-4™)
 - Generates assembly code for the TMS370 that can be easily inspected
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct referencing of the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) PACT real-time in-circuit emulation
 - Base (Part Number EDSCDT37P – for PC, requires cable)
 - Cable for 40-pin SDIP (Part No. EDSTRG40SDIL05)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC05)
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Uploads/downloads program and data memory
 - Executes programs and software routines
 - Includes 1024-sample trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A — for PC, requires programmer head)
 - Single unit head for 44-pin PLCC and 40-pin SDIP (Part No. TMDS3780513A)
 - Includes PC-based, window/function-key oriented user interface for ease of use and rapid learning environment

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device numbering conventions

Figure 12 illustrates the numbering and symbol nomenclature for the TMS370Cx9x family.

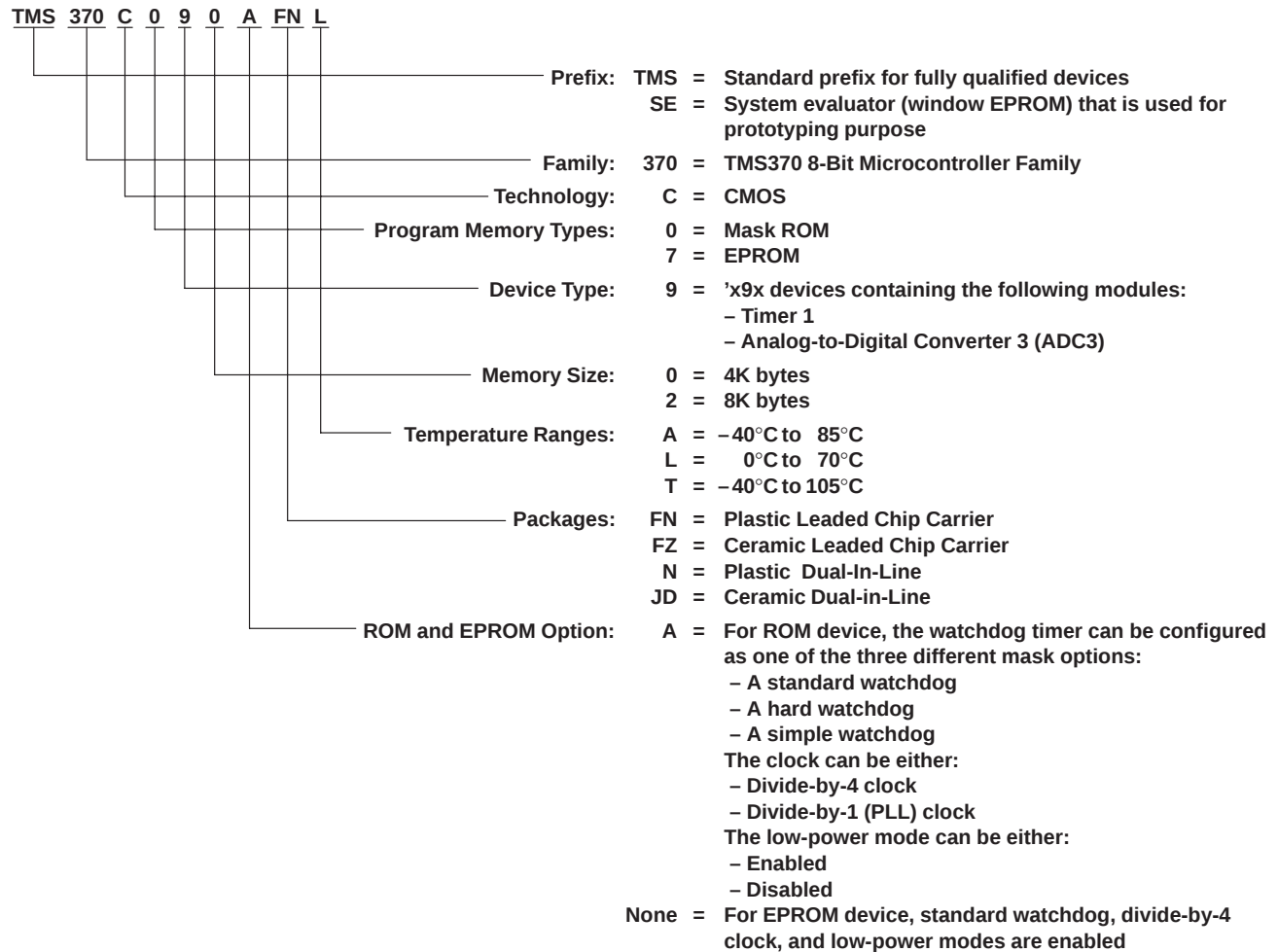


Figure 12. TMS370Cx9x Family Nomenclature

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device part numbers

Table 22 provides all the TMS370Cx9x devices available. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog-timer options desired. Each device can only have one of the three possible watchdog-timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 22. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)	DEVICE PART NUMBERS FOR 40 PINS (SDIP)
TMS370C090AFNA TMS370C090AFNL TMS370C090AFNT	TMS370C090ANJA [†] TMS370C090ANJL [‡] TMS370C090ANJT [‡]
TMS370C792FNT	TMS370C792NJT [‡]
SE370C792FZT [†]	SE370C792JCT [†]

[†] System evaluators are for use only in prototype environment, and their reliability has not been characterized.

[‡] The NJ designator for the 40-pin plastic shrink DIP package was formerly known as N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

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Table 23. Peripheral File Frame Compilation

Table 23 is a collection of all the peripheral file frames using the 'Cx9x (provided for a quick reference).

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018 to P019	Reserved								
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 [†] (must be 0)					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	Modes: Capture/Compare and Dual-Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 7	Watchdog Reset Key						Bit 0	WDRST

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 23. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Capture/Compare and Dual-Compare (Continued)									
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
P070	CONVERT START	SAMPLE START	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT3	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SE- LECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	AD RATE SELECT1	AD RATE SELECT0	ADPRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range V_{CC} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) [‡]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)	3		5.5	
V_{CC3}	Analog supply voltage (see Note 1)	3		5.5	V
V_{SS3}	Analog supply ground	–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC}	V
		XTAL2/CLKIN		$0.8 V_{CC}$	
		RESET		$0.7 V_{CC}$	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)		13	V
		EPROM programming voltage (V_{PP})		13.5	
		Microcomputer		V_{SS}	
T_A	Operating free-air temperature	L version		70	°C
		A version		85	
		T version		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. RESET must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

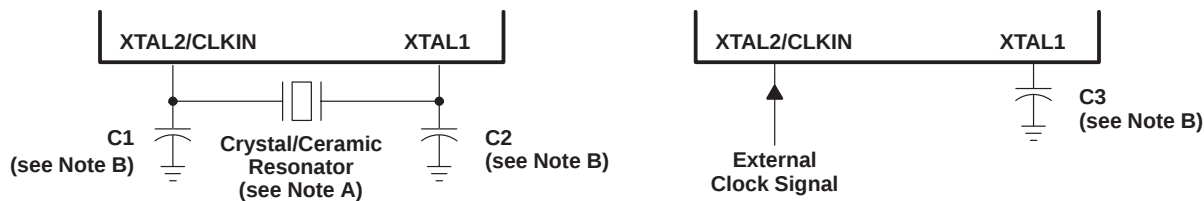


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = –50 µA	0.9 V _{CC}			V
		I _{OH} = –2 mA	2.4			
I _I	Input current	MC	0 V < V _I ≤ 0.3 V		10	µA
			0.3 V < V _I ≤ 13 V		650	
		12 V ≤ V _I ≤ 13 V	See Note 3		50	mA
	I/O pins	0 V ≤ V _I ≤ V _{CC}			± 10	µA
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC}	– 50			µA
		V _{OH} = 2.4 V	– 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 6)	SYSClk = 5 MHz	See Notes 4 and 5	30	45	mA
		SYSClk = 3 MHz	See Notes 4 and 5	20	30	
		SYSClk = 0.5 MHz	See Notes 4 and 5	7	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 7)	SYSClk = 5 MHz	See Notes 4 and 5	10	17	mA
		SYSClk = 3 MHz	See Notes 4 and 5	8	11	
		SYSClk = 0.5 MHz	See Notes 4 and 5	2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 8)	SYSClk = 3 MHz	See Notes 4 and 5	6	8.6	mA
		SYSClk = 0.5 MHz	See Notes 4 and 5	2	3	
	Supply current (HALT mode)	XTAL2/CLKIN < 0.2 V	See Note 4	2	30	µA

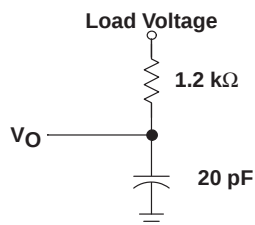
- NOTES:
- Input current I_{pp} is a maximum of 50 mA only when programming EPROM.
 - In single chip mode, ports are configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2V.
 - XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSClk, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
 - Maximum operating current for TMS370Cx9x = 7.6 (SYSClk) + 7 mA.
 - Maximum standby current for TMS370Cx9x = 3 (SYSClk) + 2 mA. (OSC POWER bit = 0).
 - Maximum standby current for TMS370Cx9x = 2.24 (SYSClk) + 1.9 mA. (OSC POWER bit =1, only valid up to 3-MHz SYSClk).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
 B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 14. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
 Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 15. Typical Output Load Circuit (see Note A)

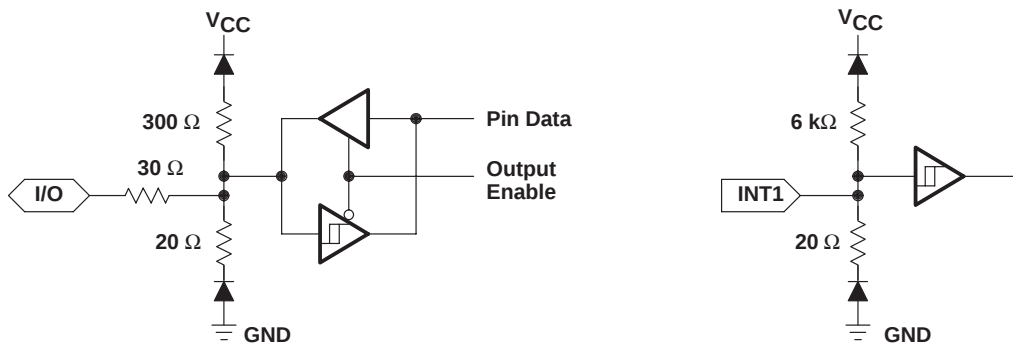


Figure 16. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	IE	Initial
AR	Array	PGM	Program
B	Byte	R	Read
CI	XTAL2/CLKIN	SC	SYSCLK
D	Data	W	Write
E	$\overline{\text{EDS}}$	WT	$\overline{\text{WAIT}}$
FE	Final		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 17 and Figure 18.



Figure 17. XTAL2/CLKIN Measurement Points

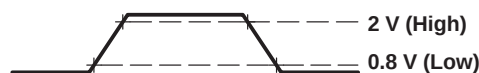


Figure 18. General Measurement Points

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external clocking requirements for clock divided by 4[†] (see Figure 19)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_W(\text{Cl})$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_r(\text{Cl})$ Rise time, XTAL2/CLKIN		30	ns
3	$t_f(\text{Cl})$ Fall time, XTAL2/CLKIN		30	ns
4	$t_d(\text{ClH-SCL})$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK System clock [‡]	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[‡] SYSCLK = CLKIN/4

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

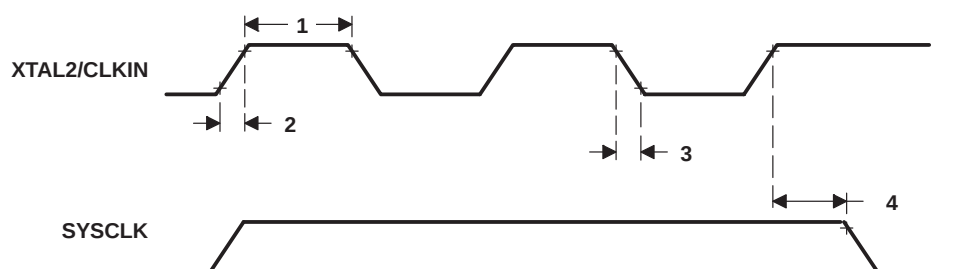


Figure 19. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†] (see Figure 20)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_W(\text{Cl})$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_r(\text{Cl})$ Rise time, XTAL2/CLKIN		30	ns
3	$t_f(\text{Cl})$ Fall time, XTAL2/CLKIN		30	ns
4	$t_d(\text{ClH-SCH})$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK System clock [§]	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[§] SYSCLK = CLKIN/1

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

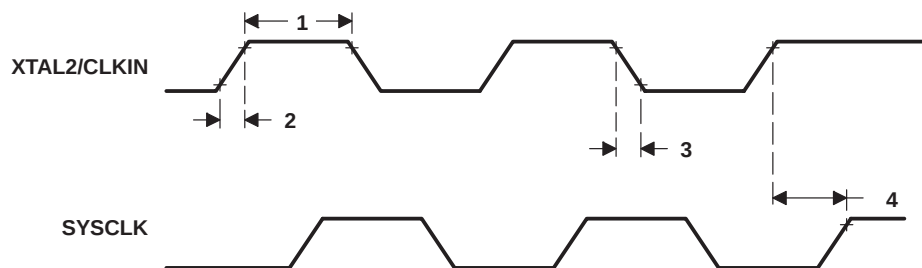


Figure 20. External Clock Timing for Divide-by-1

switching characteristics and timing requirements[†]

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK	200	2000	ns
		Divide-by-4	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5t_c$	$0.5t_c + 20$	ns

[†] t_c = system-clock cycle time = 1/SYSCLK

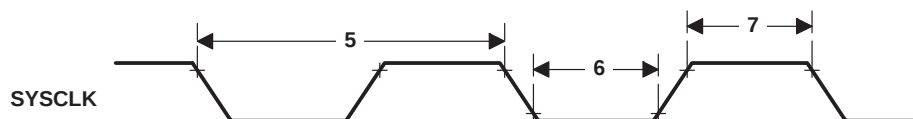


Figure 21. Switching Characteristics

general purpose output signal switching time requirements

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

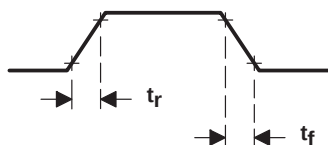


Figure 22. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$	10		ms
$t_{w(PGM)AR}$	20		ms

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recommended EPROM operating conditions for programming

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5.5	6	V
V _{PP}	Supply voltage at MC pin	13	13.2	13.5	V
I _{PP}	Supply current at MC pin during programming (V _{PP} = 13 V)		30	50	mA
SYSCLK	System clock	Divide-by-4	0.5	5	MHz
		Divide-by-1	2	5	

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
t _w (EPGM)	Pulse duration, programming signal (see Note 10)	0.40	0.50	3	ms

NOTE 10: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



analog-to-digital converter 3

The ADC3 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC3 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS} and V_{CC} from coupling into the ADC3 analog stage. All ADC3 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) 164 t_c

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC}-0.3$		$V_{CC}+0.3$	
V_{SS3} Analog ground	$V_{SS}-0.3$		$V_{SS}+0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER		MIN	MAX	UNIT
Absolute accuracy [‡]	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V	± 1.5		LSB
Differential/integral linearity error ^{‡§}	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V	± 0.9		LSB
I_{CC3} Analog supply current	Converting		2	mA
	Nonconverting		5	μ A
I_I Input current, AN0–AN14	0 V $\leq V_I \leq 5.5$ V		2	μ A
I_{ref} Input charge current			1	mA
Z_{ref} Source impedance of V_{ref}	$SYSCLK \leq 3$ MHz		24	k Ω
	3 MHz $< SYSCLK \leq 5$ MHz		10	k Ω

[‡] Absolute resolution = 20 mV. At $V_{ref} = 5$ V, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

[§] Excluding quantization error of 1/2 LSB

analog-to-digital converter 3 (continued)

The ADC3 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance sources can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC3 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements†

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion†	$(N+2)t_C$		ns
$t_{w(C)}$	Conversion time†	$(10N + 4)t_C$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance‡	1		$\mu s/k\Omega$

† N = 16, 8, 4, or 2 upon selected conversion rate.

‡ The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

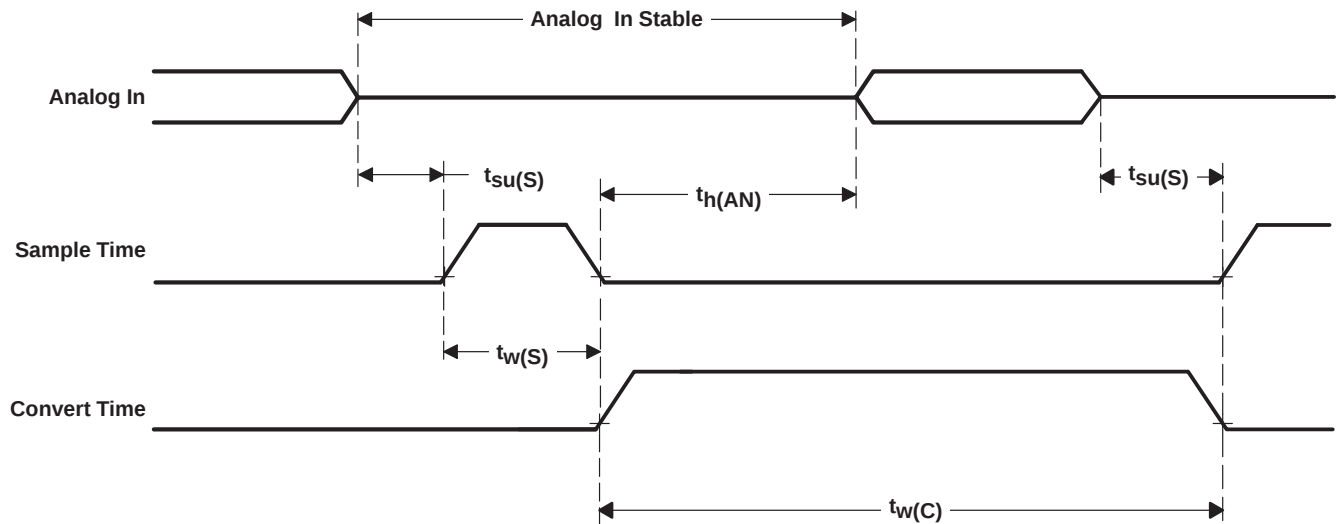


Figure 23. Analog Timing

Table 24 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 24. TMS370Cx9x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C090AFNA TMS370C090AFNL TMS370C090AFNT TMS370C792FNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C792FZT
JC – 40 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JC(R-CDIP-T40) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C792JCT
NJ – 40 pin (70-mil pin spacing) [†]	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NJ(R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C090ANJA TMS370C090ANJL TMS370C090ANJT TMS370C792NJT

[†] NJ formerly known as N2; the mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

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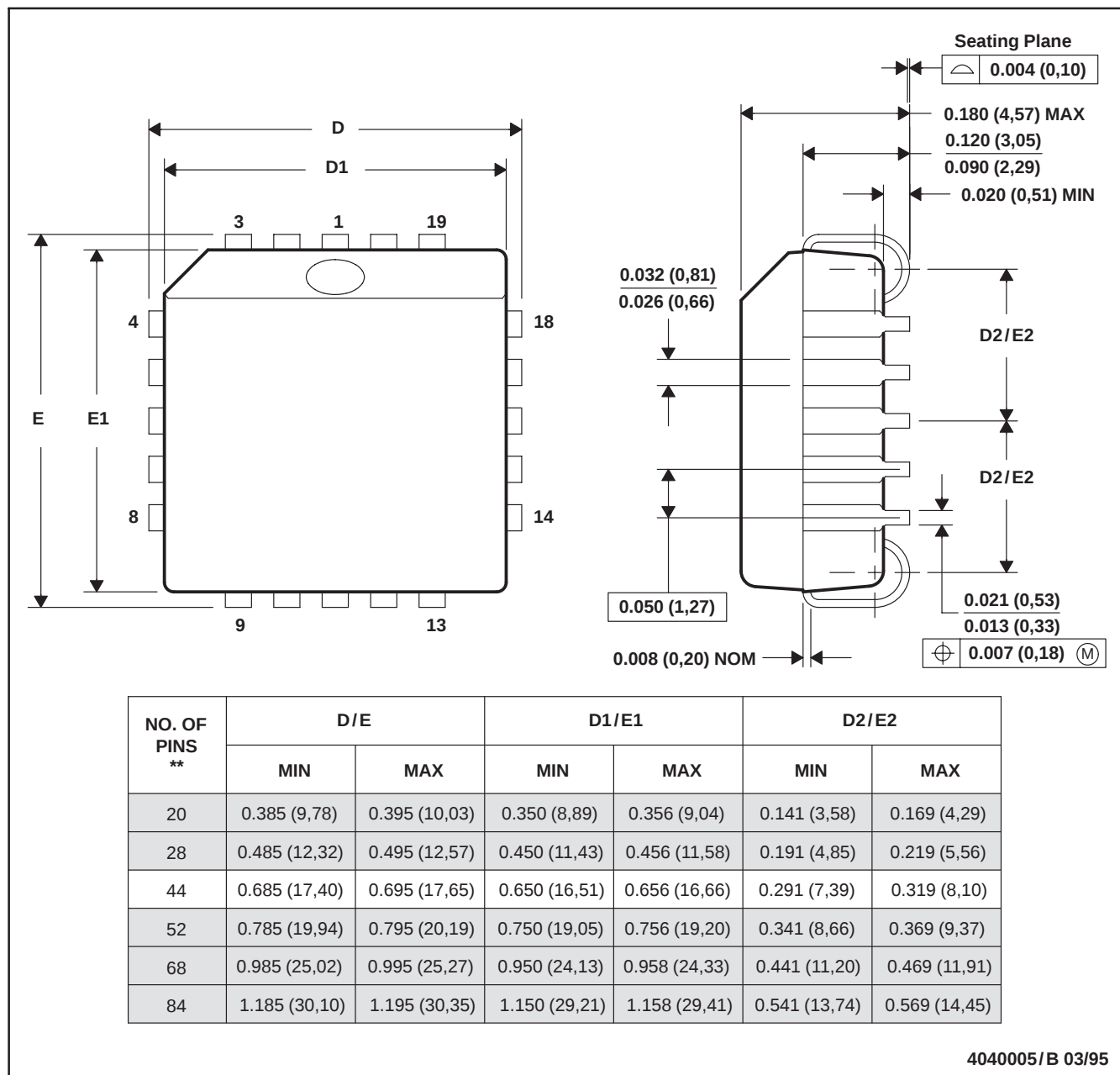
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MECHANICAL DATA

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



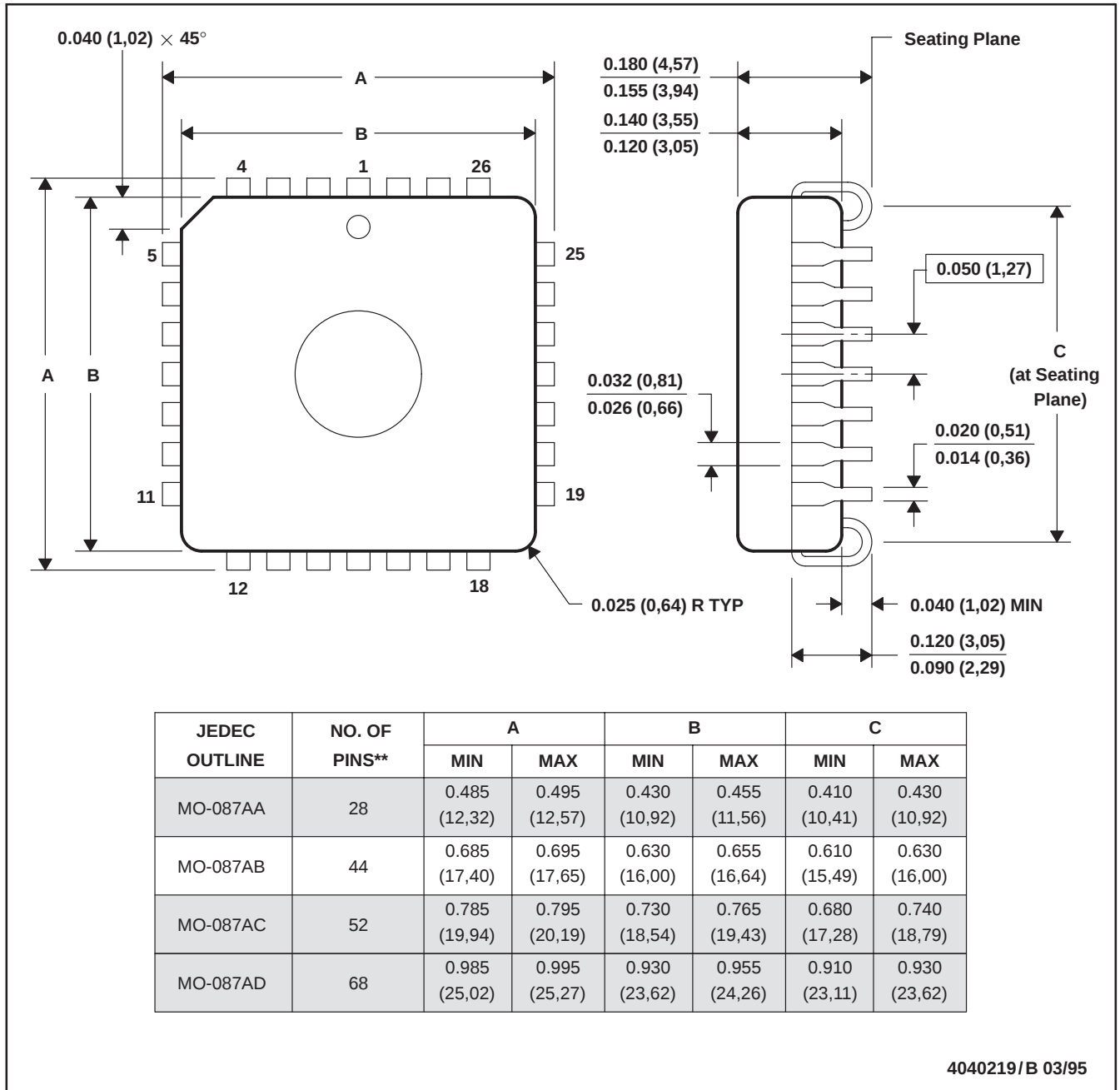
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MECHANICAL DATA

FZ (S-CQCC-J)**

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.

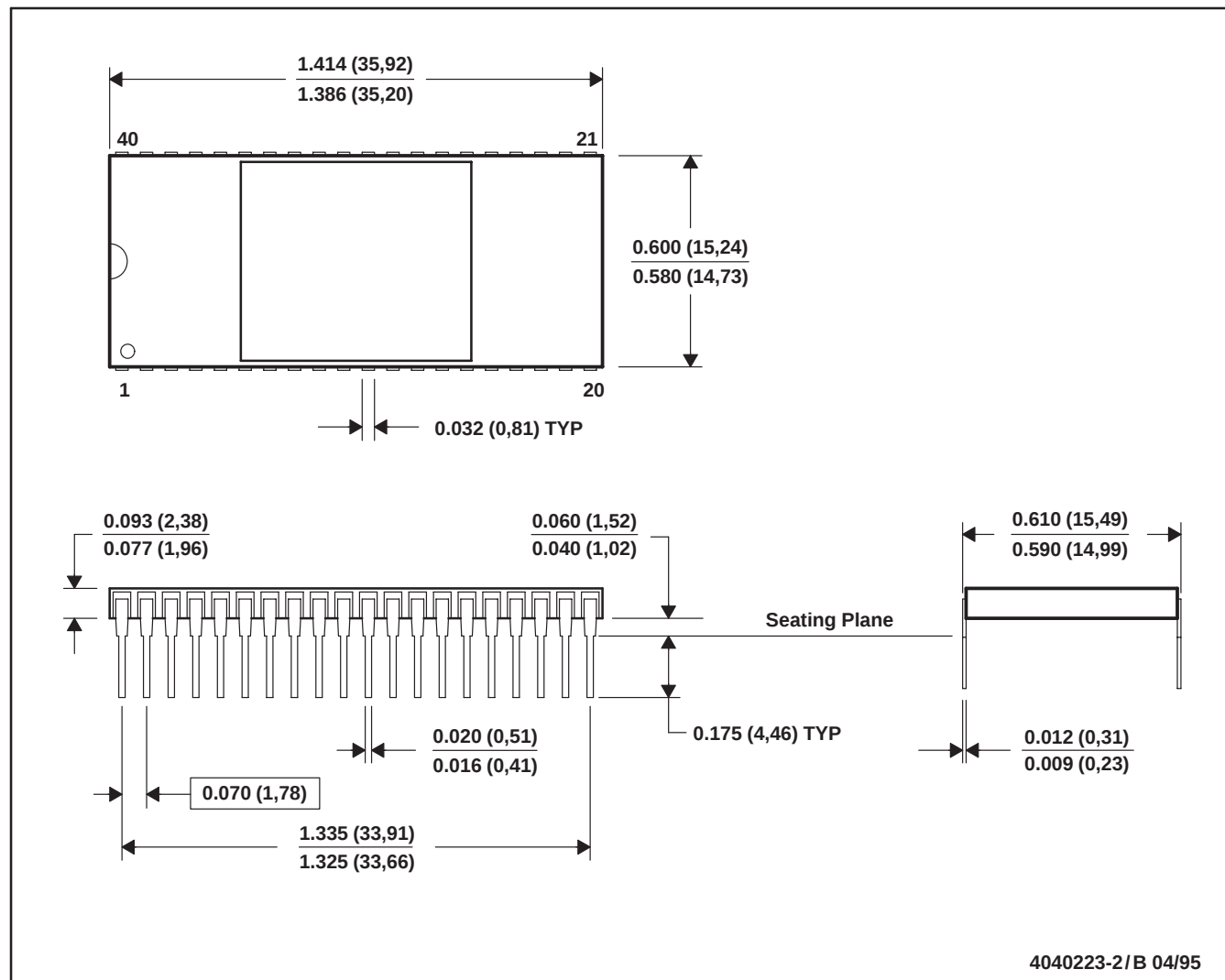
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MECHANICAL DATA

JC (R-CDIP-T40)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE



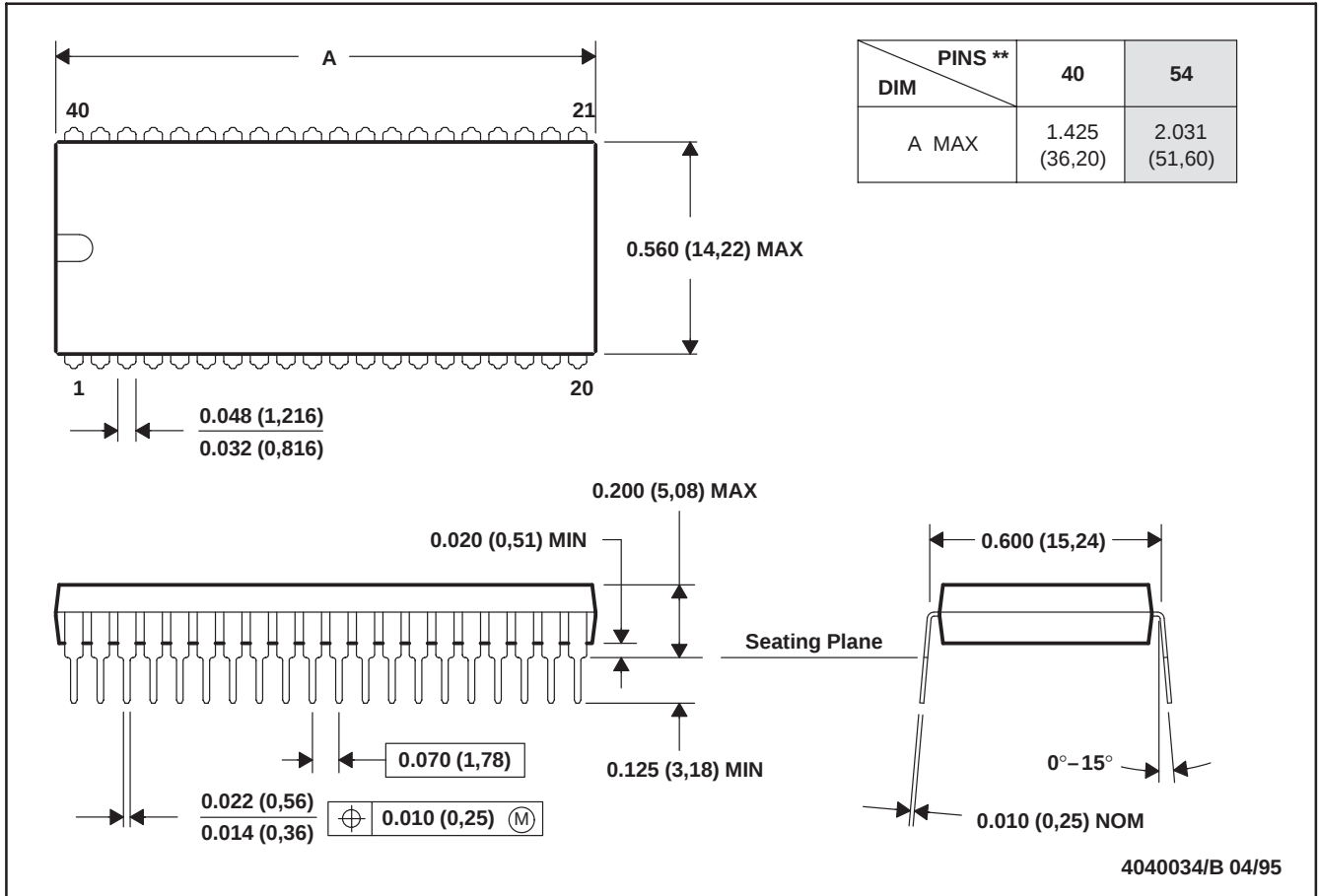
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.

MECHANICAL DATA

NJ (R-PDIP-T**)

PLASTIC SHRINK DUAL-IN-LINE PACKAGE

40 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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