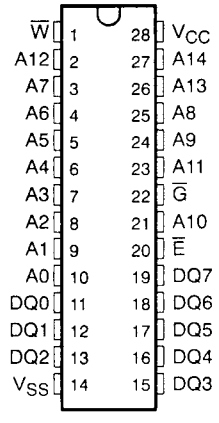
- Organization 32K × 8
- Single 5-V Power Supply
- HVCMOS Technology
- All Inputs/Outputs TTL Compatible
- Max Access/Min Cycle Time

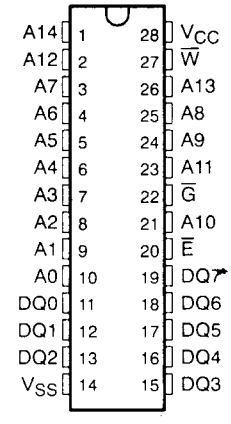
V_{CC} ± 5%	V_{CC} ± 10%	
'29F256/8/9-170		170 ns
'29F256/8/9-200	'29F256/8/9-20	200 ns
'29F256/8/9-250	'29F256/8/9-25	250 ns
'29F256/8/9-300	'29F256/8/9-30	300 ns

- Self-Timed Erasure of the Entire Memory Before any Reprogramming (15 ms MAX)
- Single Byte and Page (64 Bytes) Program:
  - Latched Address and Data
  - Self-Timed Programming Operation (15 ms MAX)
  - Data Polling Verification
- 100, 1000, and 10000 Cycles Endurance Versions
- Software Inadvertent Write Protection
- Software Erase Mode Entry
- TMS29F256 Pinout Compatible With EPROM JEDEC Standard
- TMS29F258 Pinout Compatible With EEPROM JEDEC Standard
- Choice of Operating Temperature Ranges

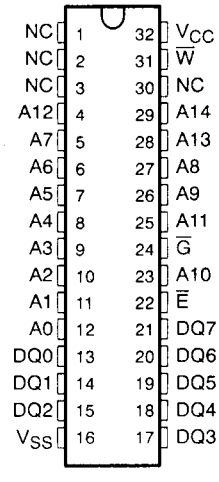
TMS29F256 . . . N Package
TMS29F256 . . . J Package
(Top View)



TMS29F258 . . . N Package
TMS29F258 . . . J Package
(Top View)



TMS29F259 . . . N Package
TMS29F259 . . . J Package
(Top View)



description

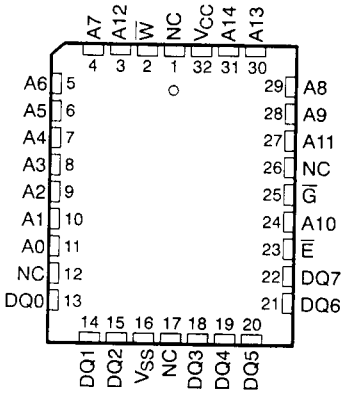
The TMS29F256, TMS29F258, and TMS29F259 are 262 144-bit, programmable read-only memories that can be electrically bulk-erased and reprogrammed. These devices are fabricated using HVCMOS flotox technology for high reliability and very low power dissipation. They perform the erase/program operations automatically with a single 5-V supply, and they can program a single byte or any number of bytes between 1 and 64.

The TMS29F256, TMS29F258, and TMS29F259 Flash EEPROMs are offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS29F256, TMS29F258, and TMS29F259 in

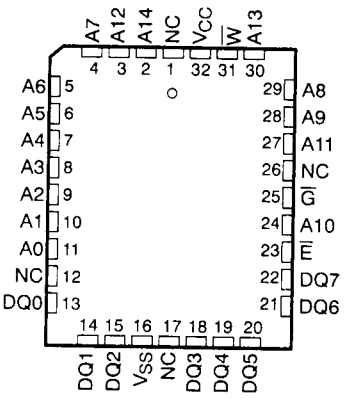
PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0-DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{SS}	Ground

the ceramic package are each offered with three guaranteed temperature ranges of 0°C to 70°C, – 40°C to 85°C, and – 40°C to 125°C (TMS29F256-_ _JL, TMS29F258-_ _JL, and TMS29F259-_ _JL for 0°C to 70°C; TMS29F256-_ _JE, TMS29F258-_ _JE, and TMS29F259-_ _JE for – 40°C to 85°C; and TMS29F256-_ _JQ, TMS29F258-_ _JQ, and TMS29F259-_ _JQ for – 40°C to 125°C).

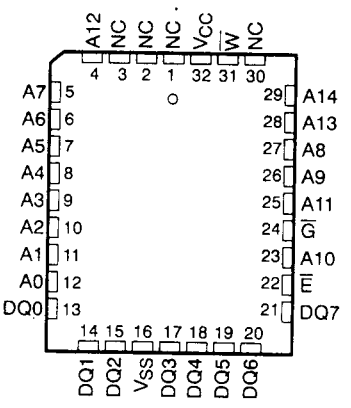
TMS29F256
FM PACKAGE
(TOP VIEW)



TMS29F258
FM PACKAGE
(TOP VIEW)



TMS29F259
FM PACKAGE
(TOP VIEW)



The TMS29F256, TMS29F258, and TMS29F259 are also offered with 168 hour burn-in temperature ranges (TMS29F256-_ _JL4, JE4, and JQ4; TMS29F258-_ _JL4, JE4, and JQ4; TMS29F259-_ _JL4, JE4, and JQ4, respectively). (See table on page 7-29.)

The TMS29F256, TMS29F258, and TMS29F259 are also offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS29F256, TMS29F258, and TMS29F259 are offered in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). These packages are guaranteed from 0°C to 70°C (NL or FML suffix).

The TMS29F256, TMS29F258, and TMS29F259 are organized as 32K × 8 bits. They feature internal circuitry to minimize the external hardware interface that provides latched address and data, self-timed programming, and data polling verification. In the erased state all bits are at a logic high. To reprogram, all memory bits are erased first, then those bits that should be logic lows are programmed accordingly. During programming, the data polling function is enabled, causing the memory to respond with the last data read except that the most significant bit is inverted to inform the host microprocessor that the memory is busy until the programming is completed.

The TMS29F256, TMS29F258, and TMS29F259 are available in 100 cycle endurance versions and will be available in 1000 and 10 000 cycle endurance versions.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Standby and Write Inhibit	Write	Signature Mode	
$\overline{E}$ (20)§	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	
$\overline{G}$ (22)§	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	
A0 (10)§	X	X	X	X	V_{IL}	V_{IH}
A9 (24)§	X	X	X	X	V_H‡	
$\overline{W}$ (1)§	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	
DQ0-DQ7 (11-13, 15-19)§	Data Out	HI-Z	HI-Z	Data In	MFG	DEVICE
					97	F1

† X = Don't care for V < V_{CC}.
‡ 12.5 V < V_H < 15 V.
§ TMS29F256 J and N package pins.

operation

read/output disable

When the outputs of two or more TMS29F256s, TMS29F258s, and TMS29F259s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices.

To read the output of the TMS29F256, TMS29F258, or TMS29F259 a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

power down

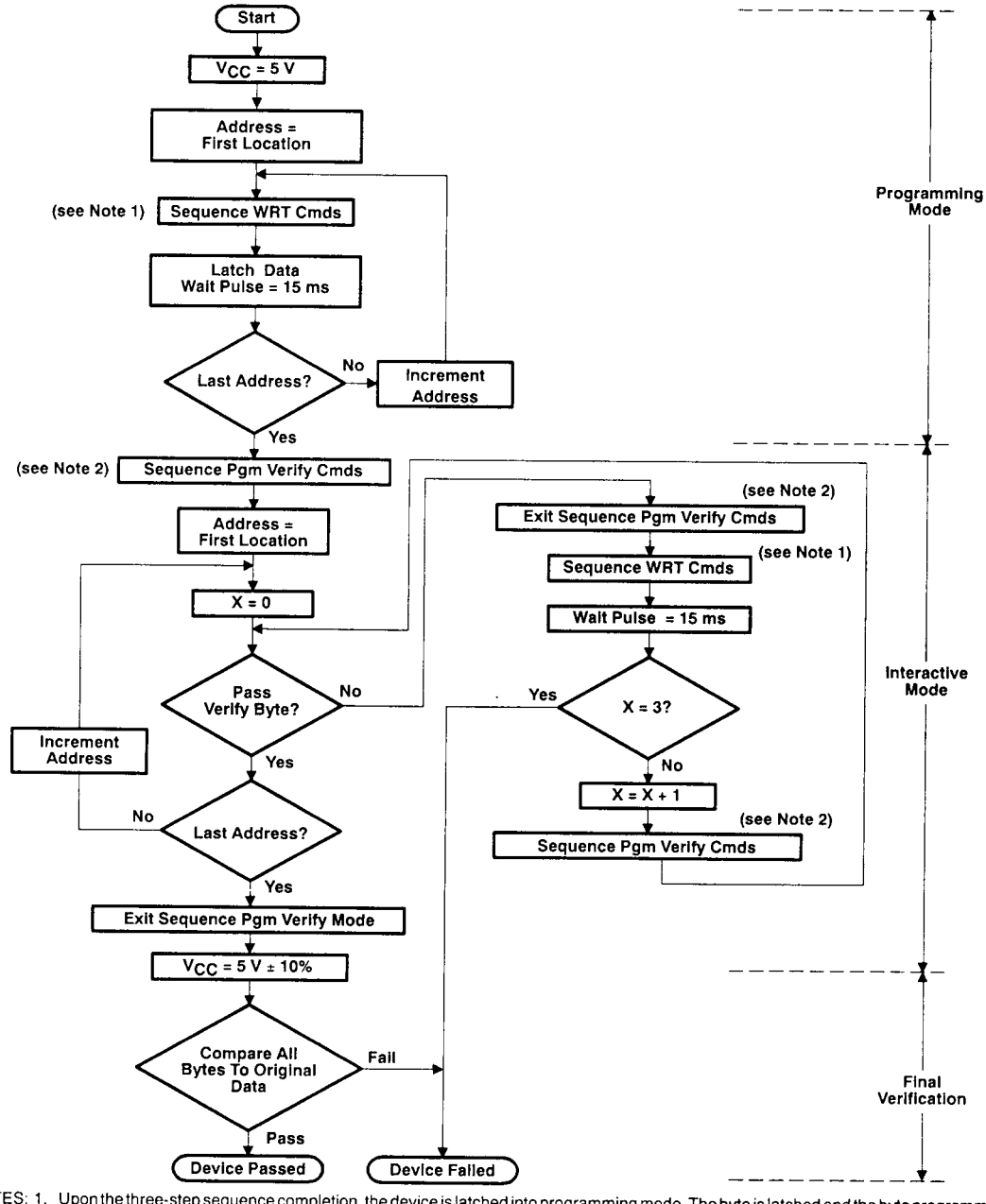
Active I_{CC} current can be reduced from 20 mA to 2 mA typically, by applying a high TTL signal to the $\overline{E}$ pin. In this mode all the outputs are in the high-impedance state.

single-byte program

The single-byte program initiates with $\overline{W}$ low and $\overline{G}$ high applied to a selected device. The addresses on the address pins will be latched on the falling edge of $\overline{E}$ or $\overline{W}$, whichever comes first. Figure 1 illustrates the single-byte programming flow.

After the latching operations are completed, the device starts automatically programming the data in the addressed location within the memory array. This internal programming operation is completed in 15 ms maximum.

FLASH EEPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN			SUFFIX FOR PEP4 168 HR. BURN-IN vs TEMPERATURE RANGES		
	0°C to 70°C	– 40°C to 85°C	– 40°C to 125°C	0°C to 70°C	– 40°C to 85°C	– 40°C to 125°C
TMS29F256-xxx	JL,NL,FML	JE	JQ	JL4	JE4	JQ4
TMS29F258-xxx	JL,NL,FML	JE	JQ	JL4	JE4	JQ4
TMS29F259-xxx	JL,NL,FML	JE	JQ	JL4	JE4	JQ4



NOTES: 1. Upon the three-step sequence completion, the device is latched into programming mode. The byte is latched and the byte programming operation starts if a subsequent rising edge of $\overline{W}$ is not detected within 100 µs.
2. Similar to the page programming mode.

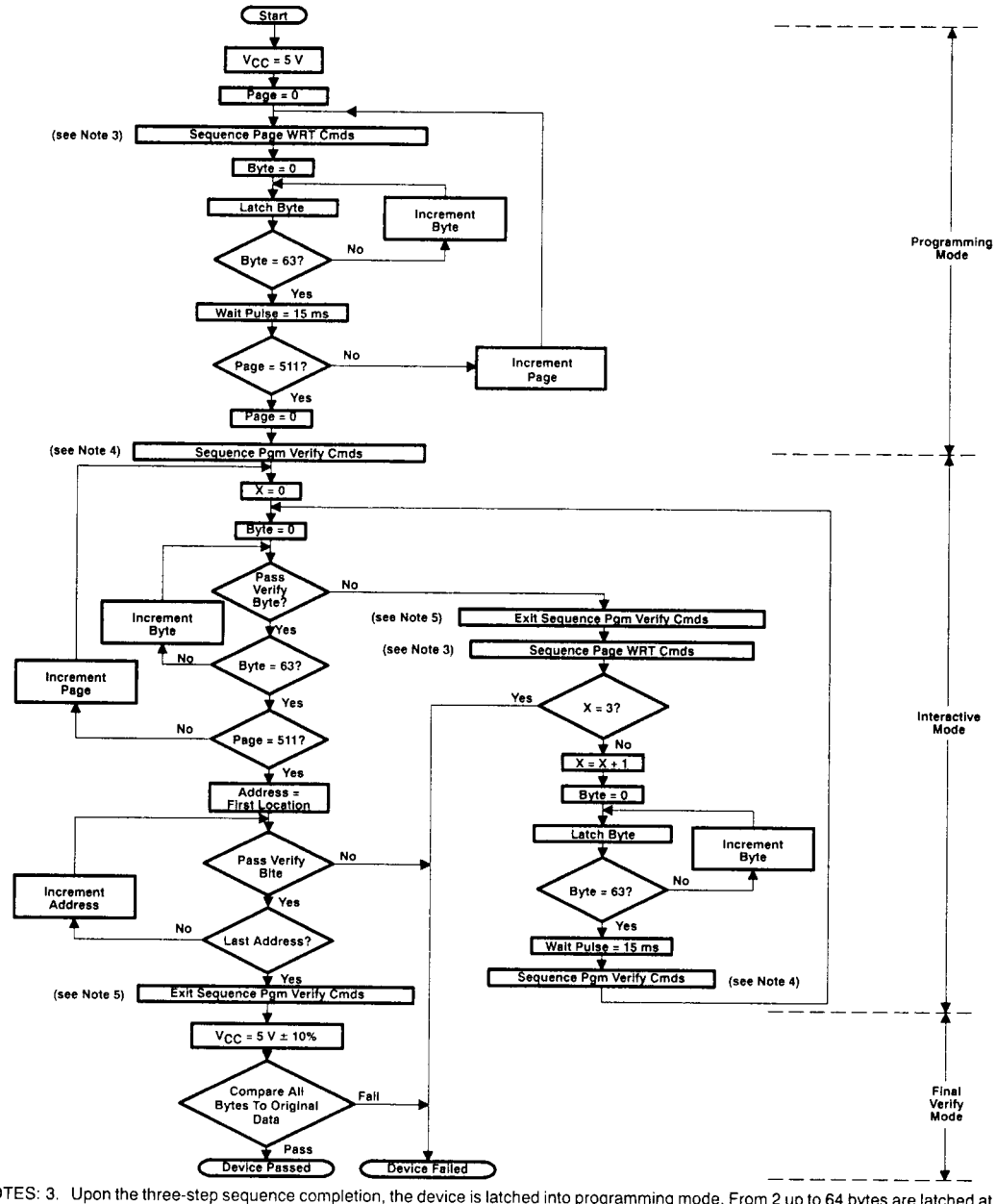
Figure 1. Single-byte Programming Flowchart

automatic page program

The page mode of the '29F256, '29F258, and '29F259 allow the user to program 2 to 64 bytes at a time. These bytes are initially loaded in the internal device register and then automatically stored in the addressed memory locations within the memory array. The internal programming operation is completed in 15 ms maximum, regardless of the number of bytes (64 maximum) loaded. During the page loading, the page address (A6 to A14) must be the same as the initial page address. Figure 2 illustrates the automatic page programming flow.

The page mode operation initiates in the same way as the single byte mode. After the first byte has been loaded, the '29F256, '29F258, and '29F259 can be loaded with 1 to 63 additional bytes. Each byte load cycle starts with the falling edge of $\overline{W}$, or $\overline{E}$, whichever comes last. A successive byte must be loaded within 100 μs from the rising edge of the previous byte load cycle. If a subsequent rising edge of $\overline{W}$ is not detected within 100 μs, the internal programming operation starts automatically and subsequent attempts to load additional bytes are ignored until the operation is completed.

Note that both the single byte and the automatic page programs can be entered after a proper "dummy" sequence of bytes has been loaded (see inadvertent write protection).



NOTES: 3. Upon the three-step sequence completion, the device is latched into programming mode. From 2 up to 64 bytes are latched at a rate of 1 μs up to 100 μs per byte.

4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).

5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.

Figure 2. Page Programming Flowchart — Entire Memory Algorithm

data polling

During a programming operation, the data polling software function is enabled to notify the host microcomputer that the memory is busy with programming and ignores any command until the programming operation is completed. If an attempt to read any byte occurs during the programming cycle, the device answers with the last loaded byte, but with the inverted logical value of DQ7. (See page 7-44 for data polling timing diagram.)

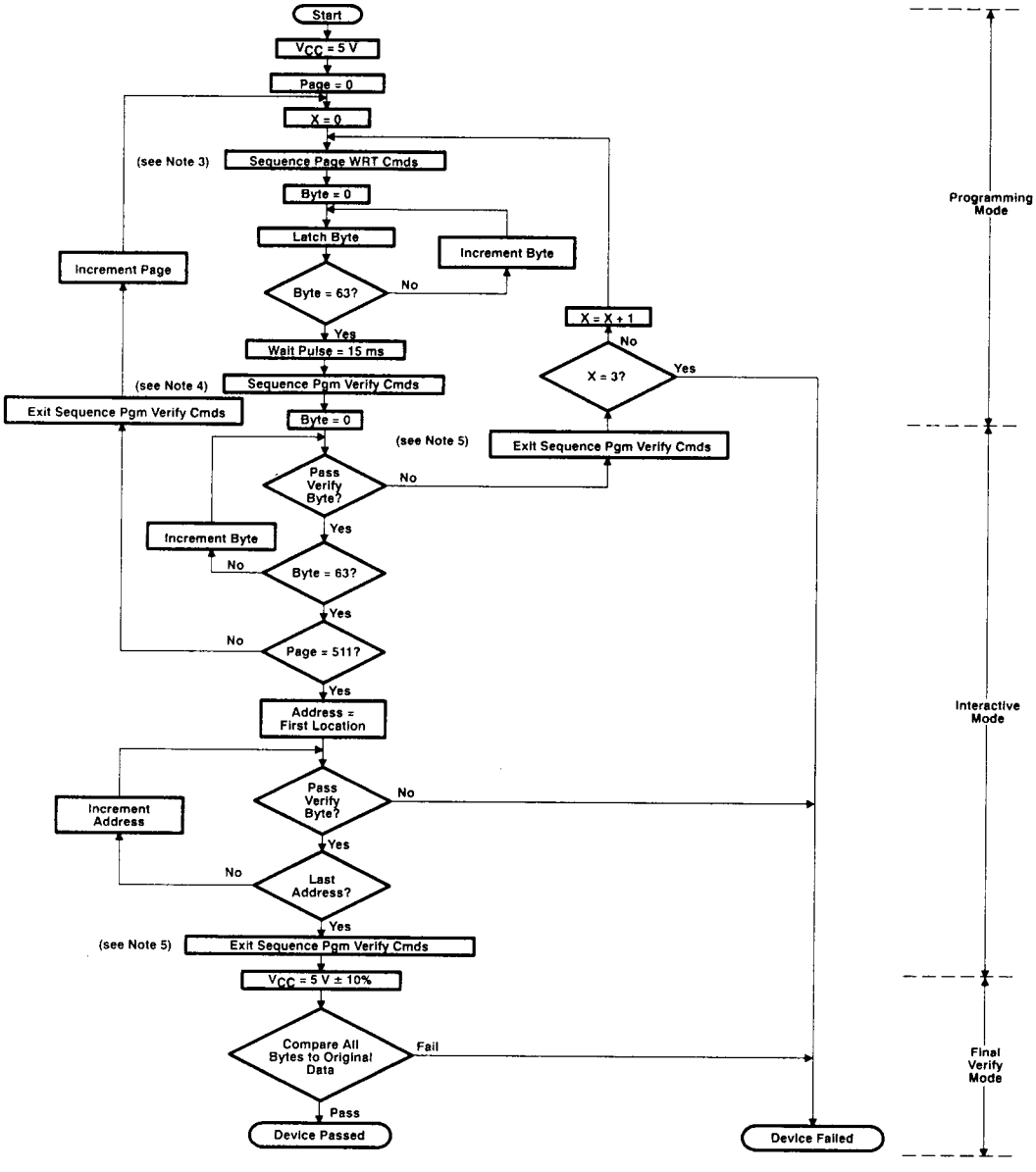
flash erase mode

The flash erase operation can be activated via software by loading a dummy sequence of data/address strings. The timing characteristics of this sequence are the same as those used for the page mode. The device detects this particular sequence and automatically starts the self-timed erase. If the sequence load cycle is longer than 100 μs, the device ignores it. This sequence should not be used in the actual software program to prevent inadvertent flash erase operations.

The specified dummy sequence to initiate the flash erase mode is:

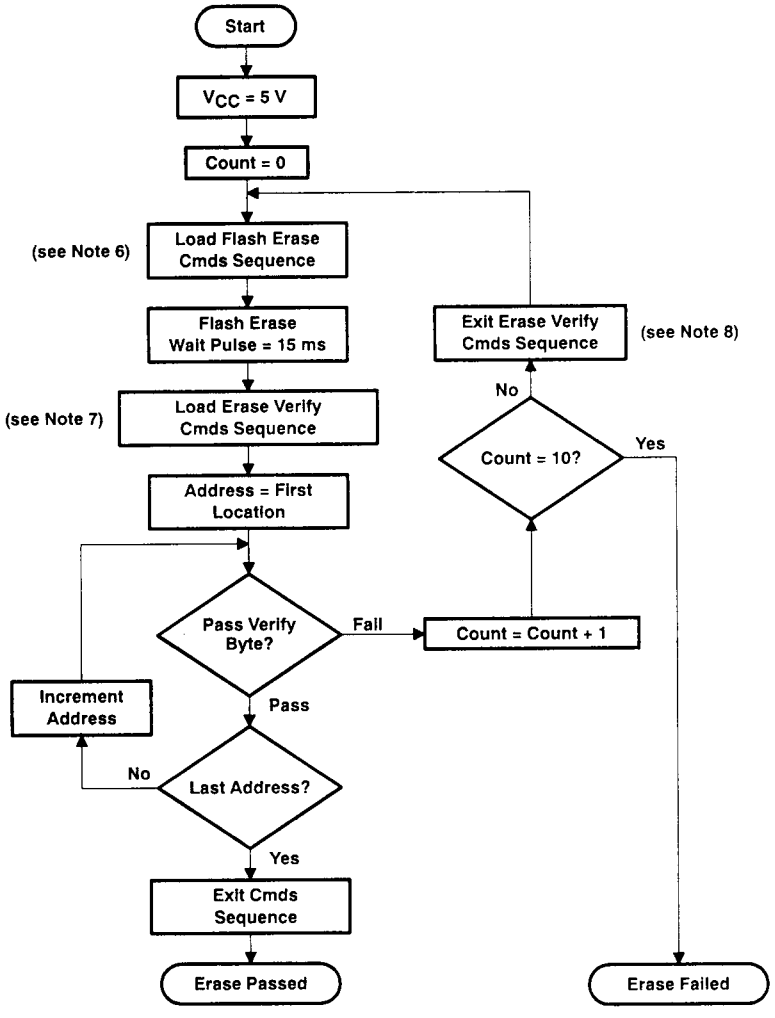
STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	80
4	Access Write	5555	AA
5	Access Write	2AAA	55
6	Access Write	5555	10

The self-timed flash erase mode starts automatically.



NOTES: 3. Upon the three-step sequence completion, the device is latched into programming mode. From 2 up to 64 bytes are latched at a rate of 1 μs up to 100 μs per byte.
4. Upon the three-step sequence completion, the device is latched into the program verify mode. All the bytes are read with a sense voltage of: (internal V_{sense} volt) + (program margin voltage).
5. Upon the three-step sequence completion, the device exits the program verify mode and returns to the page write setup.

Figure 3. Page Programming Flowchart — Standard Algorithm



NOTES: 6. The bulk-erase operation starts automatically once the six-step sequence is completed.
7. The device is latched into the Erase Verify mode once the three-step sequence is completed. All bytes are read with a sense voltage of: (internal V_{sense} voltage) — (erase margin voltage).
8. Upon the three-step sequence completion, the device is de-latched and returns to Flash operating setup.

Figure 4. Flash Erase Flowchart

signature mode

The signature mode provides access to two bytes contained in a spare row. One byte designates the manufacturer, the other byte designates the device code. The signature mode can be entered through either a hardware or a software operation.

The hardware entry mode is specified in the mode table in the description section. Setting the device in the read mode and applying V_H on pin A9 produces the manufacturer byte code at the I/O pins if A0 = V_{IL}, or the device identifier byte code if A0 = V_{IH}. The information provided by these two bytes helps the programmer select the proper programming algorithm.

The signature mode software entry sequence is specified as follows:

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	90

exit mode

The software exit sequence for any mode is specified as follows:

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	F0

program verify mode

The program verify mode allows the programmer to verify the adequacy of the programming.

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	B0

Upon completion of the three-step sequence, the device is latched into the program verify mode. All the bytes are read with a sense voltage of:

(internal V_{sense} voltage) + (program margin voltage)

The three access write (steps 1-3) are used only to enable the program verify mode: no data will actually be written to the device.

The software exit sequence must be applied to exit this program verify mode.

erase verify mode

The erase verify mode allows the programmer to verify the extent of erasure.

The device provides the following software sequence to access the erase verify mode:

STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	D0

Upon completion of the three-step sequence, the device is latched into erase verify mode. All the bytes are read with a sense voltage of:

(internal V_{sense} voltage) – (erase margin voltage)

The software exit sequence must be applied to exit this program verify mode.

Inadvertent write protection

The device is protected against write commands during power-up and power down. The protection is released only if V_{CC} is higher than 3 V. Moreover, the device provides a hardware and a software protection against inadvertent write commands that may occur even with a stable V_{CC}.

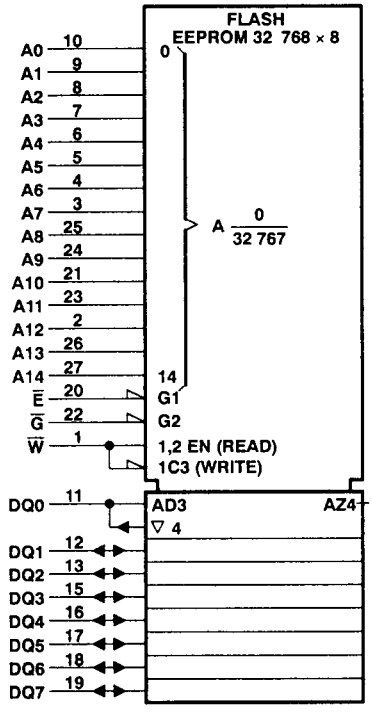
The hardware protection consists of noise immunity to a pulse on $\overline{W}$ shorter than 20 ns, which is unable to start a program cycle, and of a logic inhibit that prevents starting the program cycle unless the conditions of $\overline{W}$ low, $\overline{E}$ low, and $\overline{G}$ high are satisfied simultaneously.

The software protection is such that no program operation is enabled unless preceded by a sequence of three dummy write operations. Should the specified sequence not be loaded before any program operation or the sequence load cycle is longer than 100 μs, the device ignores the program commands.

The inadvertent write protection software sequence is specified as follows:

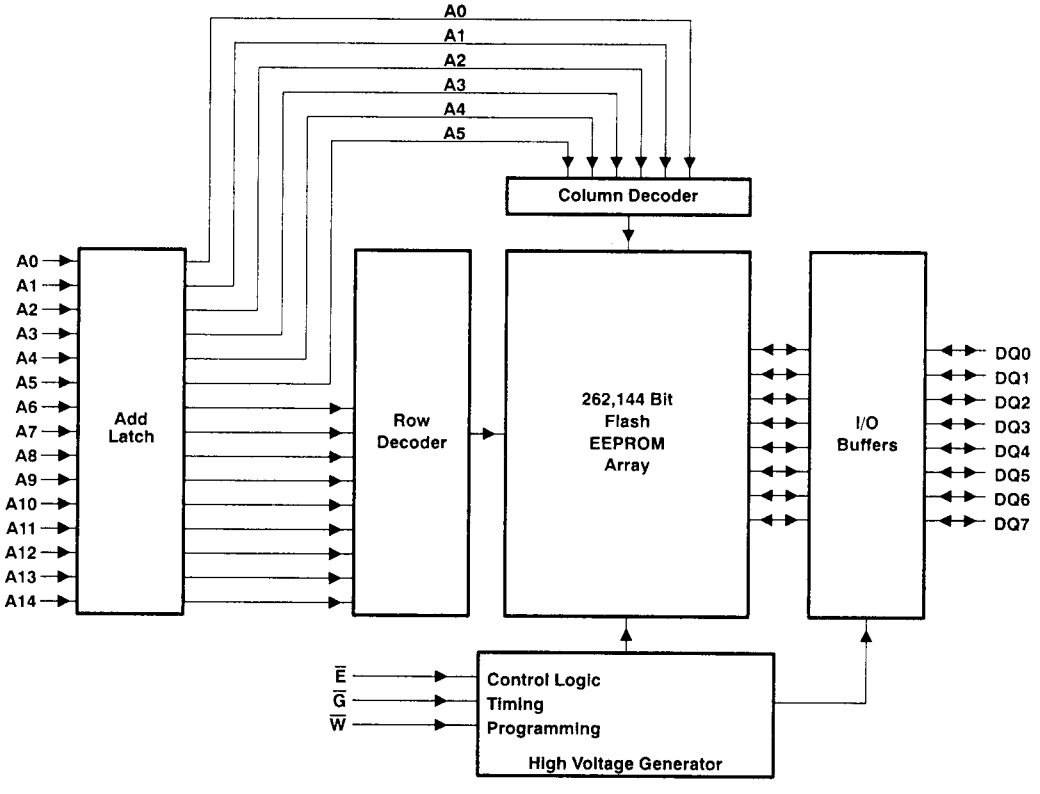
STEP	MODE	A14-A0	DQ7-DQ0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	A0
4	Page Program	page address + 1st byte address up to the 64th	1st data up to the 64th

logic symbol†



† This symbol is in accordance with ANSI/EEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the TMS29F256 J and N packages.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 9) ..... – 0.6 V to 7 V
Input voltage range: All except $\overline{G}$ and A9 ..... – 0.6 V to 6.5 V
$\overline{G}$ and A9 ..... 0.6 V to 15 V
Output voltage (see Note 9) ..... – 0.6 V to V_{CC} + 0.6 V
Operating free-air temperature range ('29F256-_ _ JL, JL4, NL, and FML;
'29F258-_ _ JL, JL4, NL, and FML; '29F259-_ _ JL, JL4, NL, and FML) ..... 0°C to 70°C
Operating free-air temperature range ('29F256-_ _ JE and JE4;
'29F258-_ _ JE and JE4; '29F259-_ _ JE and JE4) ..... – 40°C to 85°C
Operating free-air temperature range ('29F256-_ _ JQ and JQ4;
'29F258-_ _ JQ and JQ4; '29F259-_ _ JQ and JQ4) ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 9: All voltage values are with respect to the most negative supply voltage V_{SS} (substrate).

recommended operating conditions

			'29F256-170 '29F258-170 '29F259-170 '29F256-200 '29F258-200 '29F259-200		'29F256-250 '29F258-250 '29F259-250 '29F256-300 '29F258-300 '29F259-300	'29F256-20 '29F258-20 '29F259-20 '29F256-25 '29F258-25 '29F259-25		'29F256-30 '29F258-30 '29F259-30	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	−0.5		GND+0.2	
T_A	Operating free-air temperature	'29F256-_ _JL,JL4,NL,FML '29F258-_ _JL,JL4,NL,FML '29F259-_ _JL,JL4,NL,FML	0		70	0		70	°C
T_A	Operating free-air temperature	'29F256-_ _JE,JE4 '29F258-_ _JE,JE4 '29F259-_ _JE,JE4	−40		85	−40		85	°C
T_A	Operating free-air temperature	'29F256-_ _JQ,JQ4 '29F258-_ _JQ,JQ4 '29F259-_ _JQ,JQ4	−40		125	−40		125	°C

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	μA
		A9	V_I = 0 to 15 V			±50	
I_O	Output current (leakage)		V_O = 0.1 V to V_{CC}			±10	μA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		2	3.5	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		1.5	3	
I_{CC2}	V_{CC} average supply current (active read)		t_{cycle} = minimum cycle time, outputs open			15	mA
I_{CC3}	V_{CC} average supply current (active write)		t_{cycle} = 15 ms			10	mA

† Typical values are at T_A = 25° C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	6	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		8	12	pF

† Typical values are at T_A = 25°C and nominal voltage.
‡ Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

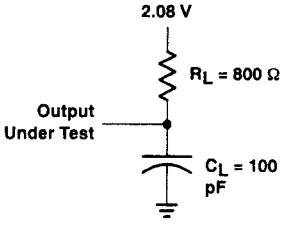
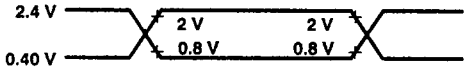


Figure 5. Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

switching characteristics over full ranges of recommended operating conditions†

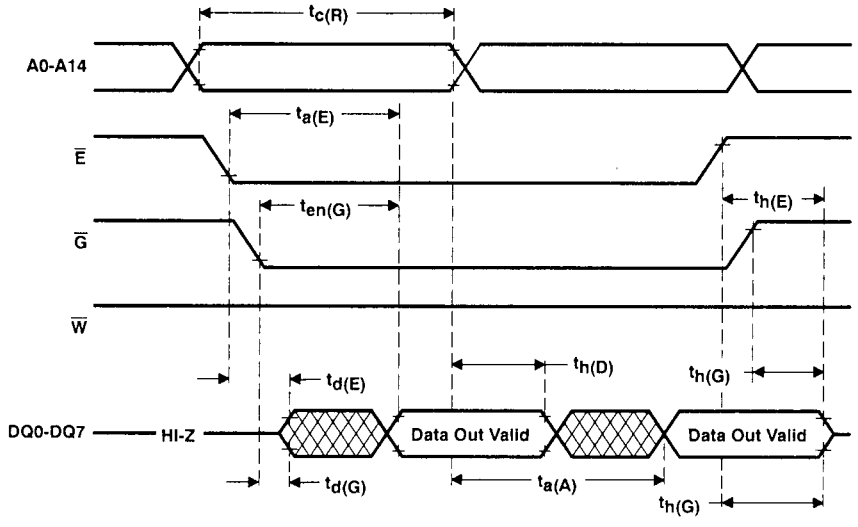
PARAMETER		'29F256-170 '29F258-170 '29F259-170		'29F256-200 '29F258-200 '29F259-200 '29F256-20 '29F258-20 '29F259-20		'29F256-250 '29F258-250 '29F259-250 '29F256-25 '29F258-25 '29F259-25		'29F256-300 '29F258-300 '29F259-300 '29F256-30 '29F258-30 '29F259-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		170		200		250		300	ns
$t_{a(E)}$	Access time from chip enable		170		200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		75		85		100		120	ns
$t_{c(R)}$	Read cycle time	170		200		250		300		ns
$t_{d(E)}$	Delay time, chip enable low to output	10	40	15	50	20	60	25	70	ns
$t_{d(G)}$	Delay time, output enable low to output	10	40	15	50	20	60	25	70	ns
$t_{h(E)}$	Hold time, chip enable to HI-Z output	10	40	15	50	20	60	25	70	ns
$t_{h(G)}$	Hold time, output enable to HI-Z output	10	40	15	50	20	60	25	70	ns
$t_{h(D)}$	Hold time, data valid to address	20	40	30	50	40	60	50	70	ns

† These parameters are guaranteed in regular read mode only.

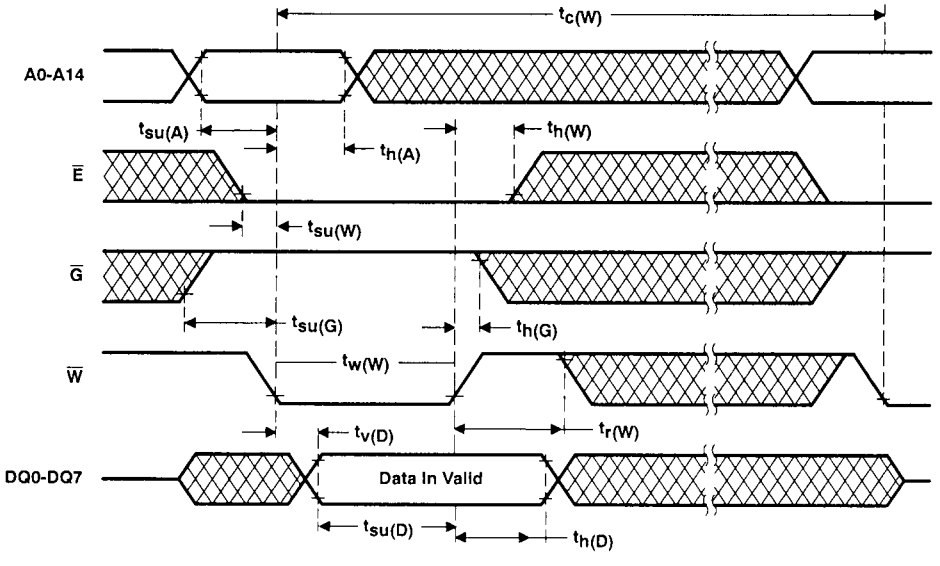
timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
$t_{c(W)}$	Write cycle time		15	ms
$t_{c(W)B}$	Byte load cycle time	1	100	µs
$t_{su(A)}$	Address setup time	10		ns
$t_{su(W)}$	Write setup time	0		ns
$t_{su(D)}$	Data setup time	80		ns
$t_{su(G)}$	Output enable setup time	10		ns
$t_{h(A)}$	Address hold time	150		ns
$t_{h(W)}$	Write hold time	0		ns
$t_{h(G)}$	Output enable hold time	10		ns
$t_{h(D)}$	Data hold time	10		ns
$t_{w(W)}$	Write pulse duration	200		ns
$t_{r(W)}$	Write high recovery time	800		ns
$t_{rec(W)}$	Write high recovery time in page mode	800		ns
$t_{r(E)}$	Chip enable high recovery time	800		ns
$t_{v(D)}$	Data valid time		300	µs
$t_{w(E)}$	Chip enable pulse duration	200		ns

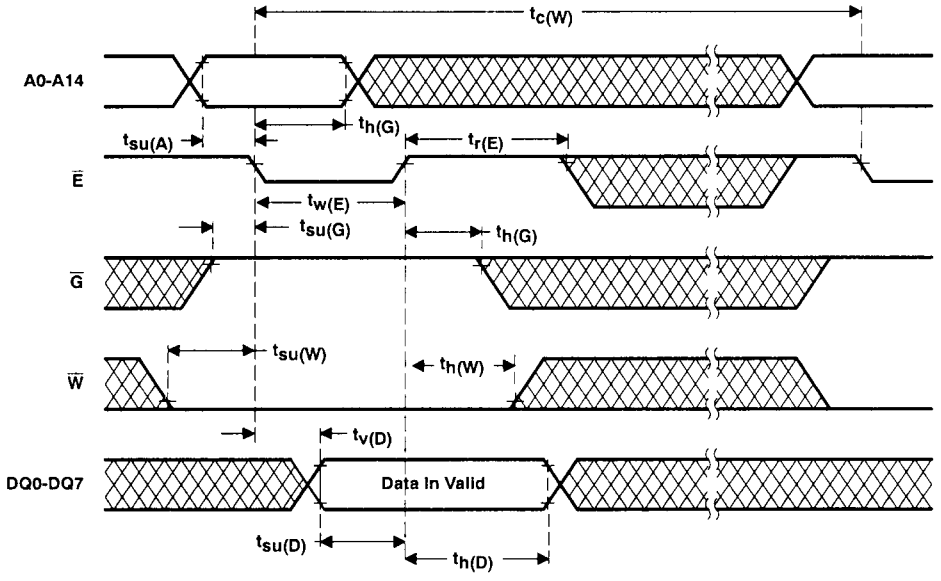
read cycle



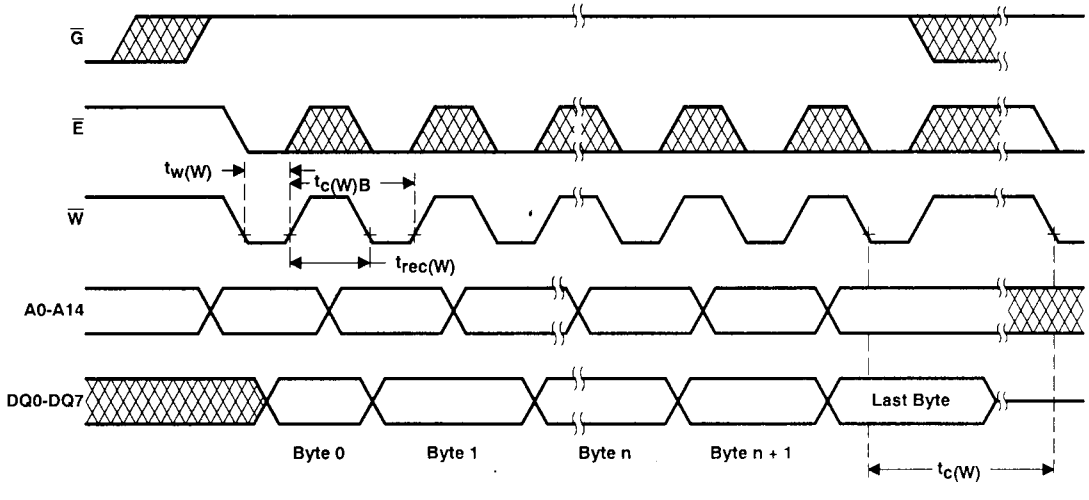
$\overline{W}$ controlled write cycle



$\overline{E}$ controlled write cycle



page write cycle



data polling