

TC74ACT139P, TC74ACT139F, TC74ACT139FN, TC74ACT139FT

DUAL 2 – TO – 4 LINE DECODER

The TC74ACT139 is an advanced high speed CMOS 2 to 4 LINE DECODER fabricated with silicon gate and double - layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

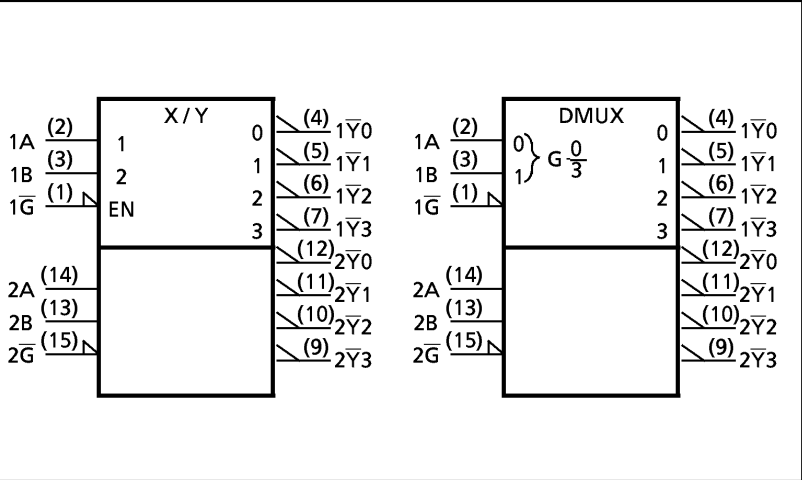
When the enable input is held “H” , all four outputs are fixed at a high logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

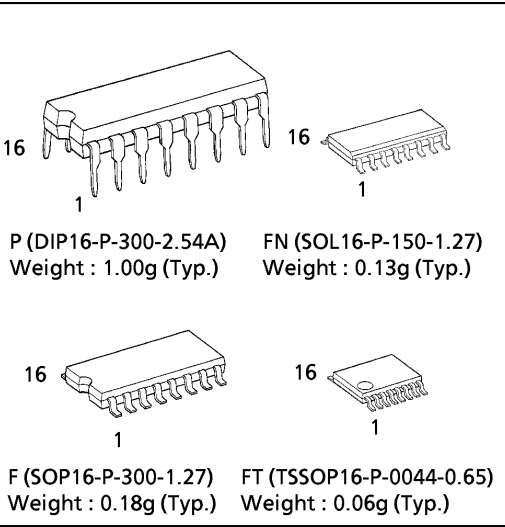
FEATURES :

- High Speed..... $t_{pd} = 5.5ns (typ.)$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A (Max.)$ at $T_a = 25^{\circ}C$
- Compatible with TTL outputs ... $V_{IL} = 0.8V (Max.)$
 $V_{IH} = 2.0V (Min.)$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24mA (Min.)$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F139

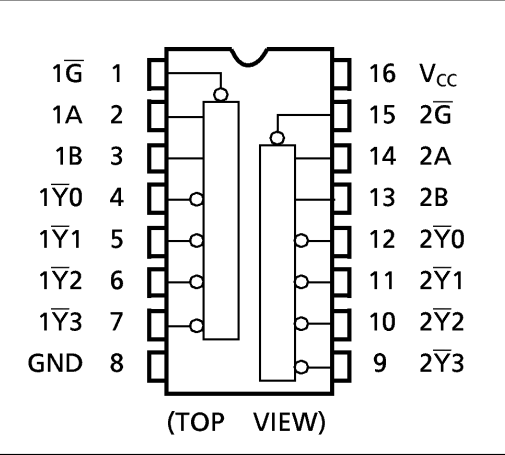
IEC LOGIC SYMBOL



(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT

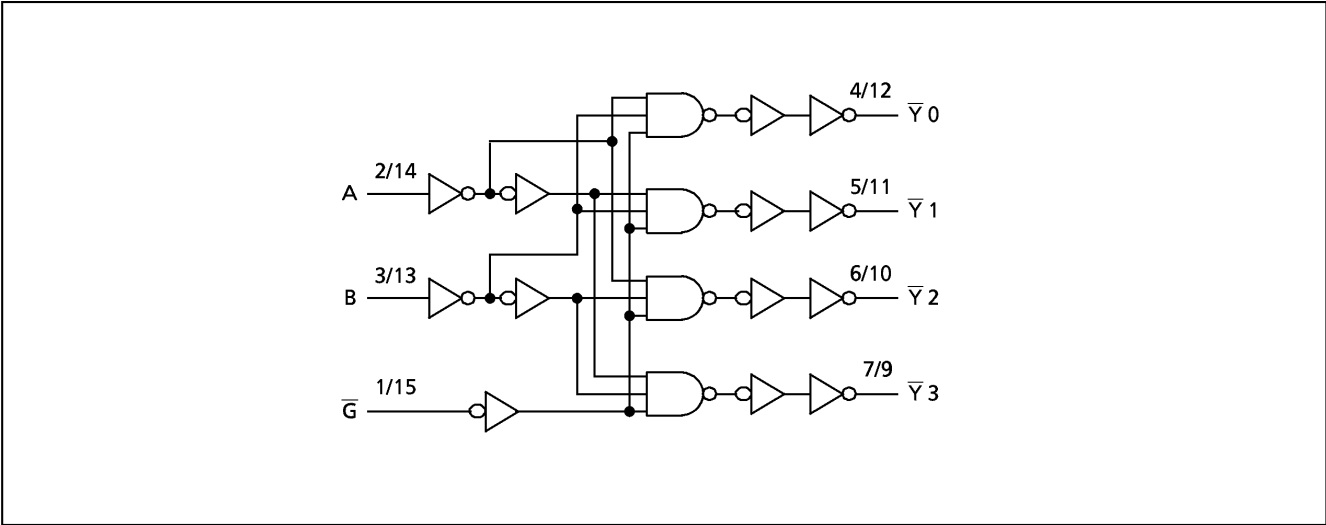


TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT		Y0	Y1	Y2	Y3	
G	B	A					
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	Y0
L	L	H	H	L	H	H	Y1
L	H	L	H	H	L	H	Y2
L	H	H	H	H	H	L	Y3

X : Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* /180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V _{IL}		4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	4.5	4.4	4.5	—	4.4	V
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	
			I _{OH} = -75mA*	5.5	—	—	—	3.85	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	4.5	—	0.0	0.1	—	V
			I _{OL} = 24mA	4.5	—	—	—	—	
			I _{OL} = 75mA*	5.5	—	—	—	—	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	
	I _C	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND	5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B - $\bar{Y}$)	t _{pLH}		5.0 ± 0.5	—	6.2	9.2	1.0	10.5	ns
	t _{pHL}		5.0 ± 0.5	—	6.3	9.6	1.0	11.0	
Propagation Delay Time ($\bar{G}$ - $\bar{Y}$)	t _{pLH} t _{pHL}		5.0 ± 0.5	—	6.3	9.6	1.0	11.0	ns
Input Capacitance	C _{IN}			—	5	10	—	10	
Power Dissipation Capacitance	C _{PD} (1)			—	51	—	—	—	pF

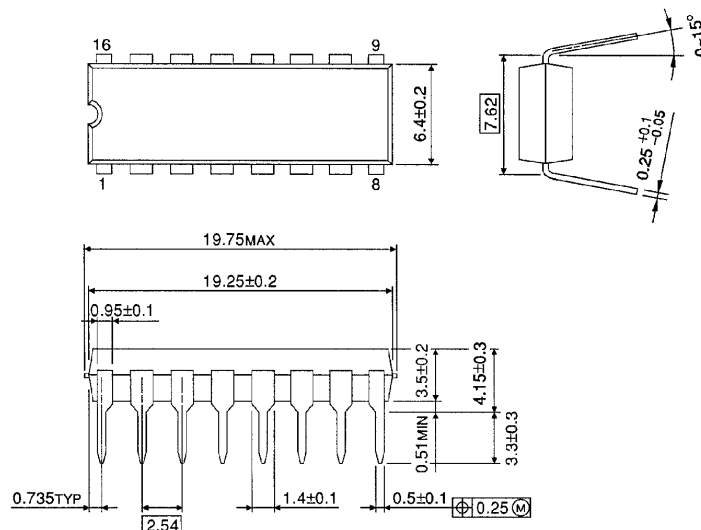
Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per Decoder)}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

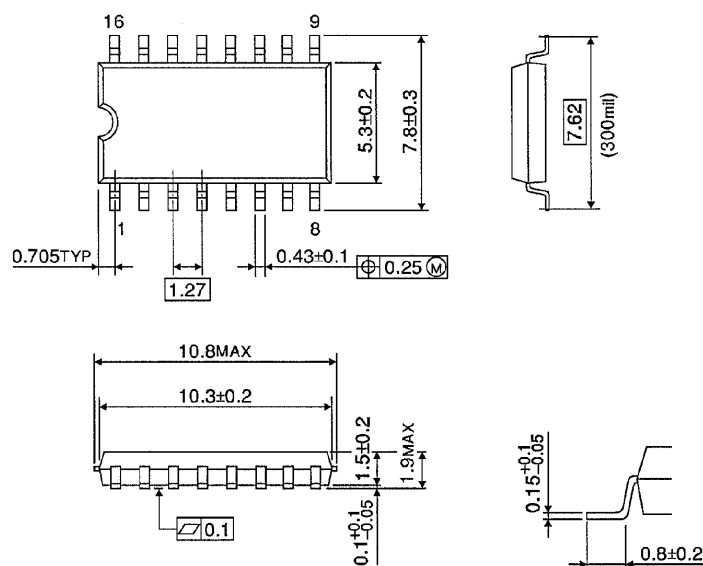
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

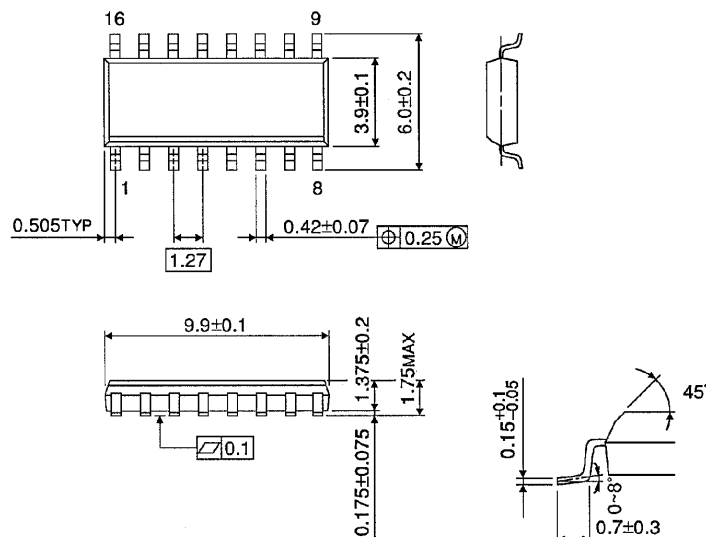


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

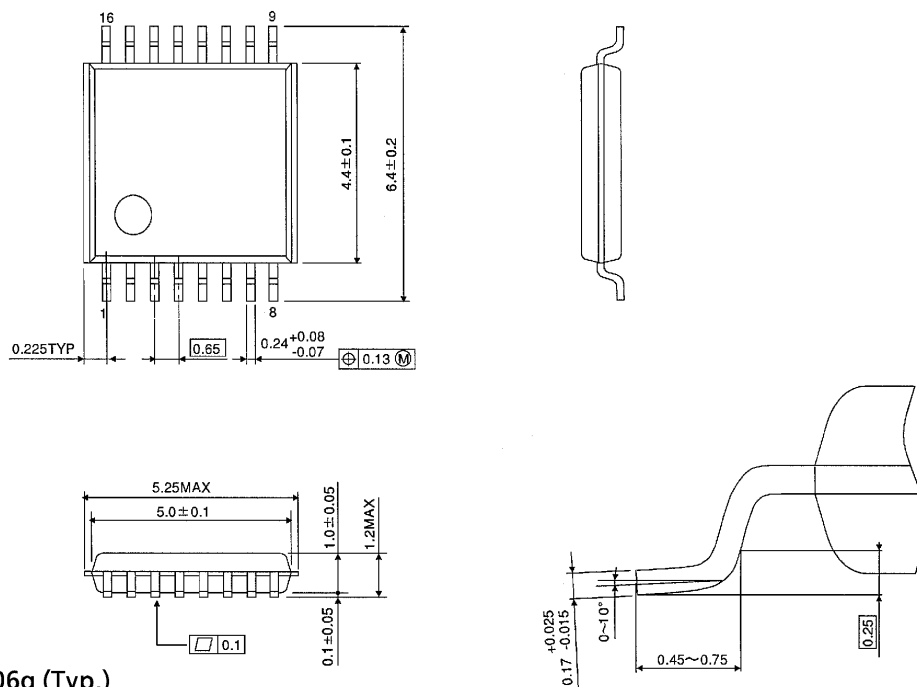
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

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000707EBA

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