

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS
131,072-WORD BY 16-BIT STATIC RAM

DESCRIPTION

The TC55V2161FTI is a 2,097,152-bit static random access memory (SRAM) organized as 131,072 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 3.6V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 85 ns. It is automatically placed in low-power mode at 1 μ A standby current (for the L-Version $V_{DD}=3V$, $T_a=25^\circ C$) when chip enable ($\overline{CE}$) is asserted high or chip select ($\overline{CS}$) is asserted low. There are three control inputs. $\overline{CE}$ is used to select the device and for data retention control, $\overline{CS}$ is used for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}, \overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to $85^\circ C$, the TC55V2161FTI can be used in environments exhibiting extreme temperature conditions. The TC55V2161FTI is available in a plastic 44-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.7 to 3.6V
- Power down features using $\overline{CE}$ and $\overline{CS}$
- Data retention supply voltage of 2 to 3.6V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to $85^\circ C$
- Standby current (maximum)

	TC55V2161FTI	
	-85, -10	-85L, -10L
3.6V	60 μA	40 μA
3.0V	50 μA	30 μA

- Access Times (maximum):

	TC55V2161FTI	
	-85, -85L	-10, -10L
Access Time	85 ns	100 ns
$\overline{CE}$ Access Time	85 ns	100 ns
$\overline{OE}$ Access Time	45 ns	50 ns

- Package:
TSOP II 44-P-400-0.80 (FT)

PIN ASSIGNMENT (TOP VIEW)

A4	1	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	$\overline{OE}$
A0	5	40	$\overline{UB}$
$\overline{CE}$	6	39	$\overline{LB}$
I/O1	7	38	I/O16
I/O2	8	37	I/O15
I/O3	9	36	I/O14
I/O4	10	35	I/O13
V_{DD}	11	34	GND
GND	12	33	V_{DD}
I/O5	13	32	I/O12
I/O6	14	31	I/O11
I/O7	15	30	I/O10
I/O8	16	29	I/O9
R/W	17	28	$\overline{CS}$
A15	18	27	A8
A14	19	26	A9
A13	20	25	A10
A12	21	24	A11
A16	22	23	NC

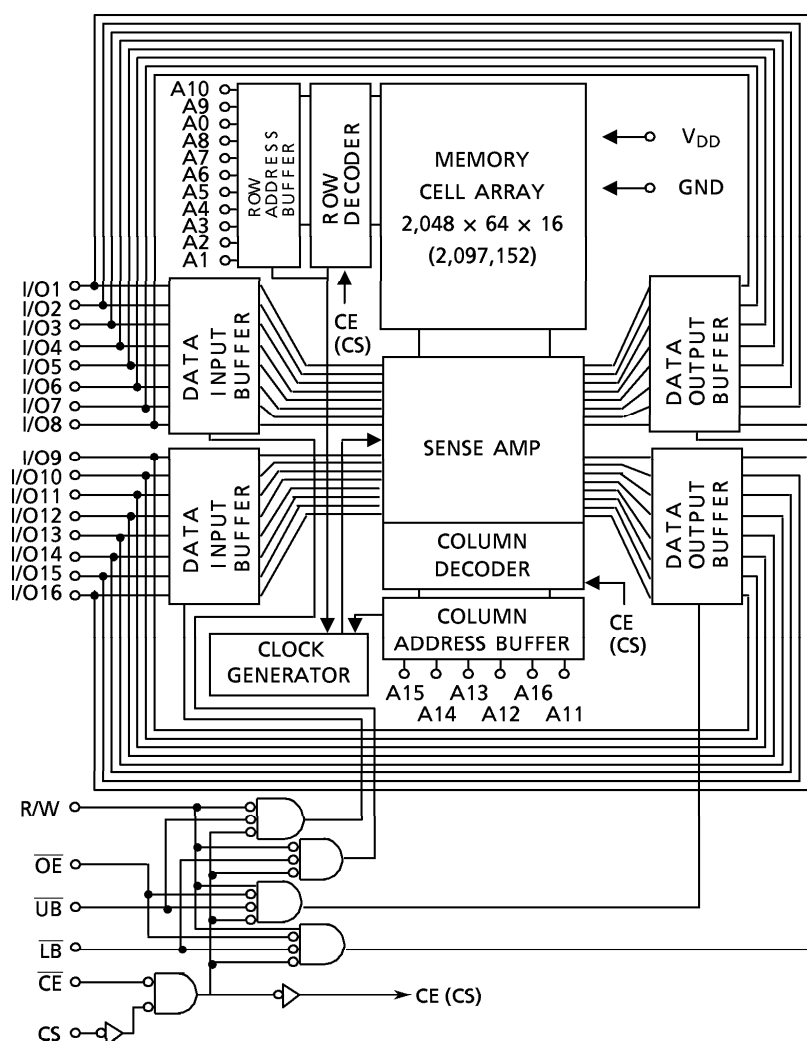
PIN NAMES

A0 to A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{CS}$	Chip Select Input
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}, \overline{UB}$	Data Byte Control Inputs
I/O1 to I/O16	Data Inputs / Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

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BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{\text{CE}}$	CS	$\overline{\text{OE}}$	R/W	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	H	L	H	L	L	D _{OUT}	D _{OUT}	I _{DDO}
					H	L	High-Z	D _{OUT}	I _{DDO}
					L	H	D _{OUT}	High-Z	I _{DDO}
Write	L	H	x	L	L	L	D _{IN}	D _{IN}	I _{DDO}
					H	L	High-Z	D _{IN}	I _{DDO}
					L	H	D _{IN}	High-Z	I _{DDO}
Output Deselect	L	H	H	H	x	x	High-Z	High-Z	I _{DDO}
			x	x	L	L			
CS Standby	x	L	x	x	x	x	High-Z	High-Z	I _{DDs}
Standby	H	x	x	x	x	x	High-Z	High-Z	I _{DDs}

Note: x = don't care. H = logic high. L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.3 to 4.6	V
V_{IN}	Input Voltage	- 0.3 * to 4.6	V
$V_{I/O}$	Input/Output Voltage	- 0.5 to $V_{DD} + 0.5$	V
P_D	Power Dissipation	0.8	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 55 to 150	°C
T_{opr}	Operating Temperature	- 40 to 85	°C

* - 3.0 V when measured at a pulse width of 30 ns

DC RECOMMENDED OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	2.7	-	3.6	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD} + 3.6$	V
V_{IL}	Input Low Voltage	- 0.3 *	-	0.6	V
V_{DH}	Data Retention Supply Voltage	2.0	-	3.6	V

* - 3.0 V when measured at a pulse width of 30 ns

DC CHARACTERISTICS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.7$ to 3.6V)

SYMBOL	PARAMETER	TEST CONDITION					MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}					–	–	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} – 0.5 V					– 0.5	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V					2.1	–	–	mA
I _{LO}	Output Leakage Current	C _E = V _{IL} or CS = V _{IH} or R/W = V _{IL} V _{OUT} = 0 V to V _{DD}					–	–	± 1.0	μA
I _{DDO1}	Operating Current	C _E = V _{IL} and CS = V _{IH} and R/W = V _{IH} and I _{OUT} = 0 mA Other Input = V _{IH} /V _{IL}	V _{DD} = 3 V ± 10%	T _{cycle}	min	–	–	55	mA	
1 μs					–	–	10			
I _{DDO2}			V _{DD} = 3.3 V ± 0.3 V	T _{cycle}	min	–	–	60		
					1 μs	–	–	12		
			C _E = 0.2 V and CS = V _{DD} – 0.2 V and R/W = V _{DD} – 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} – 0.2 V/0.2 V	V _{DD} = 3 V ± 10%	T _{cycle}	min	–	–		45
						1 μs	–	–		5
I _{DDS1}	C _E = V _{IH} or CS = V _{IL}	V _{DD} = 3.3 V ± 0.3 V	T _{cycle}	min	–	–	50			
				1 μs	–	–	6			
I _{DDS2} (Note)	Standby Current	C _E = V _{DD} – 0.2 V or CS = 0.2 V V _{DD} = 2.0 to 3.6 V	V _{DD} = 3V ± 10%	Ta = 25°C	–85, –10	–	1	2.5	μA	
–85L, –10L					–	0.5	1.2			
Ta = – 40° to 85°C				–85, –10	–	–	55			
				–85L, –10L	–	–	35			
V _{DD} = 3.3V ± 0.3V				Ta = 25°C	–85, –10	–	1.5	3		
					–85L, –10L	–	0.7	1.4		
Ta = – 40° to 85°C			–85, –10	–	–	60				
			–85L, –10L	–	–	40				
V _{DD} = 3V			Ta = 25°C	–85, –10	–	1	2			
				–85L, –10L	–	0.5	1			
			Ta = – 40° to 40°C	–85, –10	–	–	5			
				–85L, –10L	–	–	3			
			Ta = – 40° to 85°C	–85, –10	–	–	50			
				–85L, –10L	–	–	30			

Note: In standby mode with $\overline{CE} \geq V_{DD} - 0.2\text{ V}$, these limits are assured for the condition $CS \geq V_{DD} - 0.2\text{ V}$ or $CS \leq 0.2\text{ V}$.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.7$ to 3.6V)

READ CYCLE

SYMBOL	PARAMETER	TC55V2161FTI				UNIT
		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	–	100	–	ns
t _{ACC}	Address Access Time	–	85	–	100	
t _{CO}	Chip Enable Access Time	–	85	–	100	
t _{OE}	Output Enable Access Time	–	45	–	50	
t _{BA}	Data Byte Control Access Time	–	45	–	50	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{BE}	Data Byte Control Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	35	–	40	
t _{ODO}	Output Enable High to Output High-Z	–	35	–	40	
t _{BDO}	Data Byte Control High to Output High-Z	–	35	–	40	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V2161FTI				UNIT
		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	–	100	–	ns
t _{WP}	Write Pulse Width	60	–	60	–	
t _{CW}	Chip Enable to End of Write	75	–	80	–	
t _{BW}	Data Byte Control to End of Write	60	–	60	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	35	–	40	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

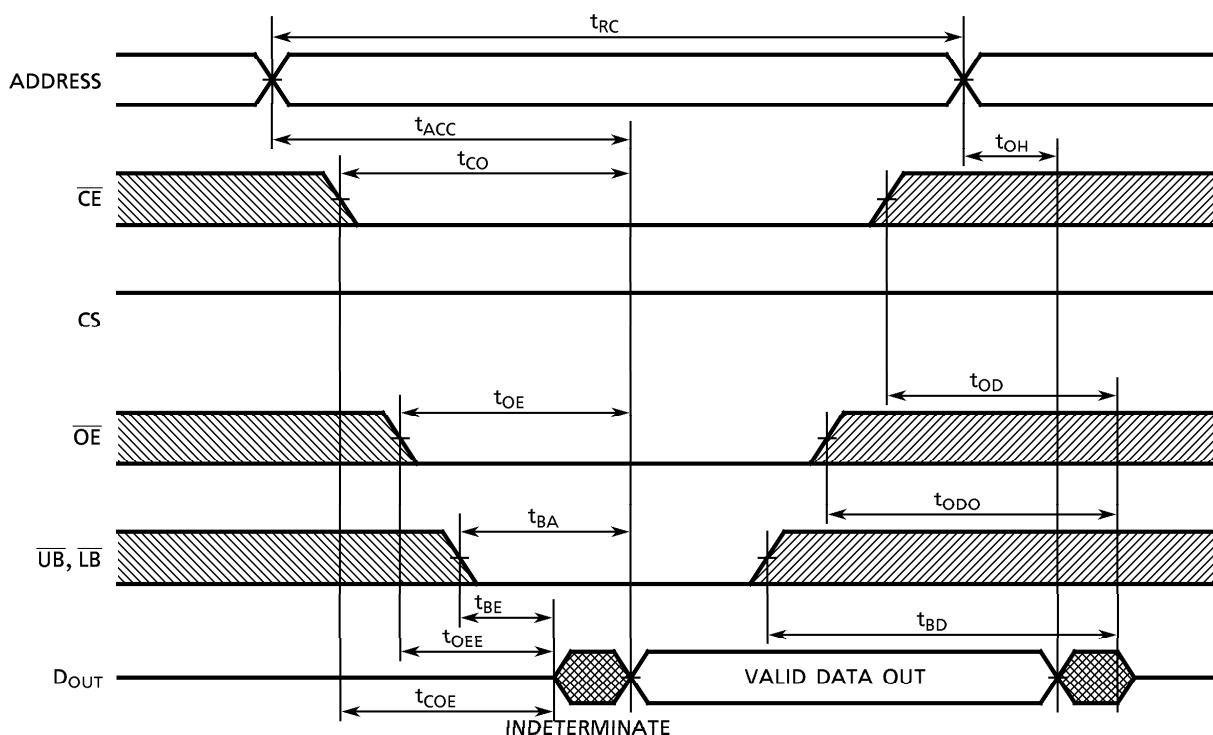
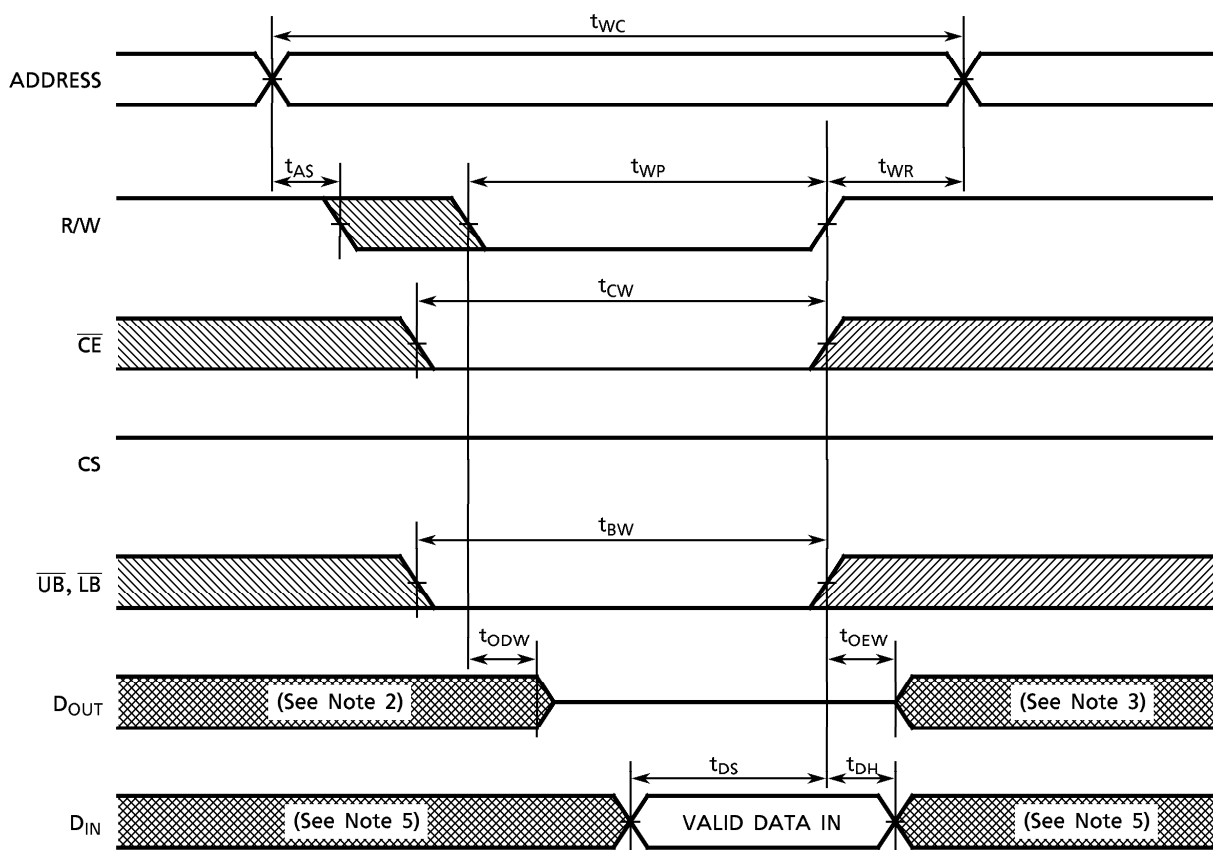
Output load: 100 pF + one TTL gate

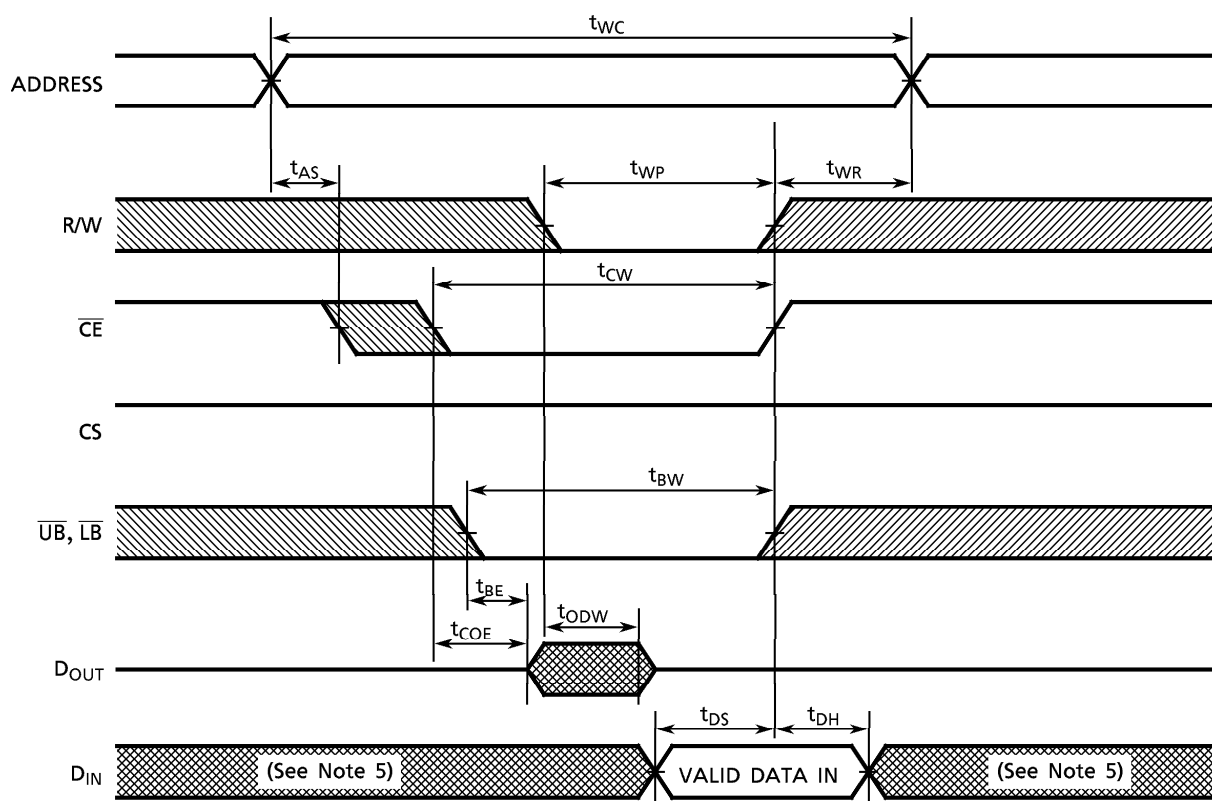
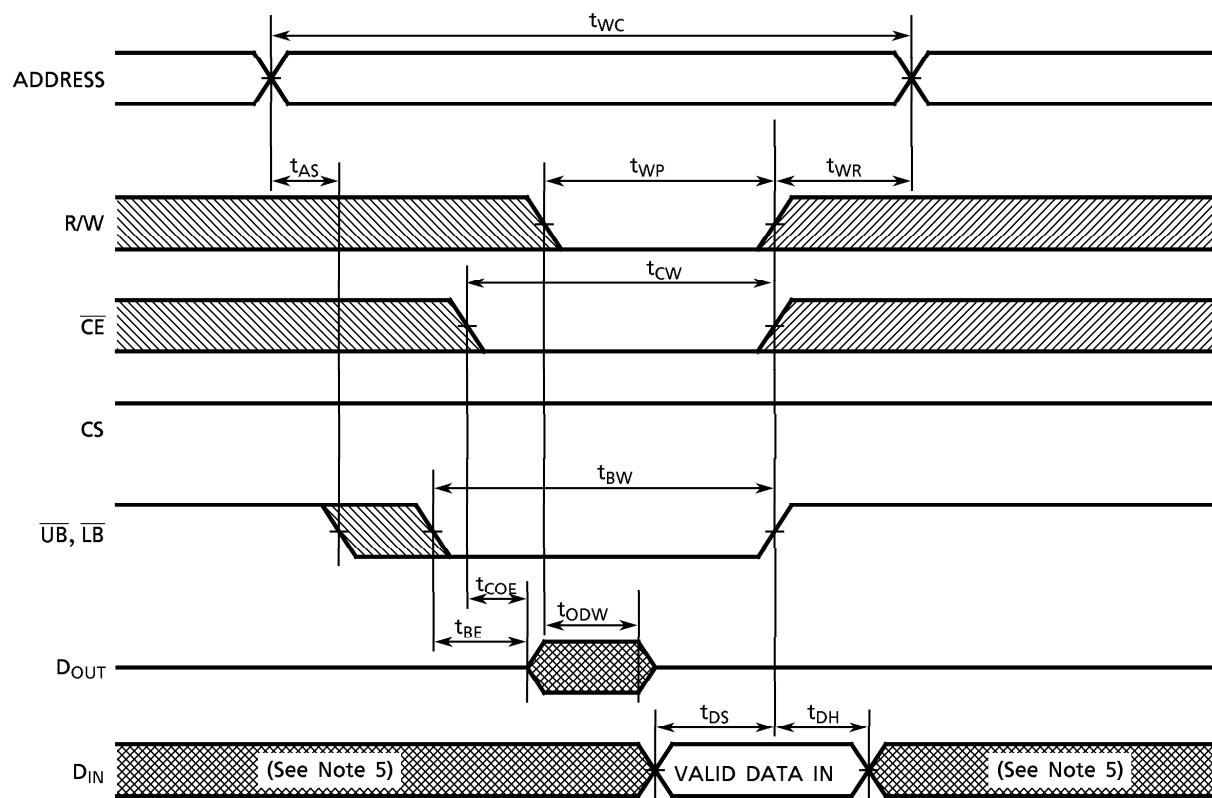
Input pulse level: 0.4 V, 2.4 V

Timing measurements: 1.5 V

Reference level: 1.5 V

t_R, t_F : 5 ns

TIMING DIAGRAMS
READ CYCLE (See Note 1)

WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)


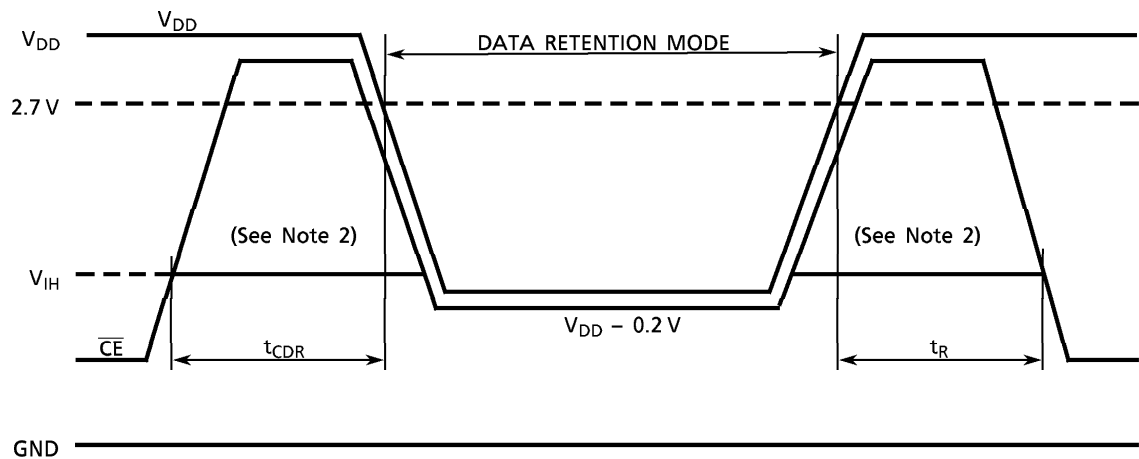
WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)

WRITE CYCLE 3 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)


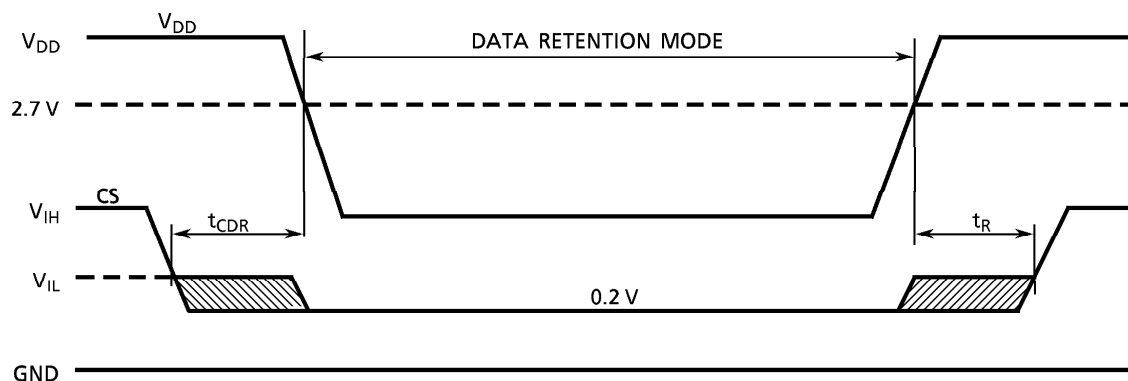
- Note:
- (1) R/W remains HIGH for the read cycle.
 - (2) If $\overline{CE}$ goes LOW (or CS goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
 - (3) If $\overline{CE}$ goes HIGH (or CS goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
 - (4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
 - (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER					MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage					2.0	–	3.6	V
I _{DDS2}	Standby Current	V _{DD} = 3.0 V	Ta = – 40° to 40°C	-85, -10	–	–	5	μA	
				-85L, -10L	–	–	3		
		V _{DD} = 3.0 V	Ta = – 40° to 85°C	-85, -10	–	–	50		
				-85L, -10L	–	–	35		
				-85, -10	–	–	60		
				-85L, -10L	–	–	45		
t _{CDR}	Chip Deselect to Data Retention Mode Time					0	–	–	nS
t _R	Recovery Time					5	–	–	mS

$\overline{CE}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE CONTROLLED DATA RETENTION MODE (See Note 3)

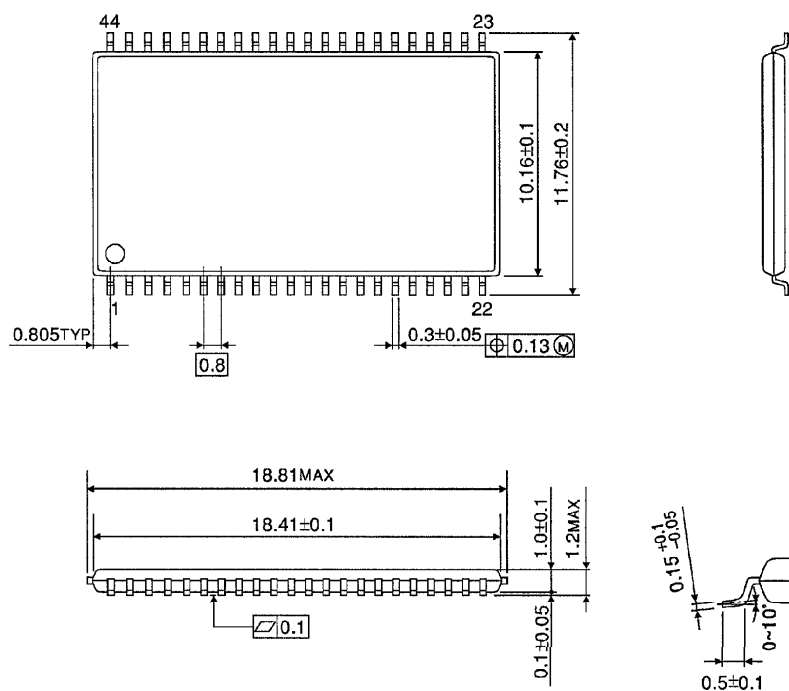
Note: (1) In $\overline{CE}$ controlled data retention mode, minimum standby current mode is entered when $CS \leq 0.2 \text{ V}$ or $CS \geq V_{DD} - 0.2 \text{ V}$.

(2) When $\overline{CE}$ is operating at the V_{IH} level (2.2 V), the operating current is given by I_{DDSI} during the transition of V_{DD} from 3.6 to 2.4 V.

(3) In CS controlled data retention mode, minimum standby current mode is entered when $CS \leq 0.2 \text{ V}$.

PACKAGE DIMENSIONS (TSOPII 44-P-400-0.80)

Units in mm



Weight: (typ)