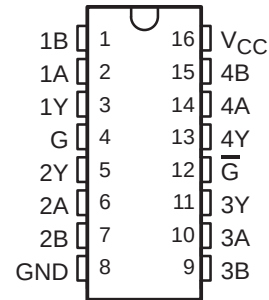


SN65LBC173, SN75LBC173 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11.
- Designed to Operate With Pulse Durations as Short as 20 ns
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Input Sensitivity . . . ± 200 mV
- Low-Power Consumption . . . 20 mA Max
- Open-Circuit Fail-Safe Design
- Pin Compatible With SN75173 and AM26LS32

D OR N PACKAGE
(TOP VIEW)



description

The SN65LBC173 and SN75LBC173 are monolithic quadruple differential line receivers with 3-state outputs. Both are designed to meet the requirements of the ANSI standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low.

Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of 12 V to -7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. Both devices are designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC173 and SN75LBC173 are available in the 16-pin DIP (N) and SOIC (D) packages.

The SN65LBC173 is characterized over the industrial temperature range of -40°C to 85°C . The SN75LBC173 is characterized for operation over the commercial temperature range of 0°C to 70°C .

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES G $\bar{G}$		OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



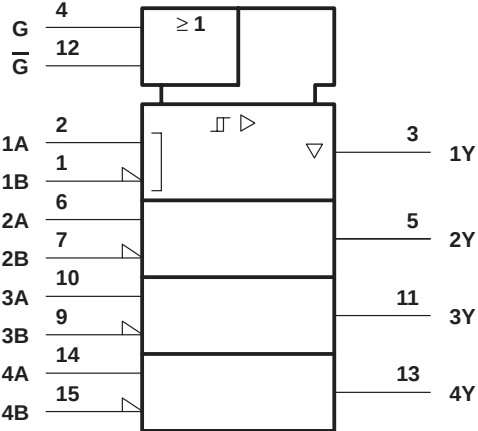
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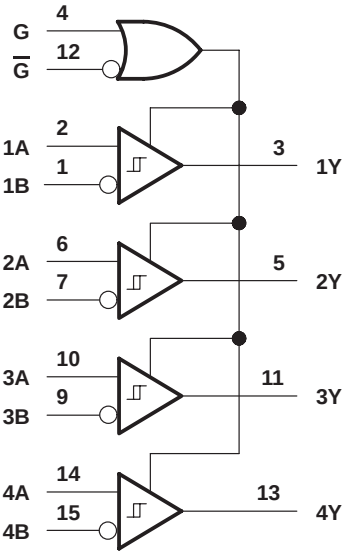
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logic symbol†

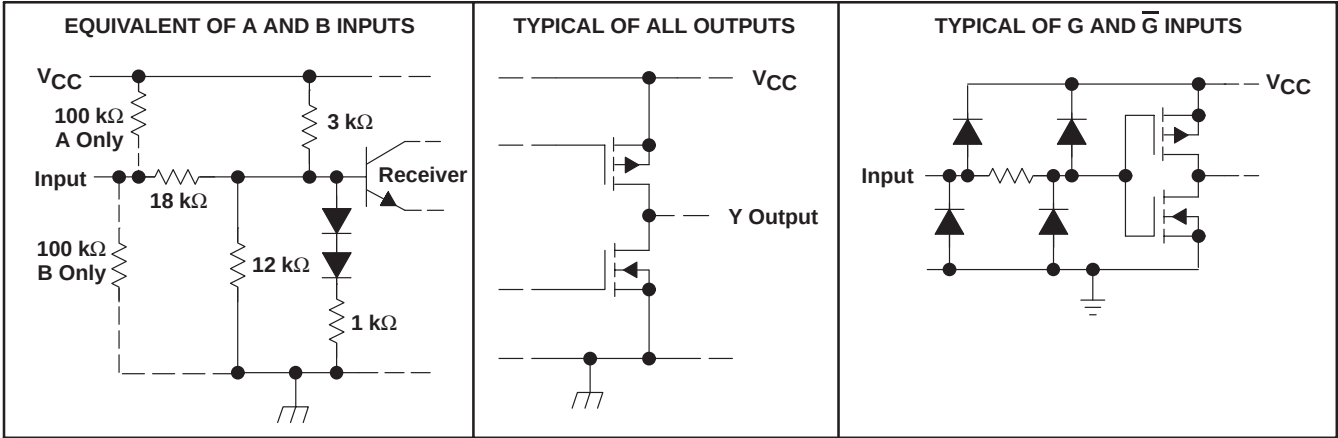


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Input voltage, V_I (A or B inputs)	± 25 V
Differential input voltage, V_{ID} (see Note 2)	± 25 V
Voltage range at Y, G, $\overline{G}$	–0.3 V to $V_{CC} + 0.5$ V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN65LBC173	–40°C to 85°C
SN75LBC173	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	1100 mW	8.7 mW/°C	708 mW	578 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		–7		12	V
Differential input voltage, V_{ID}				± 6	V
High-level input voltage, V_{IH}	G inputs	2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				–8	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65LBC173	–40		85	°C
	SN75LBC173	0		70	

SN65LBC173, SN75LBC173

QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8$ mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	$I_O = 16$ mA	-0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			45		mV
V_{IK}	Enable input clamp voltage	$I_I = -18$ mA		-0.9	-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA	3.5	4.5		V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 16$ mA	0.3	0.5		V
I_{OZ}	High-impedance-state output current	$V_O = 0$ V to V_{CC}			± 20	μ A
I_I	Bus input current	A or B inputs	$V_{IH} = 12$ V, $V_{CC} = 5$ V, Other inputs at 0 V	0.7	1	mA
			$V_{IH} = 12$ V, $V_{CC} = 0$ V, Other inputs at 0 V	0.8	1	mA
			$V_{IH} = -7$ V, $V_{CC} = 5$ V, Other inputs at 0 V	-0.5	-0.8	mA
			$V_{IH} = -7$ V, $V_{CC} = 0$ V, Other inputs at 0 V	-0.4	-0.8	mA
I_{IH}	High-level input current	$V_{IH} = 5$ V			± 20	μ A
I_{IL}	Low-level input current	$V_{IL} = 0$ V			-20	μ A
I_{OS}	Short-circuit output current	$V_O = 0$	-80	-120		mA
I_{CC}	Supply current	Outputs enabled, $I_O = 0$, $V_{ID} = 5$ V		11	20	mA
		Outputs disabled		0.9	1.4	

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output	11	22	30	ns
t_{PZH}	Output enable time to high level		17	30	ns
t_{PZL}	Output enable time to low level		18	30	ns
t_{PHZ}	Output disable time from high level		35	45	ns
t_{PLZ}	Output disable time from low level		25	40	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)		0.5	6	ns
t_t	Transition time		5	10	ns

PARAMETER MEASUREMENT INFORMATION

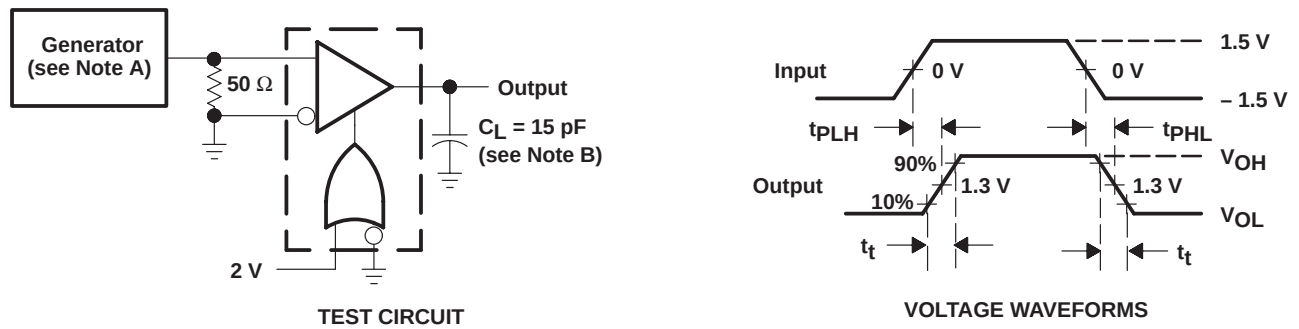
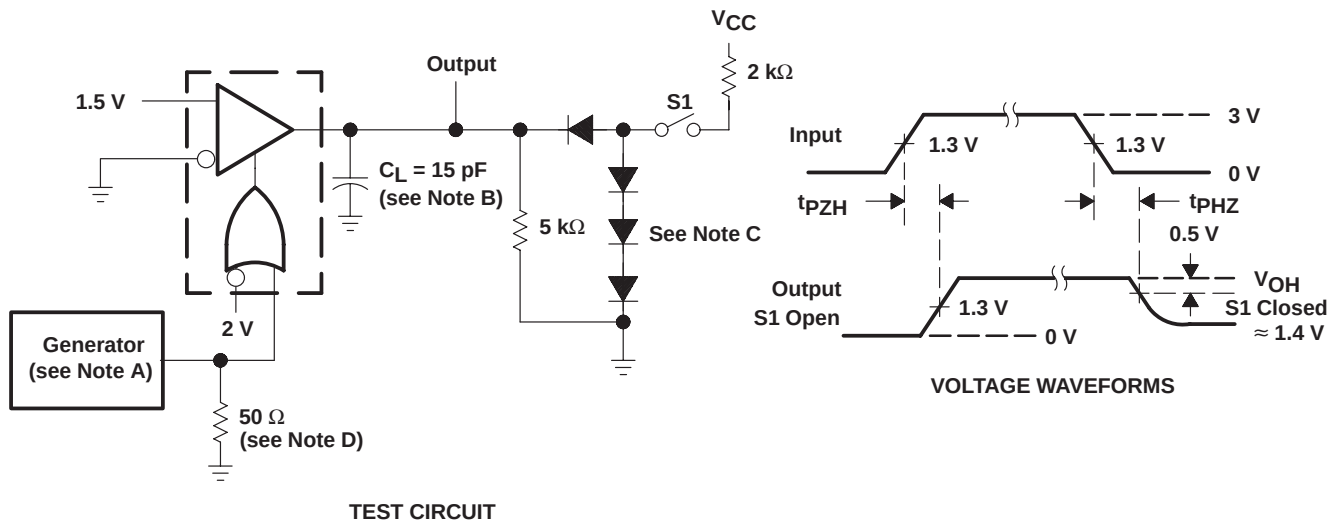


Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms



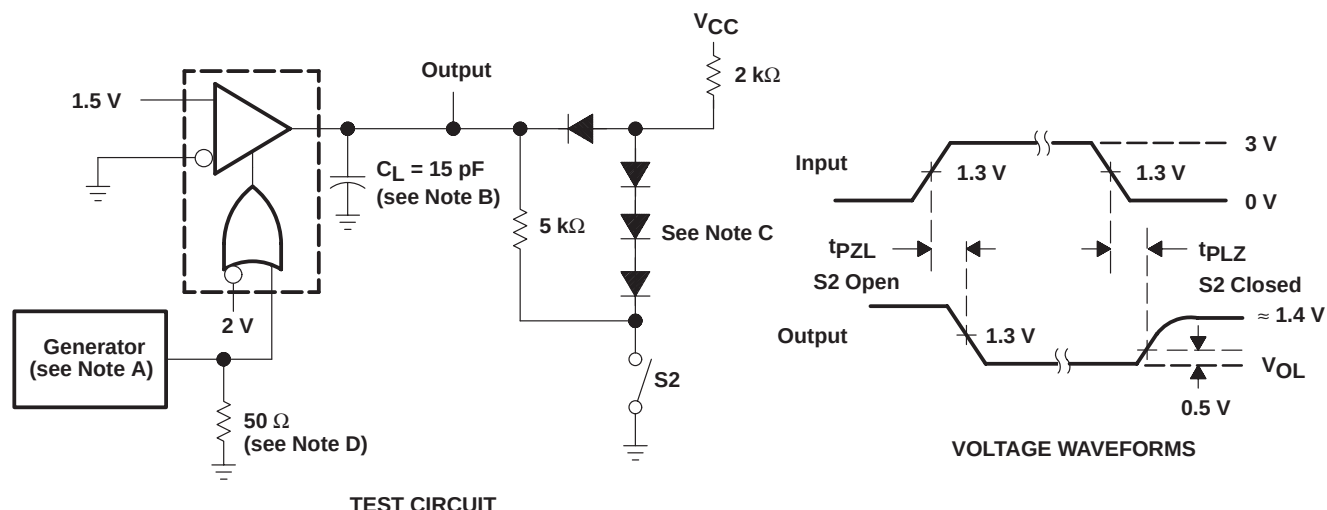
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable $\overline{G}$, ground $\overline{G}$ and apply an inverted input waveform to $\overline{G}$.

Figure 2. t_{pHZ} and t_{pZH} Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N916 or equivalent.
 D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

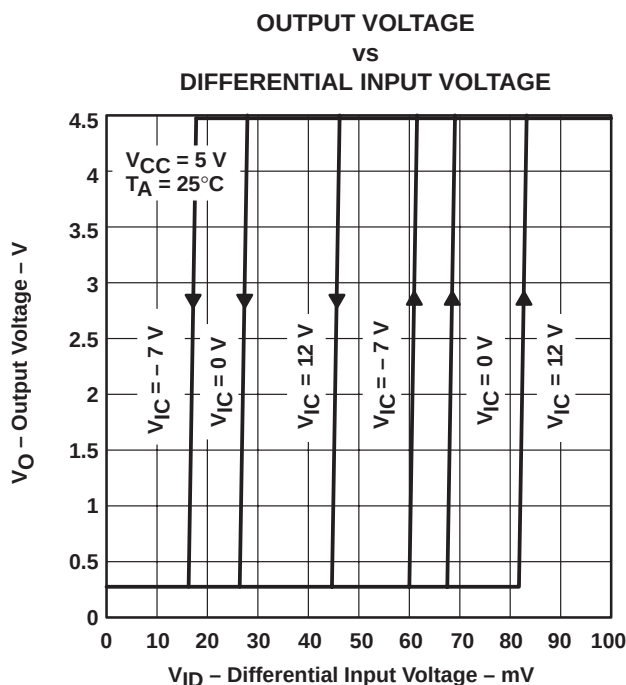


Figure 4

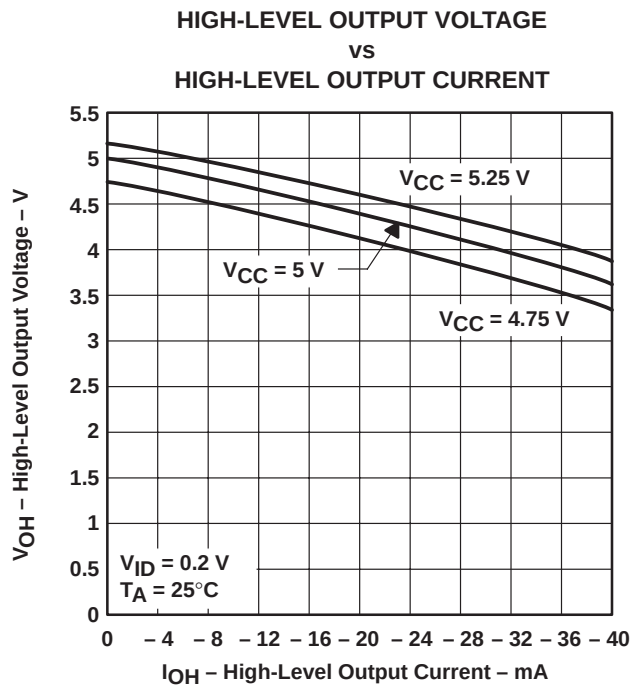


Figure 5

SN65LBC173, SN75LBC173 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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TYPICAL CHARACTERISTICS

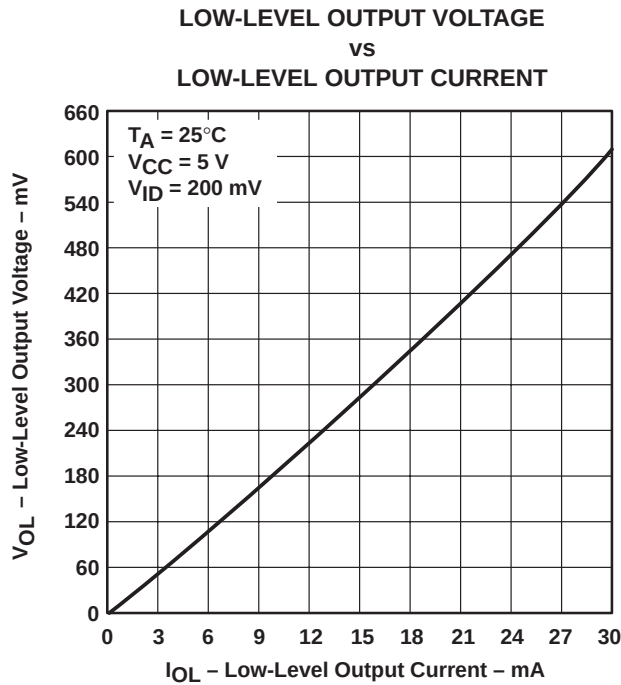


Figure 6

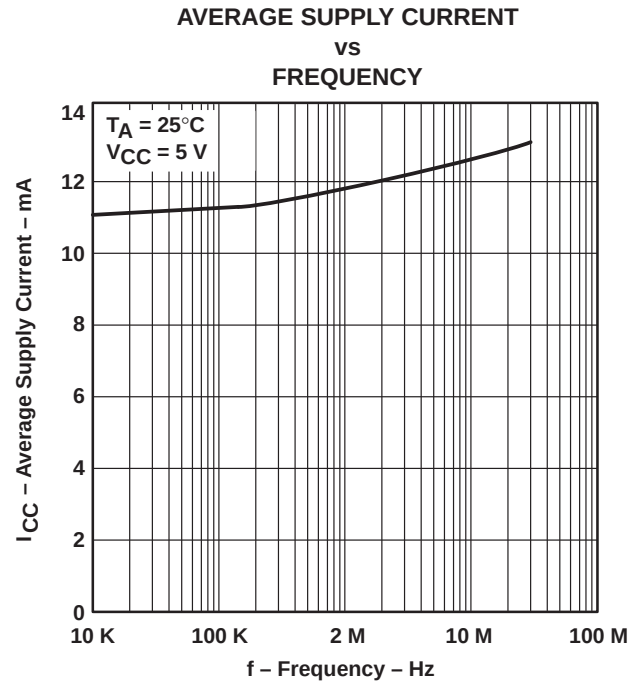


Figure 7

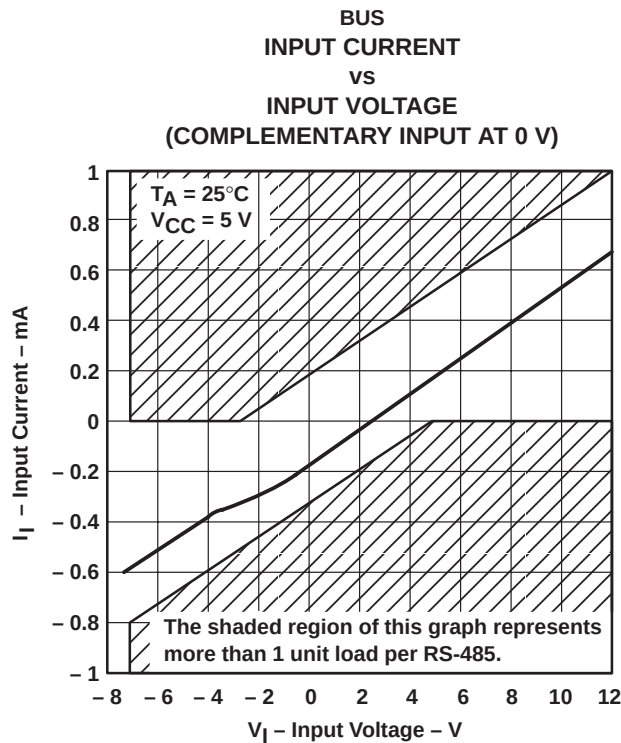


Figure 8

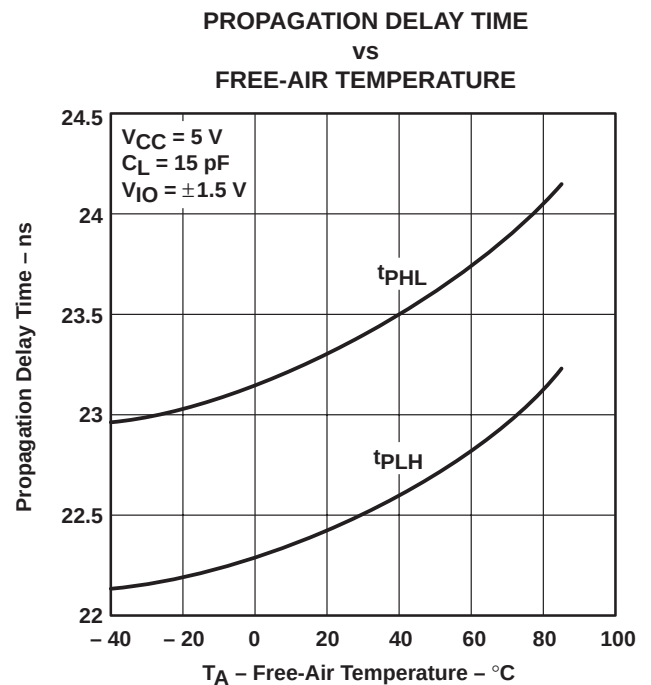


Figure 9

SN65LBC173, SN75LBC173
QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

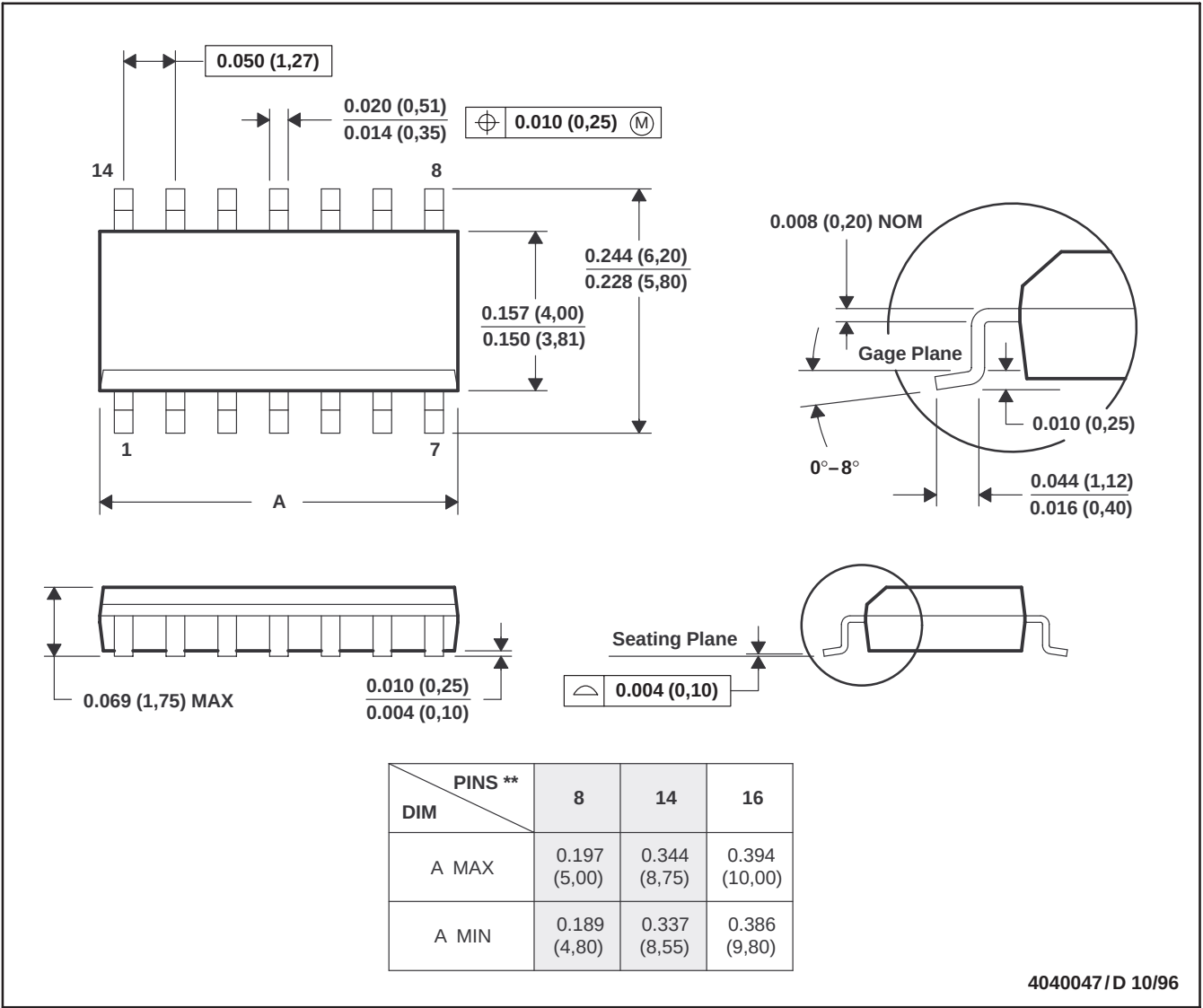
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

SN65LBC173, SN75LBC173 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

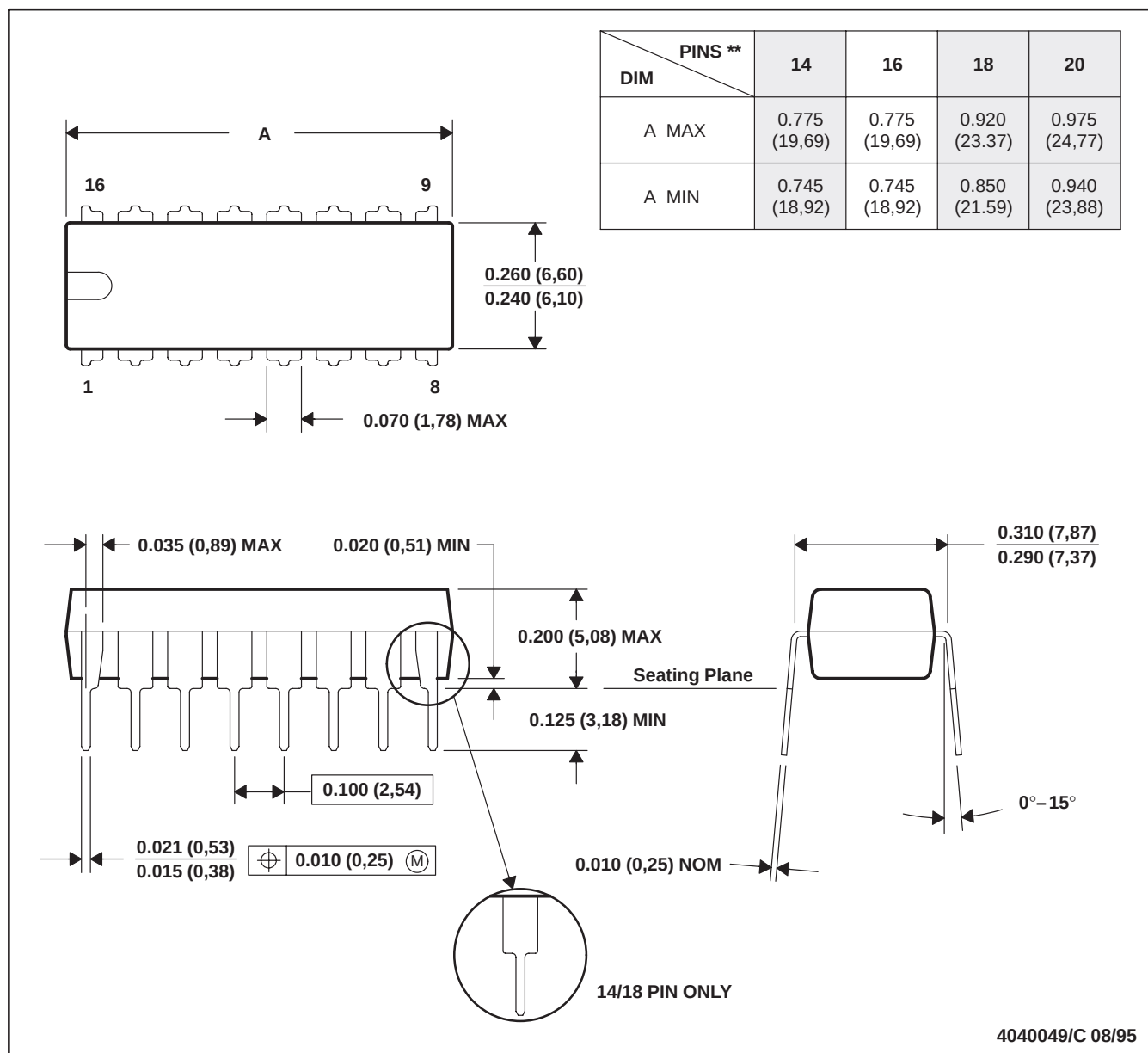
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MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

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