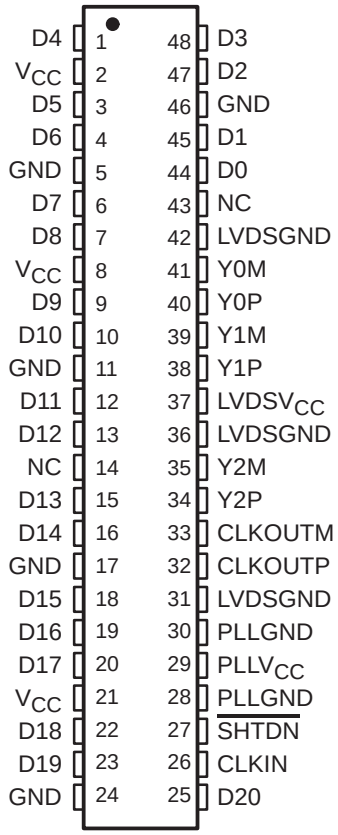
- **21:3 Data Channel Compression at up to 163 Million Bytes per Second Throughput**
- **Suited for SVGA, XGA, or SXGA Data Transmission From Controller to Display With Very Low EMI**
- **21 Data Channels Plus Clock In Low-Voltage TTL and 3 Data Channels Plus Clock Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant Data Inputs**
- **ESD Protection Exceeds 6 kV**
- **SN75LVDS84 Has Falling Clock-Edge Triggered Inputs, SN75LVDS85 Has Rising Clock-Edge-Triggered Inputs**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range: 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C561**

DGG PACKAGE
(TOP VIEW)



NC – Not Connected

description

The SN75LVDS84 and SN75LVDS85 FlatLink transmitters each contain three 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit. These functions allow 21 bits of single-ended low-voltage TTL (LVTTL) data to be synchronously transmitted over three balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 or SN75LVDS86.

When transmitting, data bits D0 – D20 are each loaded into registers of the SN75LVDS84 upon the falling edge and into the registers of the SN75LVDS85 on the rising edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times and then used to unload the data registers in 7-bit slices and serially. The three serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

AVAILABLE OPTIONS†

LATCHING CLOCK EDGE	
FALLING	**RISING**
SN75LVDS84DGG SN75LVDS84DGGR	SN75LVDS85DGG SN75LVDS85DGGR

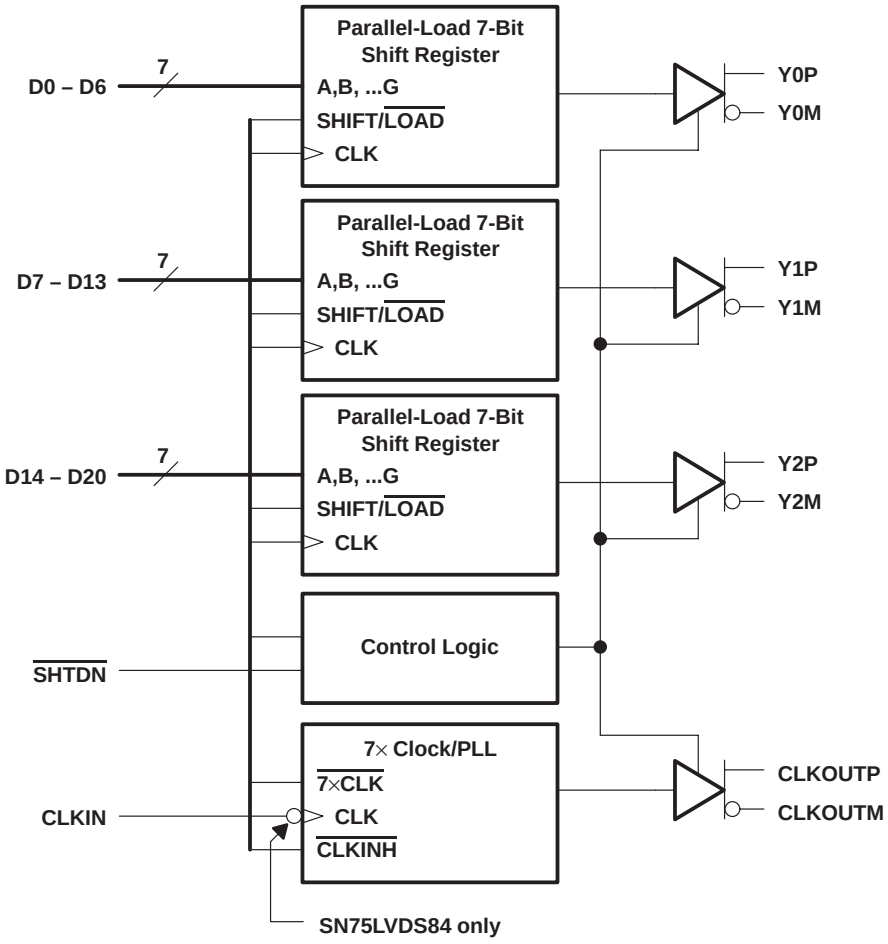
† The R suffix indicates taped and reeled packaging.

description (continued)

The SN75LVDS84 or SN75LVDS85 require no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS84 and SN75LVDS85 are characterized for operation over ambient free-air temperatures of 0°C to 70°C.

functional block diagram



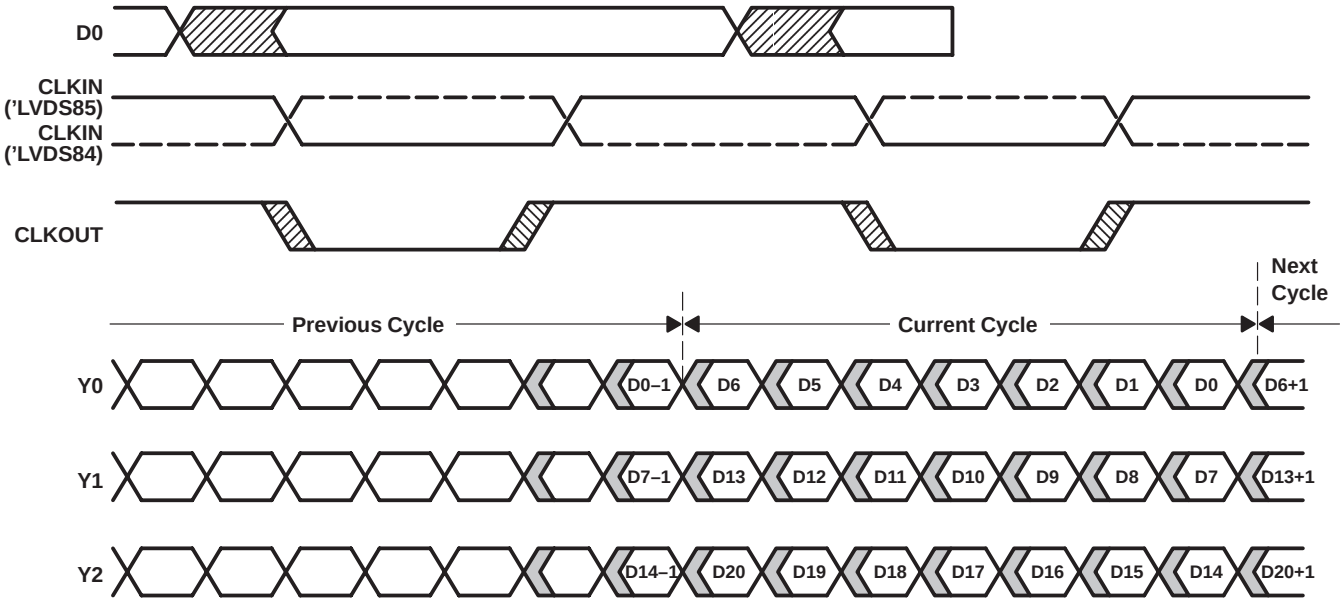
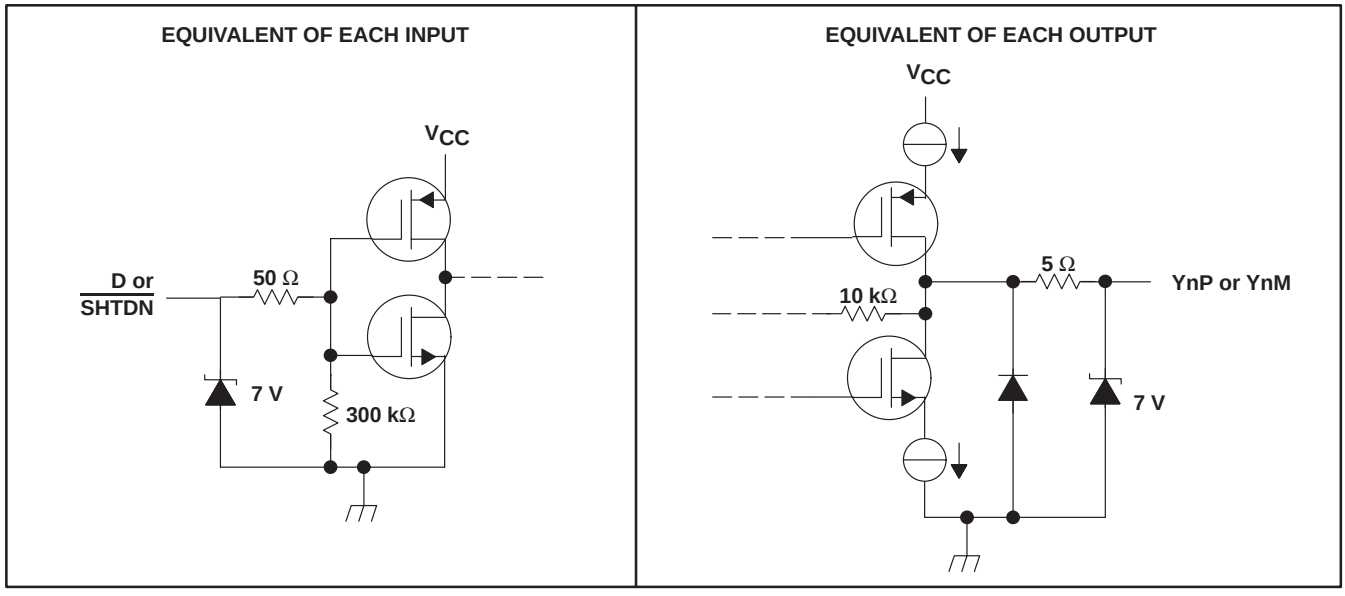


Figure 1. Load and Shift Timing Sequences

schematics of input and output



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Output voltage range, V_O (all terminals) . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (all terminals) . . . . . –0.5 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	1316 mW	13.1 mW/°C	726 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Differential load impedance, Z_L	90		132	Ω
Operating free-air temperature, T_A	0		70	°C

timing requirements

		MIN	NOM	MAX	UNIT
t_c	Input clock period	14.7		32.4	ns
t_w	Pulse duration, high-level input clock	$0.4t_c$		$0.6t_c$	ns
t_t	Transition time, input signal			5	ns
t_{su}	Setup time, data, D0 – D27 valid before CLKIN↓ (’84) or CLKIN↑ (’85) (See Figure 2)	3			ns
t_h	Hold time, data, D0 – D27 valid after CLKIN↓ (’84) or CLKIN↑ (’85) (See Figure 2)	1.5			ns

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT}	Input threshold voltage			1.4		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω, See Figure 3	247		454	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states				50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$			20	µA
I_{IL}	Low-level input current	V_{IL} = 0			±10	µA
I_{OS}	Short-circuit output current	$V_{O(Yn)}$ = 0			±24	mA
		V_{OD} = 0			±12	mA
I_{OZ}	High-impedance output current	V_O = 0 to V_{CC}			±10	µA
$I_{CC(AVG)}$	Quiescent supply current (average)	Disabled, All inputs at GND			280	µA
		Enabled, R_L = 100 Ω (4 places) Gray-scale pattern (see Figure 4), V_{CC} = 3.3 V, t_c = 15.38 ns		68	80	mA
		Enabled, R_L = 100 Ω, (4 places) Worst-case pattern (see Figure 5), t_c = 15.38 ns		75	100	mA
C_I	Input capacitance			3		pF

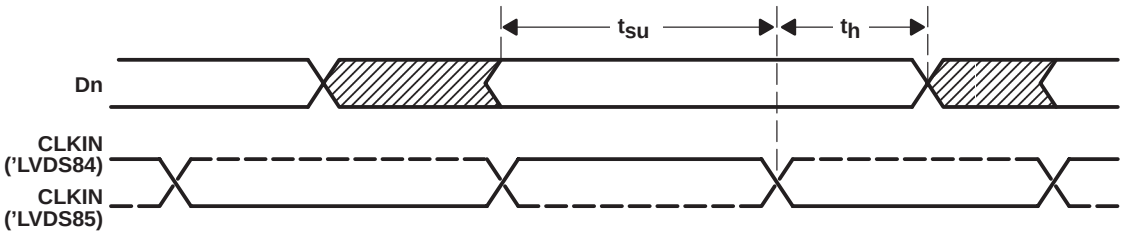
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{d0}	Delay time, CLKOUT↑ to serial bit position 0	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps‡, See Figure 6	–0.2	0	0.2	ns
t_{d1}	Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_c$ – 0.2		$\frac{1}{7}t_c$ + 0.2	ns
t_{d2}	Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_c$ – 0.2		$\frac{2}{7}t_c$ + 0.2	ns
t_{d3}	Delay time, CLKOUT↑ to serial bit position 3		$\frac{3}{7}t_c$ – 0.2		$\frac{3}{7}t_c$ + 0.2	ns
t_{d4}	Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_c$ – 0.2		$\frac{4}{7}t_c$ + 0.2	ns
t_{d5}	Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_c$ – 0.2		$\frac{5}{7}t_c$ + 0.2	ns
t_{d6}	Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_c$ – 0.2		$\frac{6}{7}t_c$ + 0.2	ns
$t_{sk(o)}$	Output skew, $t_n - \frac{n}{7}t_c$		–0.2		0.2	ns
t_{d7}	Delay time, CLKIN↓ to CLKOUT↑	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps‡, See Figure 6		4.2		ns
$\Delta t_{c(o)}$	Cycle time, Output clock jitter§	t_c = 15.38 + 0.75 sin (2π500E3t) ± 0.05 ns, See Figure 7		±70		ps
		t_c = 15.38 + 0.75 sin (2π3E6t) ± 0.05 ns, See Figure 7		±187		ps
t_w	Pulse duration, high-level output clock			$\frac{4}{7}t_c$		ns
t_t	Transition time, differential output voltage (t_r or t_f)	See Figure 3	260	700	1500	ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$↑ to phase lock (Yn valid)	See Figure 8		1		ms
t_{dis}	Disable time, $\overline{\text{SHTDN}}$↓ to off state (CLKOUT low)	See Figure 9		250		ns

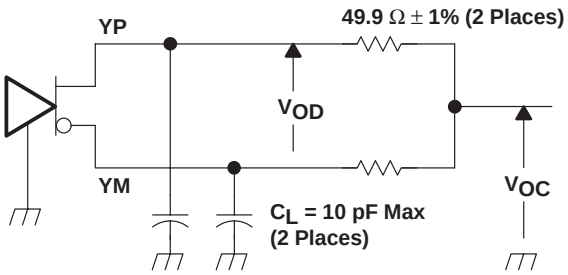
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ |Input clock jitter| is the magnitude of the change in the input clock period.
§ Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Definition



NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.

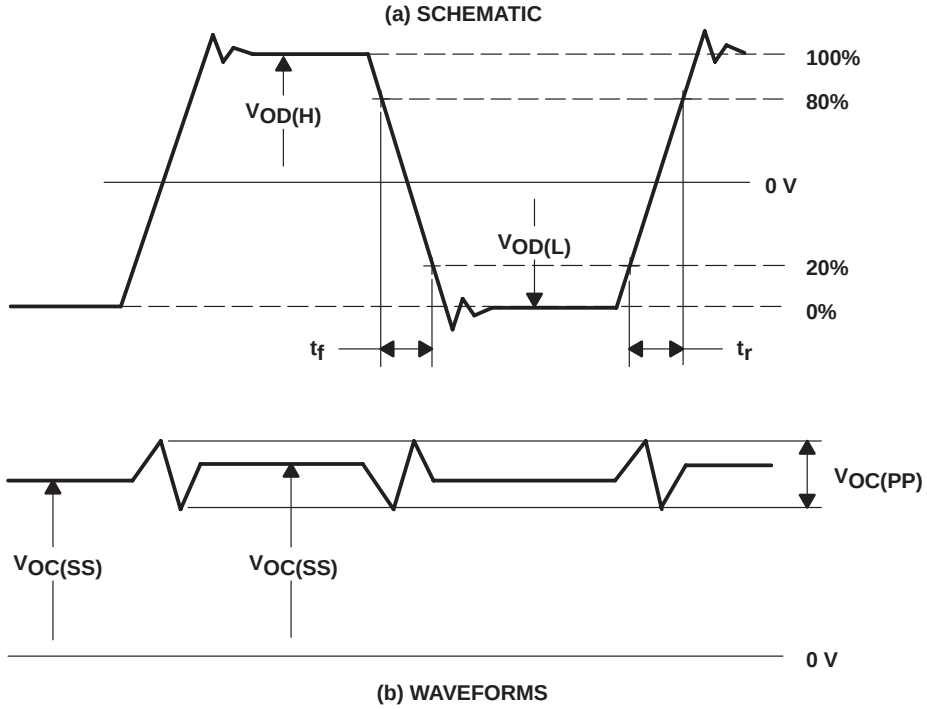
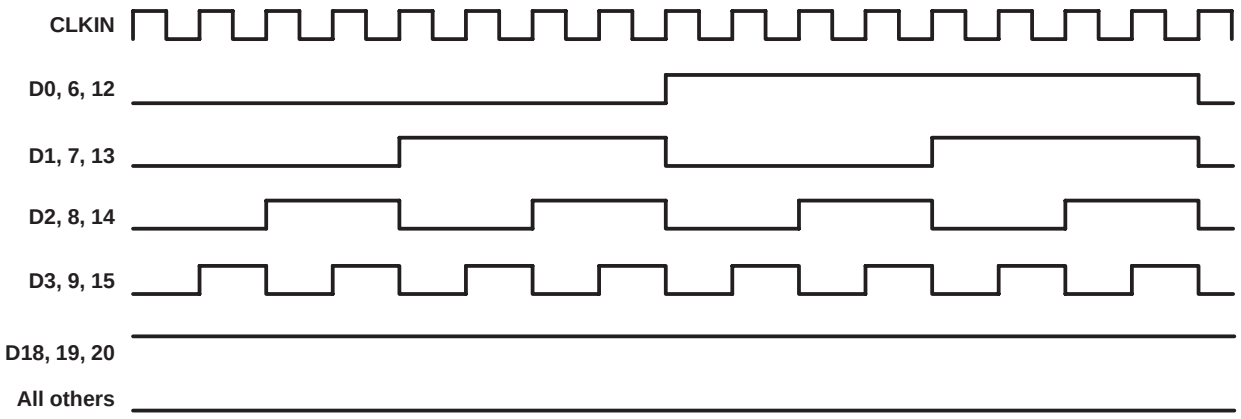


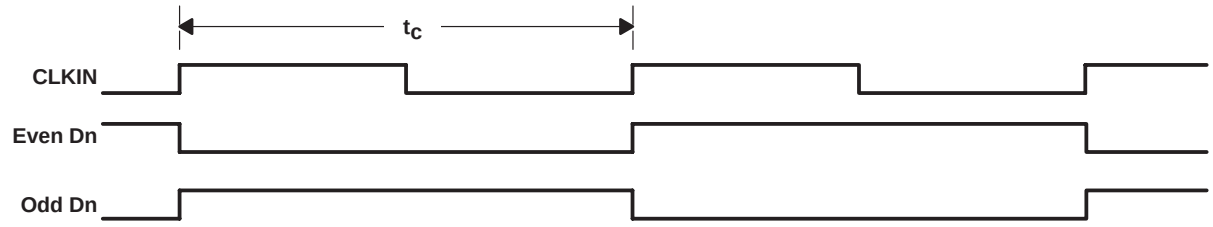
Figure 3. Test Load and Voltage Definitions for LVDS Outputs

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The 16-grayscale test-pattern test device power consumption for a typical display pattern.
B. V_{IH} = 2 V and V_{IL} = 0.8 V
C. SN75LVDS84 shown (CLKIN is inverted for SN75LVDS85).

Figure 4. 16-Grayscale Test-Pattern Waveforms



NOTES: A. The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.
B. V_{IH} = 2 V and V_{IL} = 0.8 V
C. SN75LVDS84 shown (CLKIN is inverted for SN75LVDS85).

Figure 5. Worst-Case Test-Pattern Waveforms

PARAMETER MEASUREMENT INFORMATION

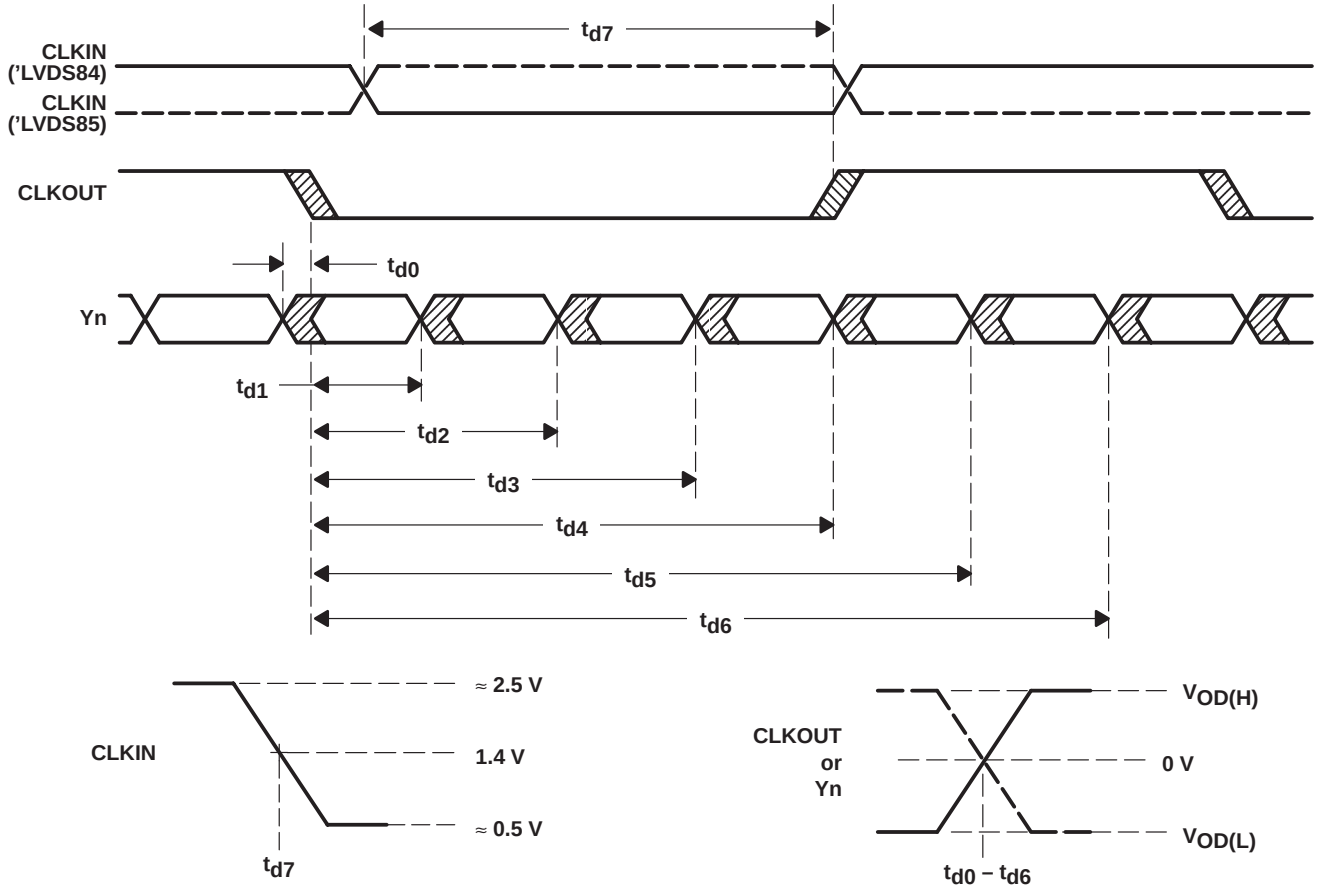


Figure 6. Timing Definitions

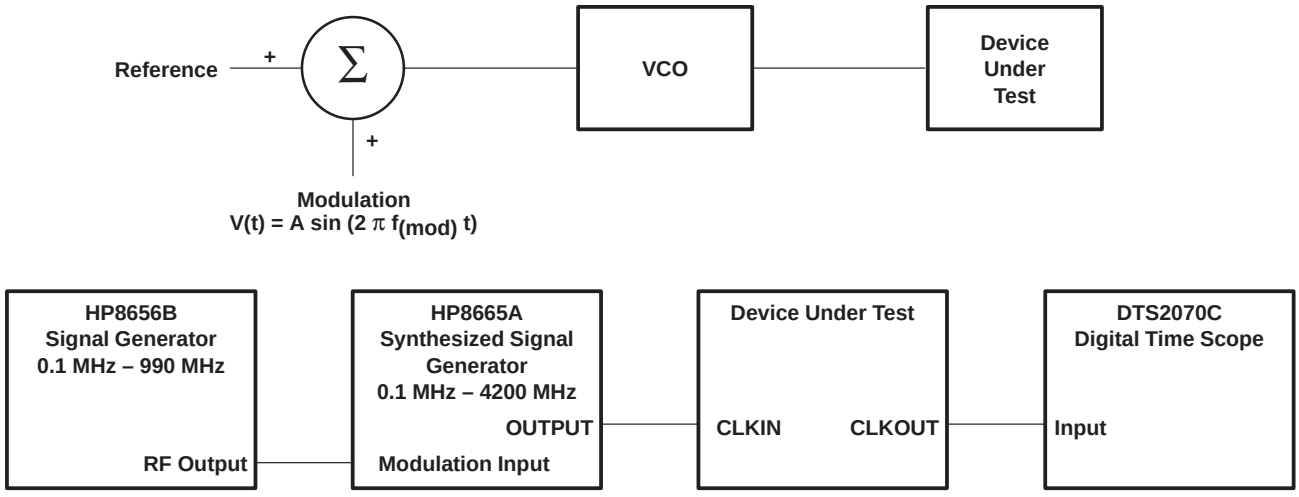
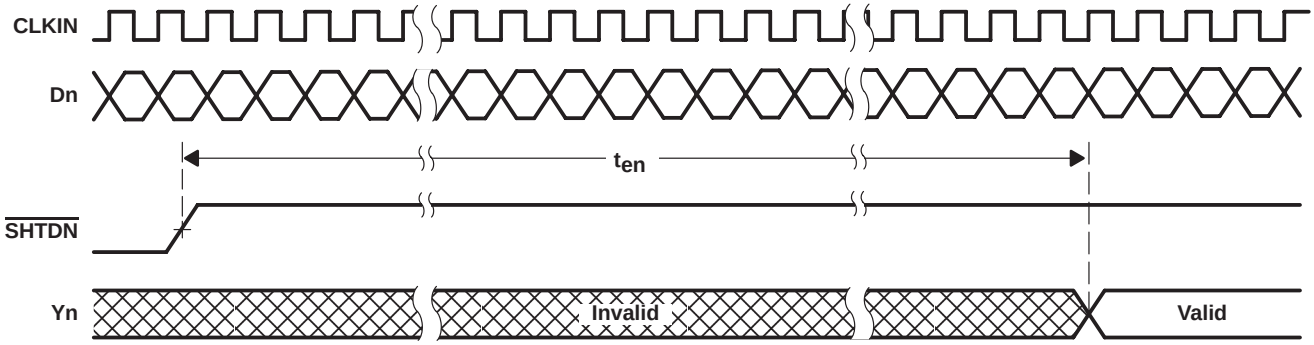


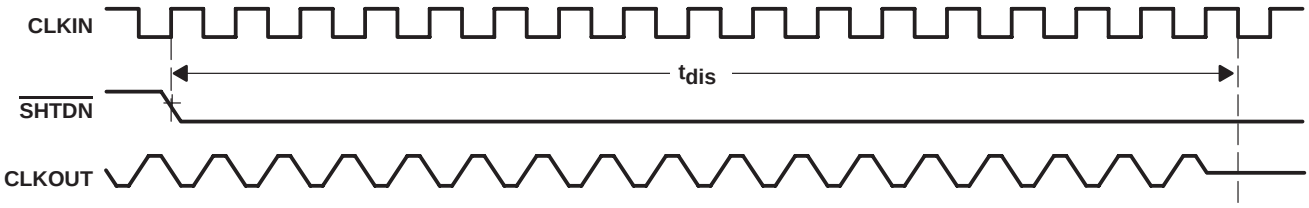
Figure 7. Clock Jitter Test Setup

TYPICAL CHARACTERISTICS



NOTE A: SN75LVDS84 shown.

Figure 8. Enable Time Waveforms



NOTE A: SN75LVDS84 shown.

Figure 9. Disable Time Waveforms

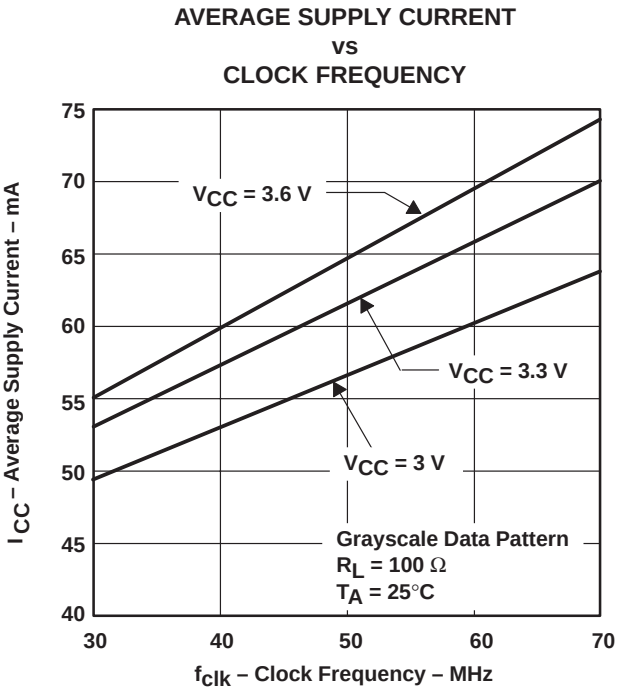


Figure 10

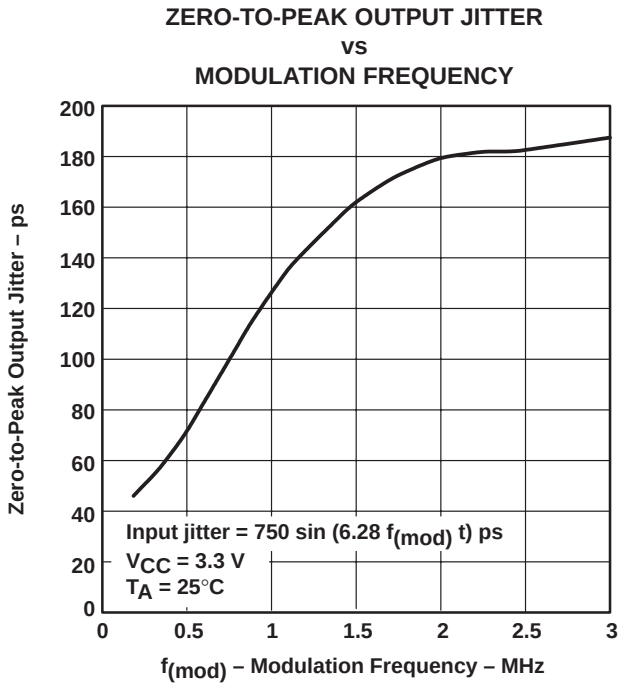
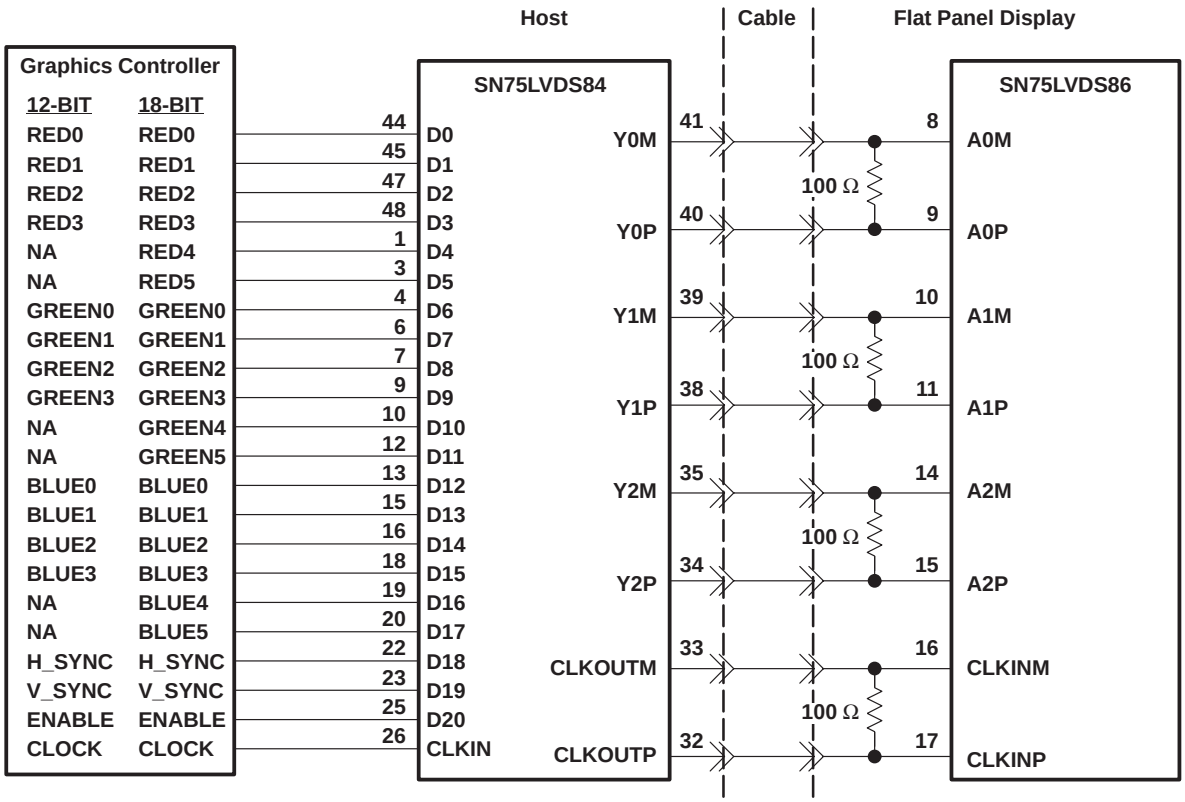


Figure 11

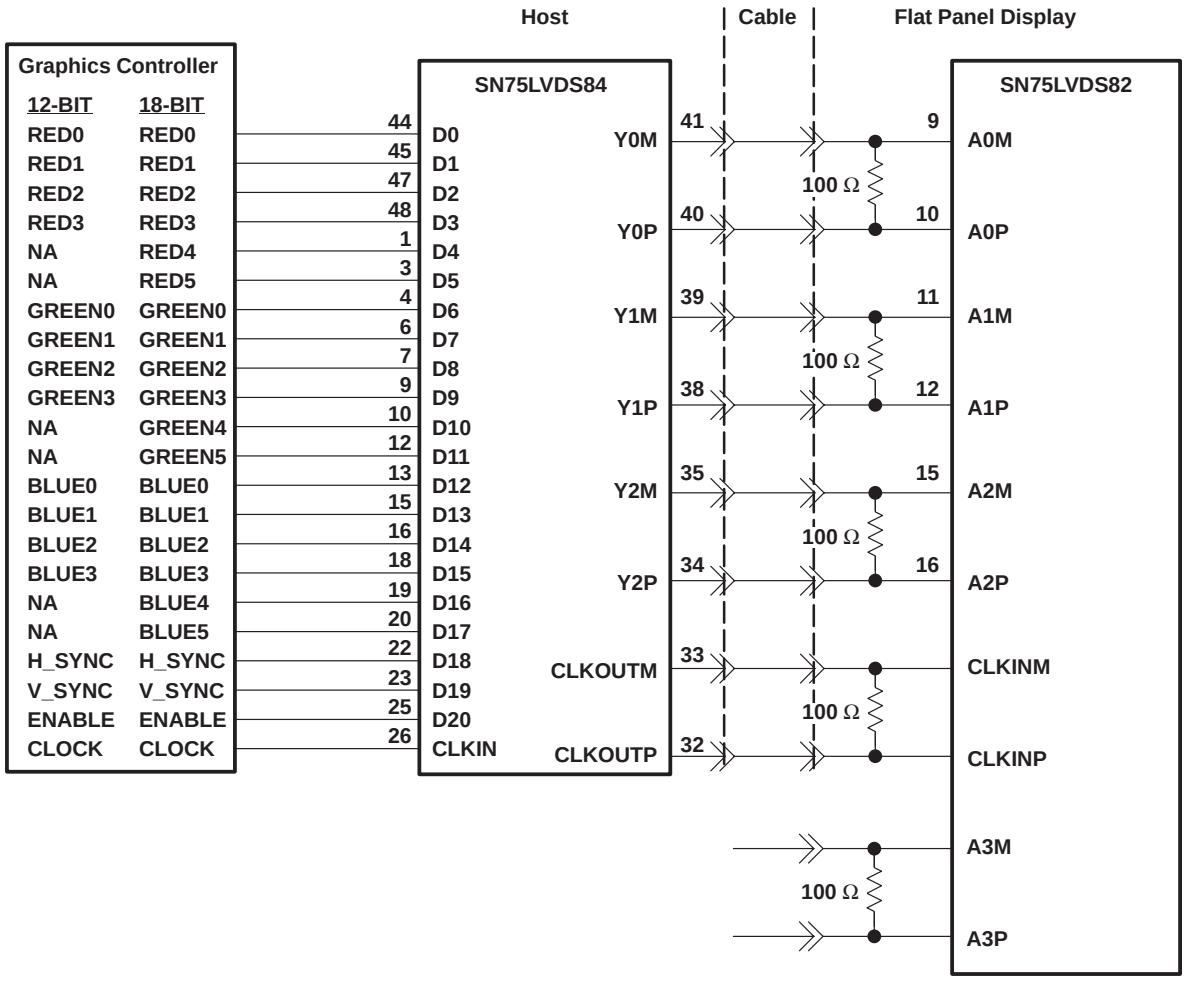
APPLICATION INFORMATION



NOTES: A. The five 100-Ω terminating resistors are recommended to be 0603 types.
B. NA – not applicable, these unused inputs should be left open.

Figure 12. Color Host to LCD Panel Application

APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA – not applicable, these unused inputs should be left open.

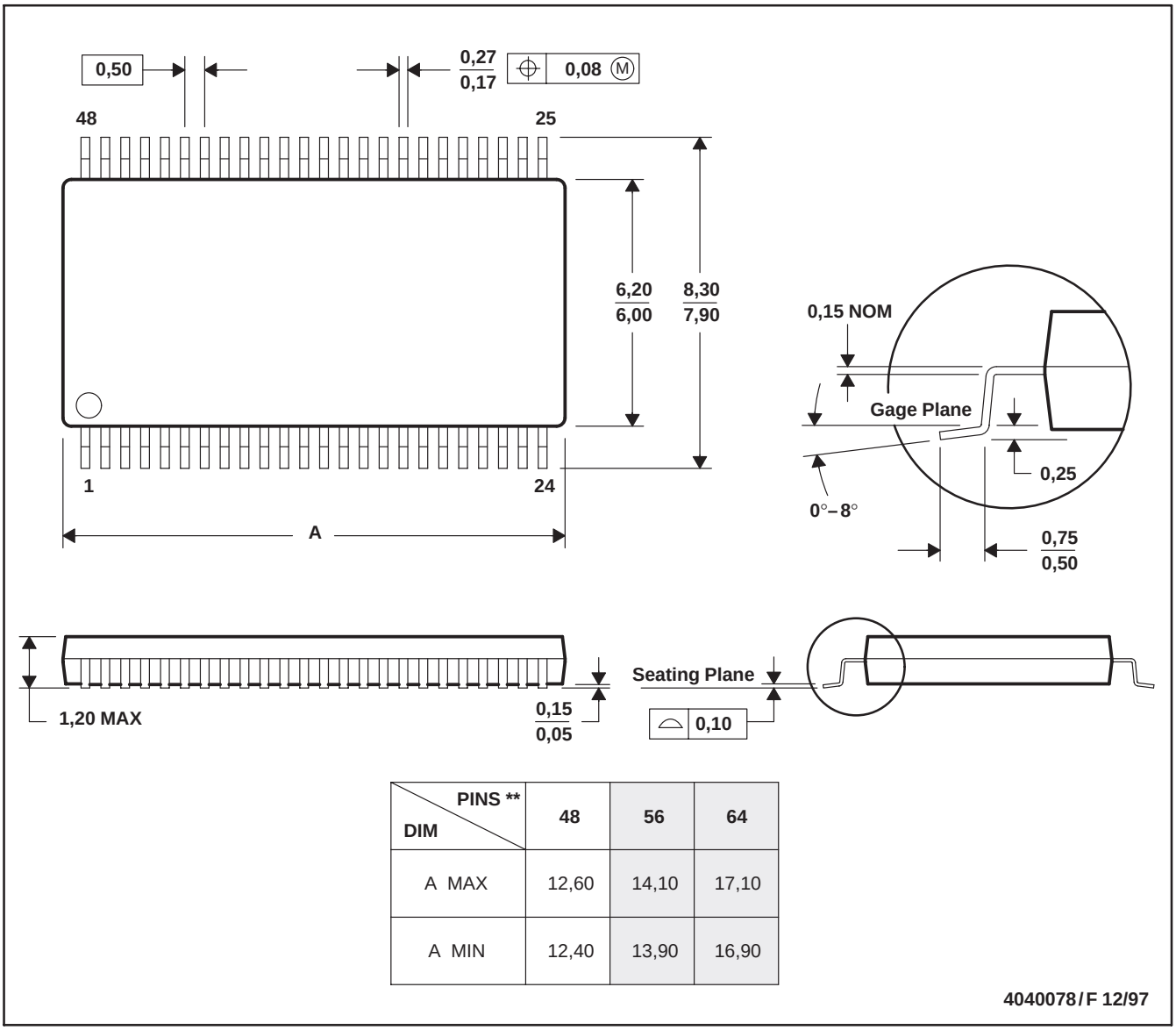
Figure 13. 18-Bit Color Host to 24-Bit LCD Display Panel Application†

† See the FlatLink Designer's Guide (SLLA012) for more application information.

MECHANICAL INFORMATION

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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