- **Flatlink Interface Utilizes Low Power Differential Signalling(LVDS)**
- **Suitable for Notebook Application**
- **XGA Resolution**
- **Six Bit System Interface**
- **Support Mainstream Data and Gate Drivers**
- **Optional Configurable Pins**
- **Low Voltage CMOS 3.3 V Technology**
- **65 MHz Phase-Lock Input**
- **100-pin TQFP Package for Compact LCD Module**
- **Tolerates 4 kV HBM ESD for LVDS Pins and 2 kV HBM for Others**
- **Improved Jitter Tolerance**

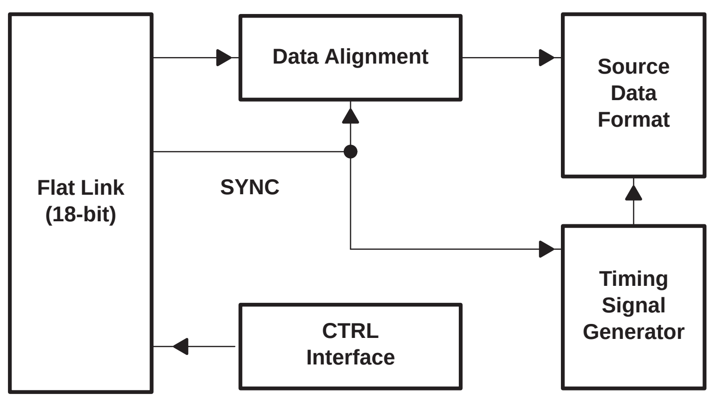
description

The SN75LVDS88A (LVDS panel timing controller) integrates a Flatlink signal interface with a TFT LCD timing controller. It resides in the LCD panel and provides interface between the graphic controller and a TFT LCD panel.

The SN75LVDS88A accepts host data through 3 pairs of inputs (18-bits) making up the LVDS bus, which is a low-EMI high-throughput interface. SN75LVDS88A then reformats the received image data into a specific data format and synchronous timing suitable for driving LCD panel column and row drivers. This device supports XGA resolution.

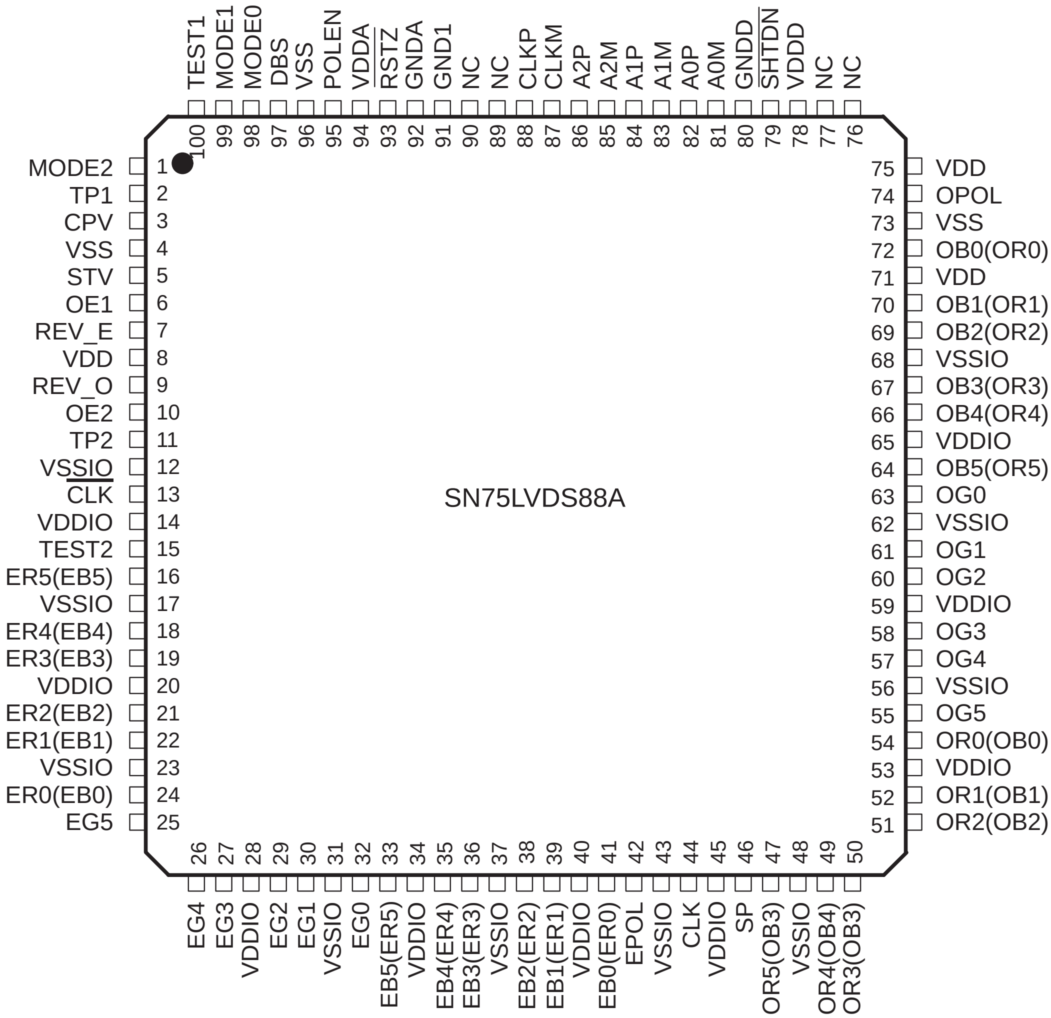
The SN75LVDS88A is easily configured by several selection terminals and is equipped with default timing specifications to support mainstream gate and source drivers on the market.

block diagram



pin assignment

TQFP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A0M/A0P	81,82	I	Flatlink 1st data pair
A1M/A1P	83, 84	I	Flatlink 2nd data pair
A2M/A2P	85, 86	I	Flatlink 3rd data pair
CLK	44	O	CD bus clock
$\overline{\text{CLK}}$	13	O	CD bus clock (180 degree out of phase)
CLKM/CLKP	87, 88	I	Flatlink clock pair
CPV	3	O	Gate driver clock
DBS	97	I	Data bus sequence
EPOL	42	O	Even RGB data stream polarity indicator
ER0..ER5 (EB0)..(EB5)	24,22,21 19,18,16	O	Even red (blue) data bus, controlled by DBS Pin, 0 = red, 1 = blue
(ER0)..(ER5) EB0..EB5	41,39,38 36,35,33	O	Even blue (red) data bus, controlled by DBS Pin, 0 = blue, 1 = red
GND1	91	P	PLL ground for LVDS
MODE0	98	I	Default timing selection pin 0
MODE1	99	I	Default timing selection pin 1
MODE2	1	I	Default timing selection pin 2
NC	76, 77, 89, 90	NC	NC terminals†
OE1, OE2	6, 10	O	Gate driver output enable
OG0..OG5	63,61,60 58,57,55	O	Odd green data bus
OPOL	74	O	Odd RGB data stream polarity indicator
OR0..OR5 (OB0)..(OB5)	54,52,51 50,49,47	O	Odd red (blue) data bus, controlled by DBS Pin, 0 = red, 1 = blue
(OR0)..(OR5) OB0..OB5	72,70,69 67,66,64	O	Odd blue (red) data bus, controlled by DBS Pin, 0 = blue, 1 = red
POLEN	95	I	Output data polarity control enable /disable
REV_E	7	O	CD line/dot inversion control signal
REV_O	9	O	CD line/dot inversion control signal (180 degree of phase)
$\overline{\text{RSTZ}}$	93	I	Reset, active low
$\overline{\text{SHTDN}}$	79	I	System shutdown control, active low
SP	46	O	Data bus starting pulse
STV	5	O	Gate driver starting pulse
TEST1, TEST2	100, 15	I	Test points†
TP1, TP2	2, 11	O	CD output control signal
VDDA	94	P	PLL power for LVDS
GNDA	92	P	Analog ground for LVDS
VDDD	78	P	Digital power supply for LVDS
GNDD	80	P	Digital power ground for LVDS
VDD	8,71,75	P	Digital power
VSS	4,73,96	P	Digital ground
VDDIO		P	I/O power
VSSIO		P	I/O ground

† Terminals must be connected to ground.

options

output control

PIN NAME	PIN NO.	INTERNAL CONNECTION		DESCRIPTION
		REQUIRED	SUGGESTED	
MODE0 MODE1 MODE2	98 99 1	Pull-up Pull-up Pull-down		Default timing selection pin 0 Default timing selection pin 1 Default timing selection pin 2
POLEN		Pull-down		0 = Output data reverse disable 1 = Output data reverse enable
DBS	97	Pull-down		Data bus sequence 0 = normal (RGB) 1 = reverse (BGR)

NOTE: DBS and POLEN functions must not be enabled together.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}‡ . . . . –0.5 V to 4 V
Voltage range at any terminal . . . . –0.5 V to V_{CC} + 0.5 V
Continuous power dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Electrostatic discharge: Class 3 A . . . . 4 kV
Class 2 B . . . . 200 V
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to the GND terminals unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR§ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PFD	1.548 W	12 mW	1.012 W

§ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	$\overline{SHTDN}$	2			V
Low-level input voltage, V_{IL}	$\overline{SHTDN}$			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$		0.1		0.6	V
Common–mode input voltage, V_{IC}		$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold				100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			mV
I_{CC}	Quiescent current (average)	Disabled, all inputs to ground			360	µA
		Enabled, AnP at 1 V and AnM at 1.4 V, t_C = 15.38 ns		80		mA
		Enabled, C_L = 8 pF, Grayscale pattern , t_C = 15.38 ns		100		mA
		Enabled, C_L = 8 pF, Worst-case pattern , t_C = 15.38 ns		120		mA
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$			±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0 V			±20	µA
I_{IN}	Input current (A inputs)	0 V ≤ V_I ≤ 2.4 V			±20	µA
I_{OZ}	High-impendance output current	V_O = 0 V or V_{CC}			±10	µA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

timing requirements

		MIN	TYP	MAX	UNIT
t_c§	Input clock period	14.7		31.25	ns
t_{su}/t_h	Input set up or hold time	550			ps

§ t_c is defined as the mean duration of a minimum of 32,000 clock periods.

output buffer rating

	MIN	TYP	MAX	UNIT
STV, SP		4		mA
CLK, $\overline{CLK}$		12		mA
Data bus and remaining outputs		8		mA

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dr1}	Input clock rising to output clock rising delay	C_L = 100 pF	10		40	ns
t_{df1}	Input clock rising to output clock falling delay		10		40	ns
t_{su1}	Data set up time, E/O RGB to CLK↑	C_L = 100 pF	10		20	ns
t_{h1}	Data hold time, CLK↑ to E/O RGB		10		20	ns
$t_{(RSKM)}$	Receiver input skew margin, See Note 4	t_c = 15.38 ns (±0.2%), |Input clock jitter |< 50 ps, See Note 5	550	700		ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$ to phase lock			1		ms
t_{dis}	Disable time, $\overline{\text{SHTDN}}$ to off state			250		ns
t_{su2}	SP setup time	C_{sp} = 15 pF	10		20	ns
t_{h2}	SP pulse hold time		10		20	ns

NOTES: 1. t_{RSKM} is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from $t_{RSKM} = \frac{t_c}{14} - 300$ ps.

2. |Input clock jitter| is the magnitude of the change in the input clock period.

PARAMETER MEASUREMENT INFORMATION

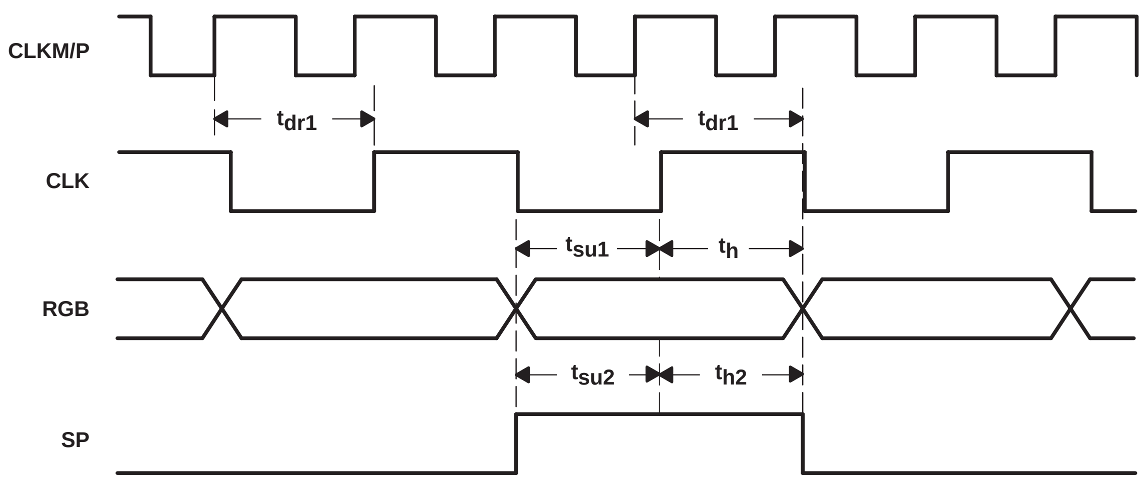


Figure 1. Output Setup and Hold Time

REFERENCE TIMING DIAGRAM

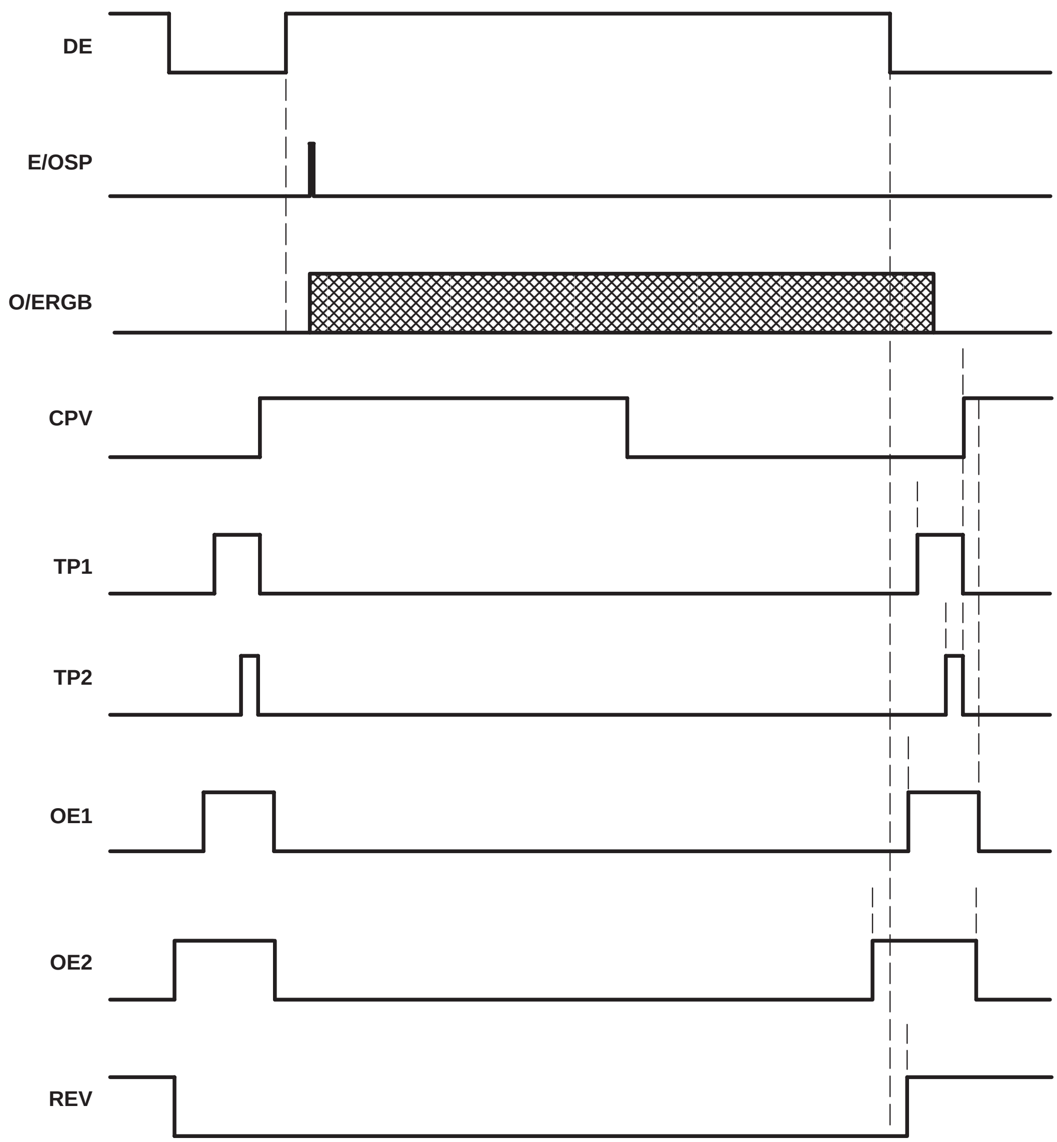


Figure 2. Typical Output Waveform

PARAMETER MEASUREMENT INFORMATION

functional description

Flatlink

The core of the Flatlink is TIs original 86A LVDS receiver which has three data channels for the 18-bit color plus one clock channel.

data alignment

The data alignment block supports dual bus dual port column driver configuration. When interfacing a 2-port column driver, the controller arranges pixels in odd and even order, then distributes them to odd and even buses and each connects to either of the driver ports. Under this setup, the controller outputs one clock, one or two data polarities (depends on driver), and one inverse (support line inversion) signal to the drivers.

output formatting

The output formatting provides several functions to reduce EMI, noise, and timing delay arrangement. These functions are controllable through some optional pins. See the registers and options section for reference.

- Reverse Polarity Generation
  When enable this function generates polarity indication signals. This occurs when the number of transitions in the output data bus exceeds 18-bits compared to the previous output under normal polarity. The polarity signal will be active and the output will be the opposite polarity to reduce transition
- Line Inversion
  When enabled, the REV_O and REV_E terminals will output the same line inversion control signals but in opposite polaritys.

timing control

- Source Shifted Clock(SSC)
  The master data clock could be arranged to have an intentional phase delay relative to the output data, which helps the system engineer tune the clock to latch the data correctly regardless of the characteristics presented by the PCB and the layout.
- Horizontal Starting pulses
  ESP and OSP terminals are used as the horizontal starting pulses outputs pins. Their output are one HCLK period ahead of the RGB data stream
- Horizontal Clock
  ECLK and OCLK terminals are responsible for the clock pulses, based on the XGA resolution when its frequency is at 32.5 MHz.
- CD Data Latch Pulse
  TP1 and TP2 provide the column driver input latch and output enable signals.
- Gate Driver Clock
  The CPV terminal output the clock pulses to the gate drivers as the horizontal sync timing in its CRT counter part.
- Gate Driver Starting Pulse
  The vertical starting pulse automatically generates at the start of every frame.
- Gate Driver Output Enable
  The OE1 and OE2 terminals provide the gate output enabale signals.

PARAMETER MEASUREMENT INFORMATION

functional description (continued)

vertical/horizontal reference generator

This block provides vertical and horizontal reference points for timing control. Vsync, Hsync, and ENAB signals along with the auto detection function determine when the video from the host is valid.

power-up procedure

Due to the uncertainty of registers and counters in the driver, SN75LVDS88A combines the input from both reset and Vsync to blank the output and simultaneously resets the content of drivers (see Figure 3).

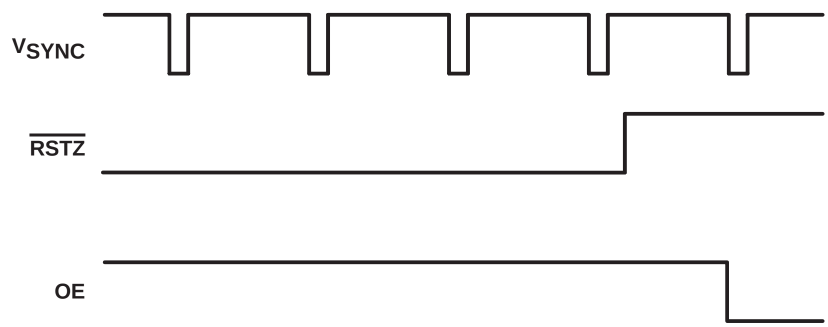
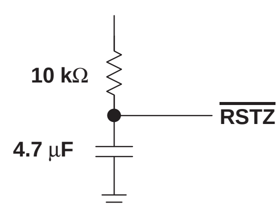


Figure 3. Reset Waveform

It is recommended that the following circuit be used to ensure the device is reset for more than 5 ms after power up.



APPLICATION INFORMATION

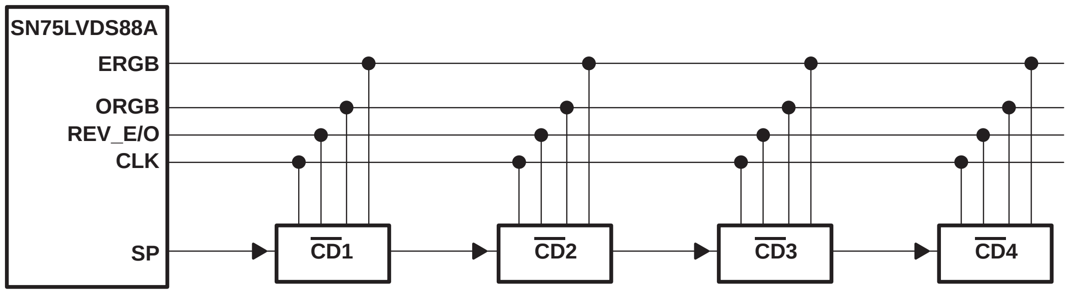


Figure 4. Application Block Diagram

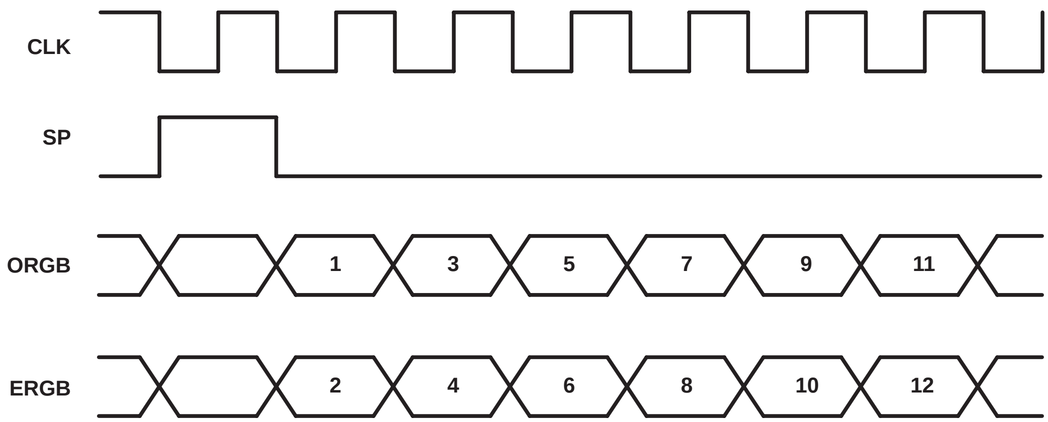
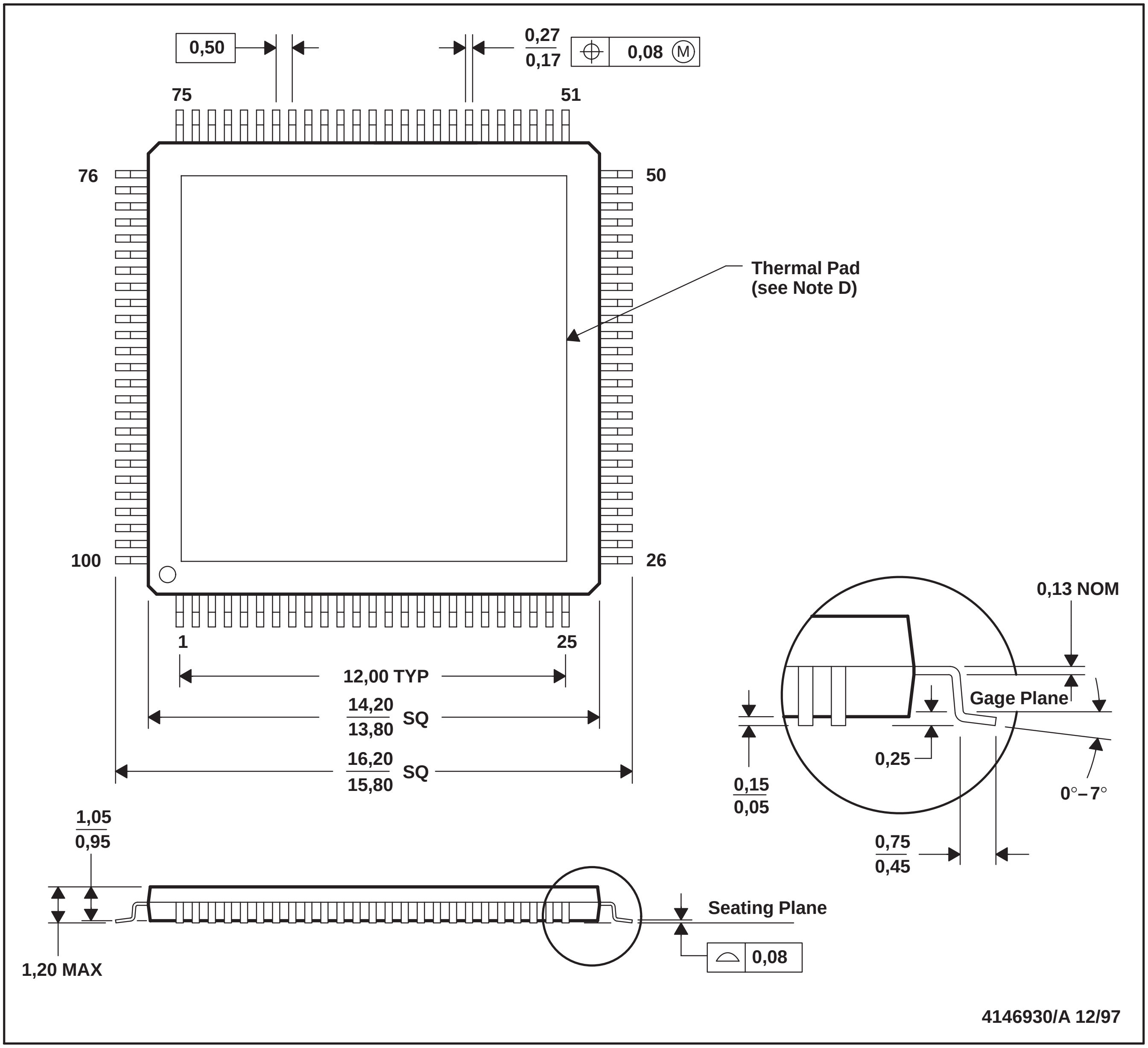


Figure 5. Data Output Format

MECHANICAL DATA

PFD (S-PQFP-G100) **PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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