3.3V FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS

FEATURES

- **1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Optional Driver Output Transition Times for Signaling Rates (1) of 1 Mbps, 5 Mbps and 25 Mbps**
- **Low-Current Standby Mode: < 1 μA**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **5V Tolerant Inputs**
- **Bus Idle, Open, and Short Circuit Failsafe**
- **Meets or exceeds the requirements of ANSI TIA/EIA-485-A and RS-422 Compatible**
- **5-V Devices available, SN65HVD50-59**

APPLICATIONS

- **Utility Meters**
- **DTE/DCE Interfaces**
- **Industrial, Process, and Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

DESCRIPTION

The SN65HVD3X devices are 3-state differential line drivers and differential-input line receivers that operate with 3.3-V power supply.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11 and ISO 8482:1993 standard-compliant devices.

The SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36 and SN65HVD37 are fully enabled with no external enabling pins. The SN65HVD36 and SN65HVD37 implement receiver equalization technology for improved performance in long distance applications.

The SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, and SN65HVD39 have active-high driver enables and active-low receiver enables. A very low, less than 1 μA, standby current can be achieved by disabling both the driver and receiver. The SN65HVD38 and SN65HVD39 implement receiver equalization technology for improved performance in long distance applications.

All devices are characterized for operation from -40°C to +85°C.

The SN65HVD36 and SN65HVD38 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates up to 20 Mbps at cable lengths up to 160 meters.

The SN65HVD37 and SN65HVD39 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates in the range of 1 to 5 Mbps at cable lengths up to 1000 meters.

IMPROVED REPLACEMENT FOR:

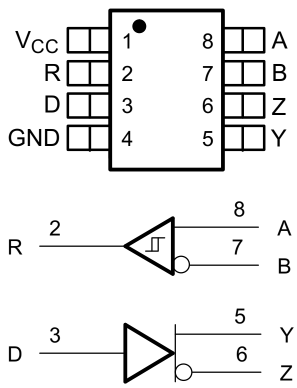
Part Number	Replace with	
xxx3491	SN65HVD33:	Better ESD protection (15kV vs 2kV or not specified) Higher Signaling Rate (25Mbps vs 20Mbps) Fractional Unit Load (64 Nodes vs 32)
MAX3491E	SN65HVD33:	Higher Signaling Rate (25Mbps vs 12Mbps) Fractional Unit Load (64 Nodes vs 32)
MAX3076E	SN65HVD33:	Higher Signaling Rate (25Mbps vs 16Mbps) Lower Standby Current (1 μA vs 10 μA)
MAX3073E	SN65HVD34:	Higher Signaling Rate (5Mbps vs 500kbps) Lower Standby Current (1 μA vs 10 μA)
MAX3070E	SN65HVD35:	Higher Signaling Rate (1Mbps vs 250kbps) Lower Standby Current (1 μA vs 10 μA)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

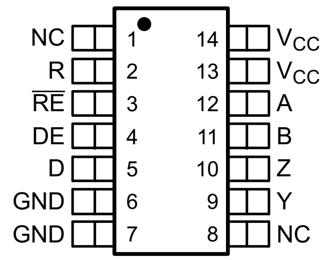
SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, SN65HVD37

D PACKAGE (TOP VIEW)

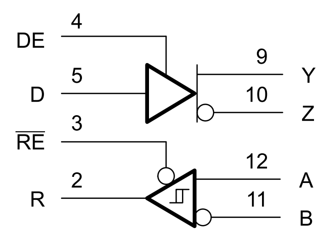


SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, SN65HVD39

D PACKAGE (TOP VIEW)



NC - No internal connection



AVAILABLE OPTIONS

SIGNALING RATE	UNIT LOADS	RECEIVER EQUALIZATION	ENABLES	BASE PART NUMBER	SOIC MARKING
25 Mbps	1/2	No	No	SN65HVD30	PREVIEW
5 Mbps	1/8	No	No	SN65HVD31	PREVIEW
1 Mbps	1/8	No	No	SN65HVD32	PREVIEW
25 Mbps	1/2	No	Yes	SN65HVD33	65HVD33
5 Mbps	1/8	No	Yes	SN65HVD34	65HVD34
1 Mbps	1/8	No	Yes	SN65HVD35	65HVD35
25 Mbps	1/2	Yes	No	SN65HVD36	PREVIEW
5 Mbps	1/8	Yes	No	SN65HVD37	PREVIEW
25 Mbps	1/2	Yes	Yes	SN65HVD38	PREVIEW
5 Mbps	1/8	Yes	Yes	SN65HVD39	PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[(1)(2)]

		UNIT
V_{CC}	Supply voltage range, V_{CC}	–0.3 V to 6 V
	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
	Voltage input, transient pulse through 100 Ω. See Figure 12 (A, B, Y, Z)[(3)]	–50 to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	-0.5 V to 7 V
	Continuous total power dissipation	Internally limited
I_O	Output current (receiver output only, R)	11 mA

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.0		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7[(1)]		12	V
$1/t_{UI}$	Signaling rate	SN65HVD30, SN65HVD33, SN65HVD36, SN65HVD38			25	Mbps
		SN65HVD31, SN65HVD34, SN65HVD37, SN65HVD39			5	Mbps
		SN65HVD32, SN65HVD35			1	Mbps
R_L	Differential load resistance		54	60		Ω
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			mA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	mA
T_A	Ambient still-air temperature		–40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
Human body model	Bus terminals and GND		±16		kV
Human body model[(2)]	All pins		±4		kV
Charged-device-model[(3)]	All pins		±1		kV

(1) All typical values at 25°C with 3.3-V supply.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
$V_{I(K)}$	Input clamp voltage		I_I = –18 mA		–1.5			
$\|V_{OD(SS)}\|$	Steady-state differential output voltage		I_O = 0		2.5		V_{CC}	
			R_L = 54 Ω, See Figure 1 (RS-485)		1.5	2.0		
			R_L = 100 Ω, See Figure 1[(2)] (RS-422)		2.0	2.3		
			V_{test} = –7 V to 12 V, See Figure 2		1.5			
$\Delta\|V_{OD(SS)}\|$	Change in magnitude of steady-state differential output voltage between states		R_L = 54 Ω, See Figure 1 and Figure 2		–0.2		0.2	
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot		R_L = 54 Ω, C_L = 50 pF, See Figure 5 and Figure 3				0.05 $\|V_{OD(SS)}\|$	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD30, HVD33, HVD36, HVD38	See Figure 4			0.5		
		HVD31, HVD34, HVD37, HVD39, HVD32, HVD35				0.25		
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 4		1.6		2.3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.05		0.05	
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current		V_{CC} = 0 V, V_Z or V_Y = 12 V, Other input at 0 V				90	µA
			V_{CC} = 0 V, V_Z or V_Y = –7 V, Other input at 0 V		–10			
		HVD33, HVD34, HVD35, HVD38, HVD39	V_{CC} = 5 V or 0 V, DE = 0 V V_Z or V_Y = 12 V	Other input at 0 V			90	
			V_{CC} = 5 V or 0 V, DE = 0 V V_Z or V_Y = –7 V		–10			
$I_{Z(S)}$ or $I_{Y(S)}$	Short Circuit output Current		V_Z or V_Y = –7 V	Other input at 0 V	–250		250	mA
			V_Z or V_Y = 12 V		–250		250	
I_I	Input current	D, DE			0		100	µA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) V_{CC} is 3.3 Vdc ± 5%

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD30, HVD33, HVD36, HVD38	R_L = 54 Ω, C_L = 50 pF, See Figure 5	4	10	18	ns
		HVD31, HVD34, HVD37, HVD39		25	38	65	
		HVD32, HVD35		120	175	305	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD30, HVD33, HVD36, HVD38		4	9	18	ns
		HVD31, HVD34, HVD37, HVD39		25	38	65	
		HVD32, HVD35		120	175	305	
t_r	Differential output signal rise time	HVD30, HVD33, HVD36, HVD38		2.5	5	12	ns
		HVD31, HVD34, HVD37, HVD39		20	37	60	
		HVD32, HVD35		120	185	300	
t_f	Differential output signal fall time	HVD30, HVD33, HVD36, HVD38		2.5	5	12	ns
		HVD31, HVD34, HVD37, HVD39		20	35	60	
		HVD32, HVD35		120	180	300	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$ - $t_{PLH}\|$)	HVD30, HVD33, HVD36, HVD38				2	ns
		HVD31, HVD34, HVD37, HVD39				4	
		HVD32, HVD35				7	
t_{PZH1}	Propagation delay time, high-impedance-to-high-level output	HVD33, HVD38	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See Figure 6			45	ns
		HVD34, HVD39				235	
		HVD35				490	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD33, HVD38				25	ns
		HVD34, HVD39				65	
		HVD35				165	
t_{PZL1}	Propagation delay time, high-impedance-to-low-level output	HVD33, HVD38	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See Figure 7			35	ns
		HVD34, HVD39				190	
		HVD35				490	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD33, HVD38				30	ns
		HVD34, HVD39				120	
		HVD35				290	
t_{PZH2}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z See Figure 6			4000	ns
t_{PZL2}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y See Figure 7			4000	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –8 mA				–0.02	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 8 mA		–0.20			V
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})					50		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA		–1.5			V
V_O	Output voltage		V_{ID} = 200 mV, I_O = –8 mA, See Figure 8		2.4			V
			V_{ID} = –200 mV, I_O = 8 mA, See Figure 8				0.4	V
$I_{O(Z)}$	High-impedance-state output current		V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_A or I_B	Bus input current	HVD31, HVD32, HVD34, HVD35, HVD37, HVD39	V_A or V_B = 12 V	Other input at 0V		0.05	0.10	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.06	0.10	
			V_A or V_B = -7 V		–0.10	–0.04		
			V_A or V_B = -7 V, V_{CC} = 0 V		–0.10	–0.03		
		HVD30, HVD33, HVD36, HVD38	V_A or V_B = 12 V	Other input at 0 V		0.20	0.35	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.24	0.40	
			V_A or V_B = -7 V		–0.35	–0.18		
			V_A or V_B = -7 V, V_{CC} = 0 V		–0.25	–0.13		
I_{IH}	Input current, $\overline{RE}$		V_{IH} = 0.8 V or 2 V		–60			µA
C_{ID}	Differential input capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			15		pF
I_{CC}	Supply current	HVD30, HVD31, HVD32	D at 0 V or V_{CC} and No Load				6.4	mA
		HVD36, HVD37					7.9	mA
		HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at 0 V, No load (Receiver enabled and driver disabled)				1.8	mA
		HVD34, HVD35					2.2	
		HVD38, HVD39					3.8	
		HVD33, HVD34, HVD35, HVD38, HVD39	$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load (Receiver disabled and driver disabled)			0.022	1	µA
		HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at V_{CC}, No load (Receiver enabled and driver enabled)				2.1	mA
		HVD34, HVD35					6.5	
		HVD38					3.5	
		HVD39					8.0	
		HVD33	$\overline{RE}$ at V_{CC}, D at 0 V or V_{CC}, DE at V_{CC} No load (Receiver disabled and driver enabled)				1.8	
		HVD34, HVD35					6.2	
		HVD38					2.5	
		HVD39					7.0	

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD30, HVD33, HVD36, HVD38	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See Figure 9			26	45	ns
		HVD31, HVD32, HVD34, HVD35, HVD37, HVD39				47	70	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD30, HVD33, HVD36, HVD38				29	45	
		HVD31, HVD32, HVD34, HVD35, HVD37, HVD39				49	70	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	HVD30, HVD33, HVD36, HVD37, HVD38, HVD39					7	
		HVD31, HVD34, HVD32, HVD35					10	
t_r	Output signal rise time						5	
t_f	Output signal fall time						6	
t_{PHZ}	Output disable time from high level		DE at 3 V	C_L = 15 pF See Figure 10			20	
t_{PZH1}	Output enable time to high level						20	
t_{PZH2}	Propagation delay time, standby-to-high-level output		DE at 0 V				4000	
t_{PLZ}	Output disable time from low level		DE at 3 V	C_L = 15 pF See Figure 11			20	
t_{PZL1}	Output enable time to low level						20	
t_{PZL2}	Propagation delay time, standby-to-low-level output		DE at 0 V				4000	

(1) All typical values are at 25°C and with a 3.3-V supply

RECEIVER EQUALIZATION CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS			DEVICE	MIN	TYP(1)	MAX	UNIT
$t_{j(pp)}$	Peak-to-peak eye-pattern jitter	Pseudo-random NRZ code with a bit pattern length o 2^{16}-1, Belden 3105A cable	25 Mbps	0 m	HVD36, HVD38		PREVIEW		ns
				100 m	HVD33(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
				150 m	HVD33(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
				200 m	HVD33(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
			10 Mbps	200 m	HVD33(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
				250 m	HVD33(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
				300 m	HVD33(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
			5 Mbps	500 m	HVD34(2)		PREVIEW		
					HVD37, HVD39		PREVIEW		
			3 Mbps	500 m	HVD33(2)		PREVIEW		
					HVD34(2)		PREVIEW		
					HVD36, HVD38		PREVIEW		
					HVD37, HVD39		PREVIEW		
			1 Mbps	1000 m	HVD34(2)		PREVIEW		
					HVD37, HVD39		PREVIEW		

(1) All typical values are at V_{CC} = 5 V, and temperature = 25°C.
(2) The HVD33 and the HVD34 do not have receiver equalization but are specified for comparison.

DEVICE POWER DISSIPATION - P_D

TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
R_L = 60 , C_L = 50 pF, Input to D a 50% duty cycle square wave at indicated signaling rate T_A = 85°C	HVD30, HVD36 (25 Mbps)			197	mW
	HVD31, HVD37 (5 Mbps)			213	
	HVD32 (1 Mbps)			193	
R_L = 60 , C_L = 50 pF, DE at VCC, $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate T_A = 85°C	HVD33, HVD38 (25 Mbps)			197	
	HVD34, HVD39 (5 Mbps)			193	
	HVD35 (1 Mbps)			248	

PARAMETER MEASUREMENT INFORMATION

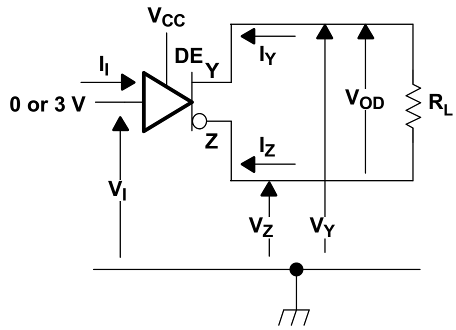


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

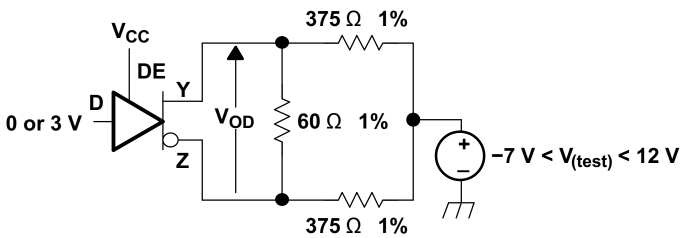


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

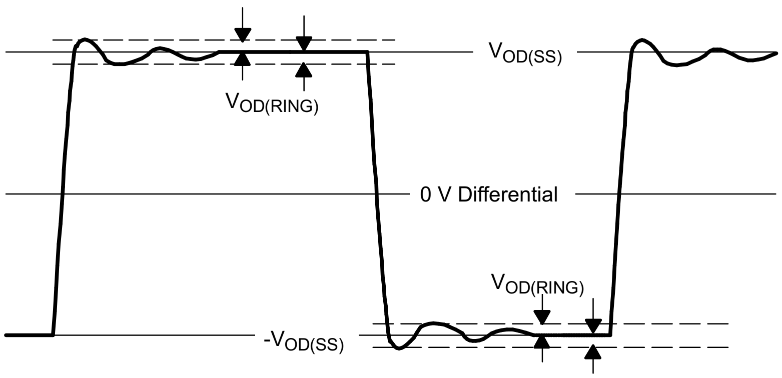


Figure 3. $V_{OD(RING)}$ Waveform and Definitions

VOD(RING) is measured at four points on the output waveform, corresponding to overshoot and undershoot from theVOD(H) and VOD(L) steady state values.

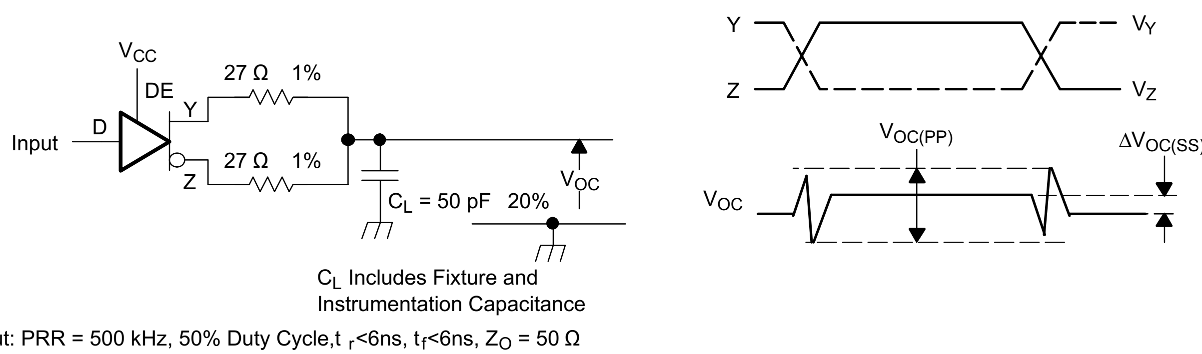
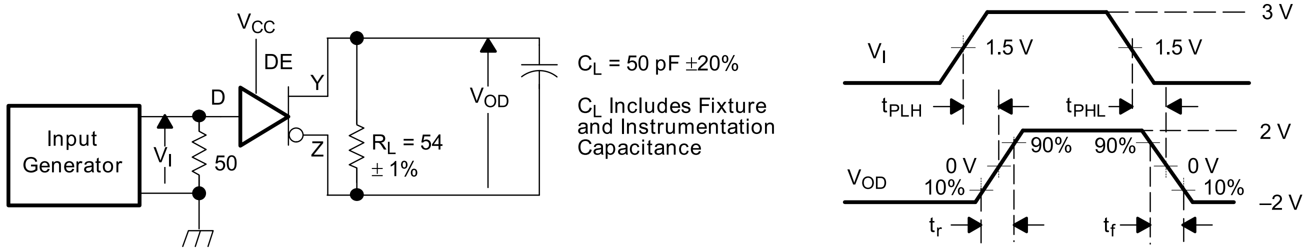


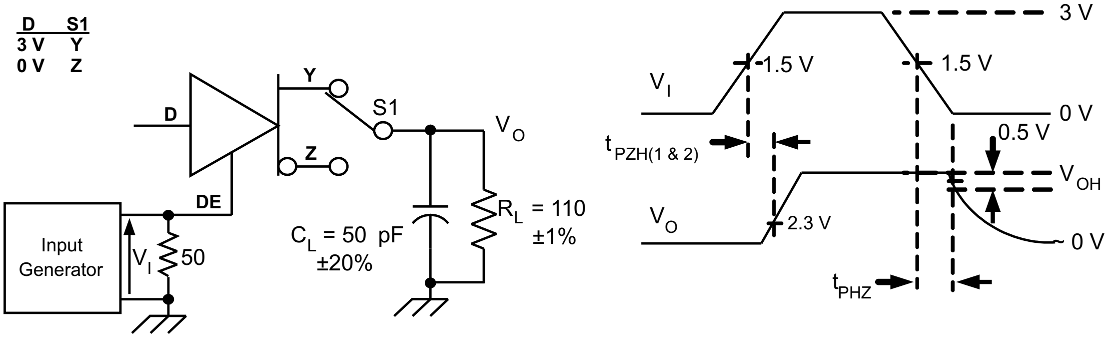
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



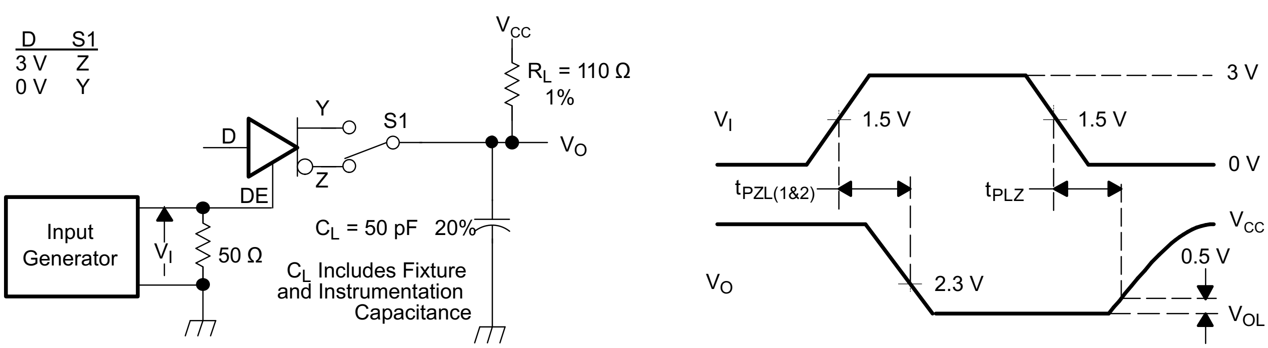
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50

Figure 5. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500kHz, 50% Duty Cycle, t_r<6 ns, t_f < 6ns, Z_0 = 50
C_L Includes Fixture and Instrumentation Capacitance

Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

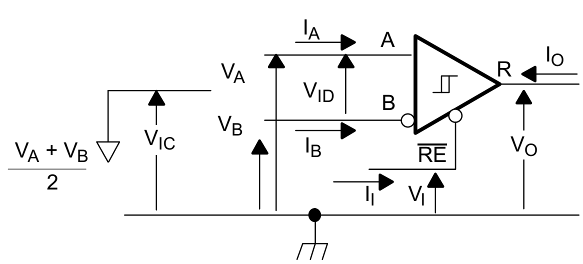


Figure 8. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

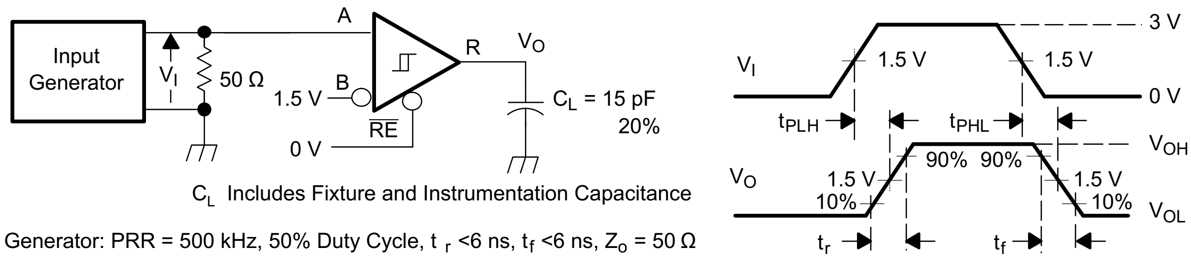


Figure 9. Receiver Switching Test Circuit and Voltage Waveforms

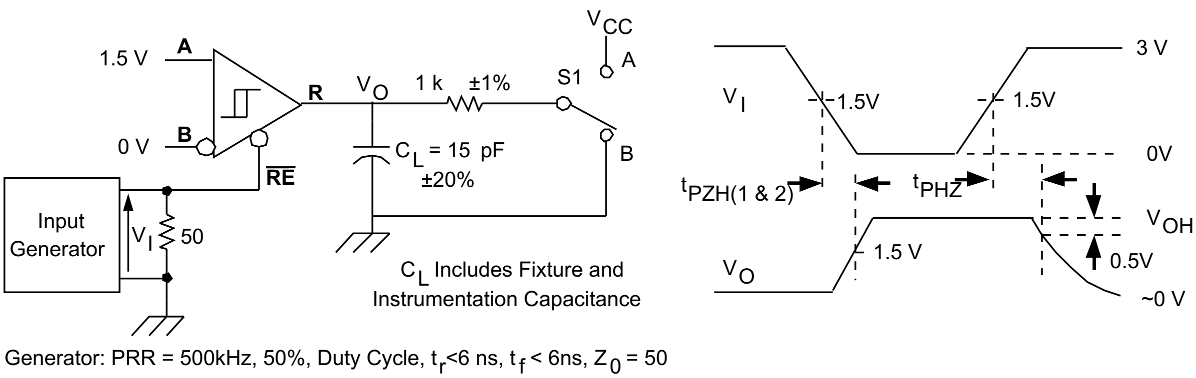


Figure 10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

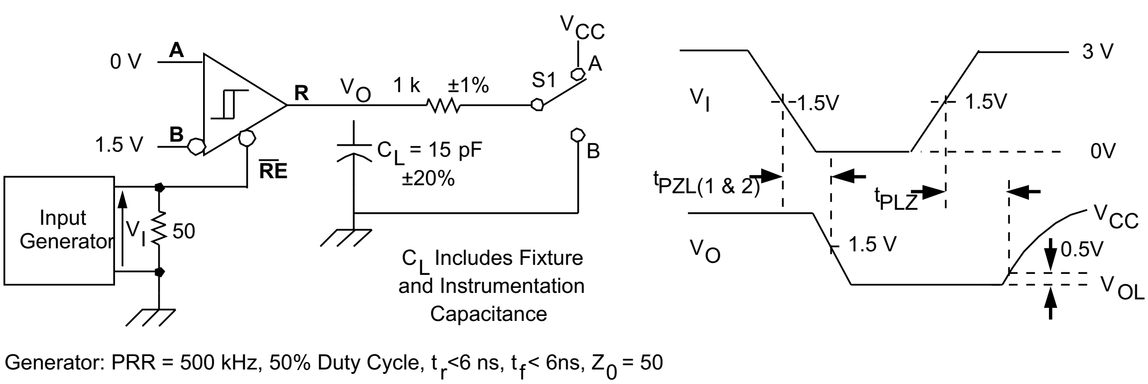


Figure 11. Receiver Enable Time From Standby (Driver Disabled)

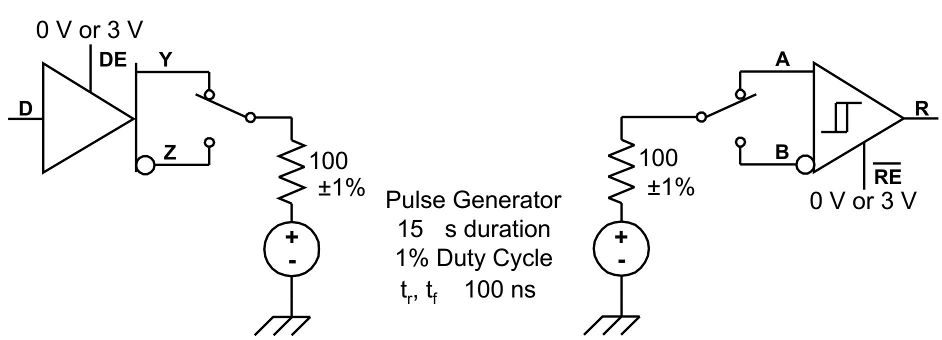


Figure 12. Test Circuit, Transient Over Voltage Test

DEVICE INFORMATION

LOW-POWER SHUTDOWN MODE

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

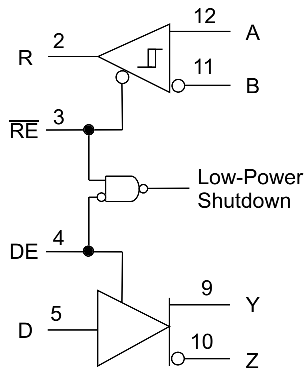


Figure 13. Low-Power Shutdown Logic Diagram

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

DEVICE INFORMATION (continued)

FUNCTION TABLES

SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, SN65HVD39 DRIVER

INPUTS		OUTPUTS	
D	**DE**	**Y**	**Z**
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, SN65HVD39 RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq –0.2$ V	L	L
$–0.2 V < V_{ID} < –0.02$ V	L	?
$–0.02 V \leq V_{ID}$	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_A=V_B$	L	H

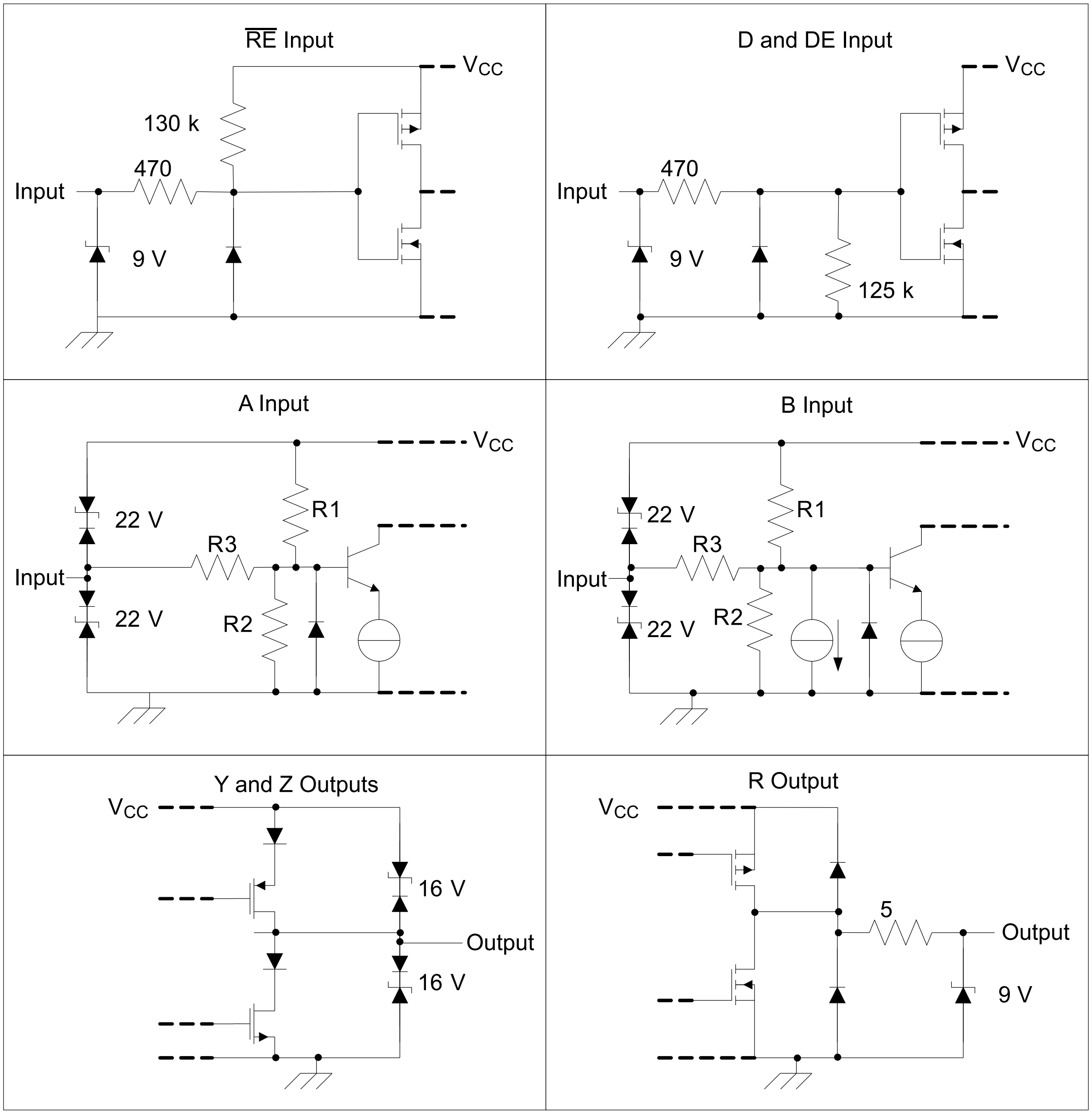
SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, SN65HVD37 DRIVER

	OUTPUTS	
INPUT D	**Y**	**Z**
H	H	L
L	L	H
Open	L	H

SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, SN65HVD37 RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	OUTPUT R
$V_{ID} \leq –0.2$ V	L
$–0.2 V < V_{ID} < –0.02$ V	?
$–0.02 V \leq V_{ID}$	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_A=V_B$	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD30, SN65HVD33, SN65HVD36, SN65HVD38	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35 SN65HVD37, SN65HVD38, SN65HVD39	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

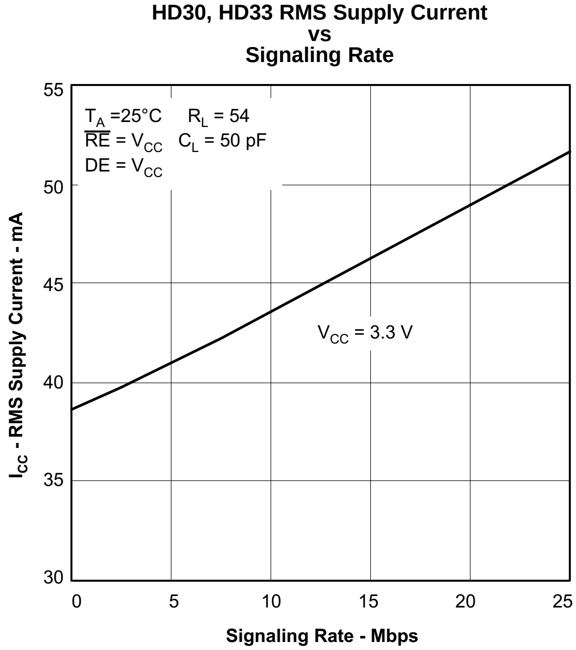


Figure 14.

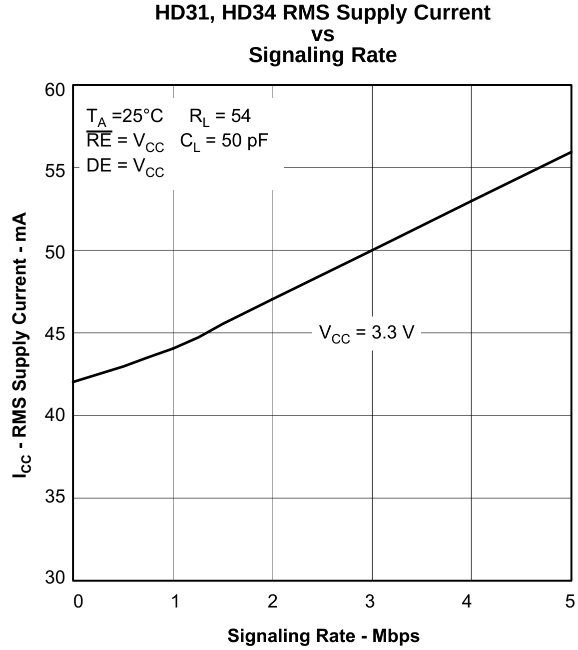


Figure 15.

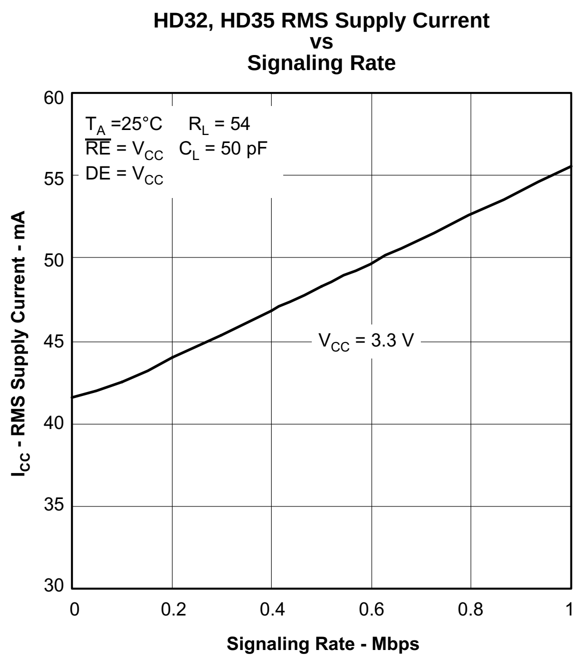


Figure 16.

TYPICAL CHARACTERISTICS (continued)

HVD30, HVD33
Bus Input Current
vs
Input Voltage

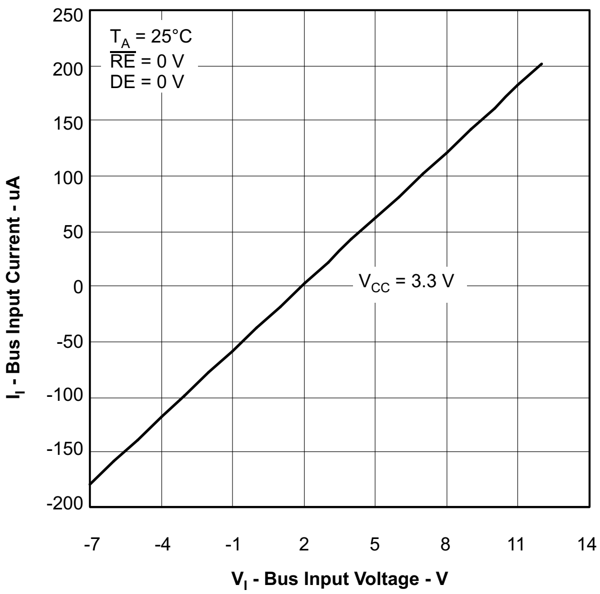


Figure 17.

HVD31, HVD32, HVD34, HVD35
Bus Input Current
vs
Input Voltage

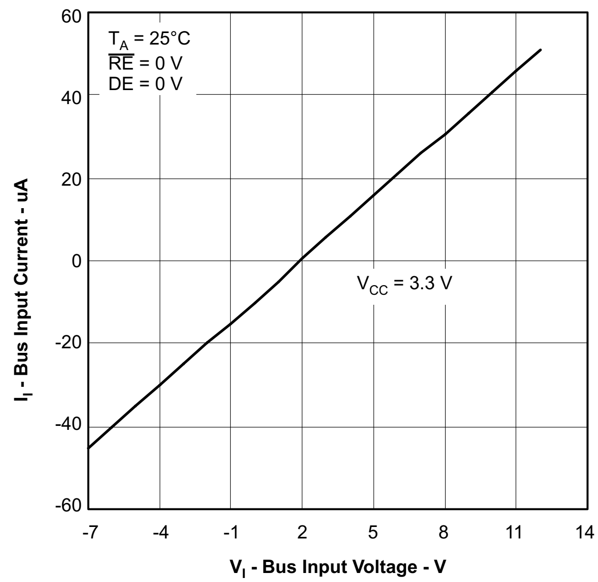


Figure 18.

Driver Low-Level Output Current
vs
Low-Level Output Voltage

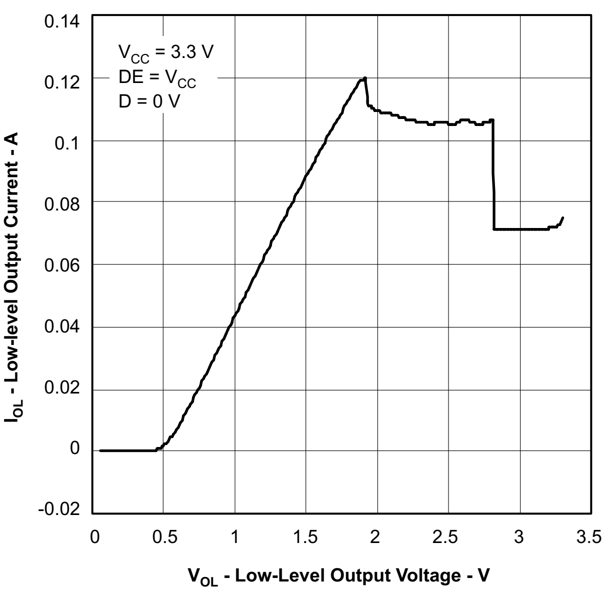


Figure 19.

Driver High-Level Output Current
vs
High-Level Output Voltage

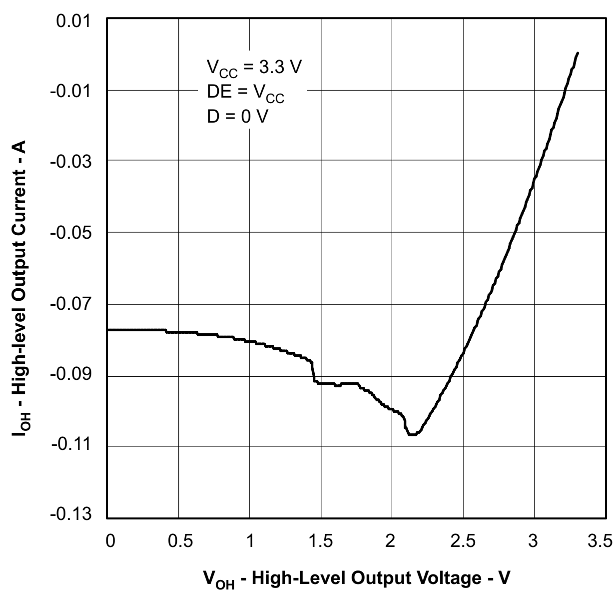


Figure 20.

TYPICAL CHARACTERISTICS (continued)

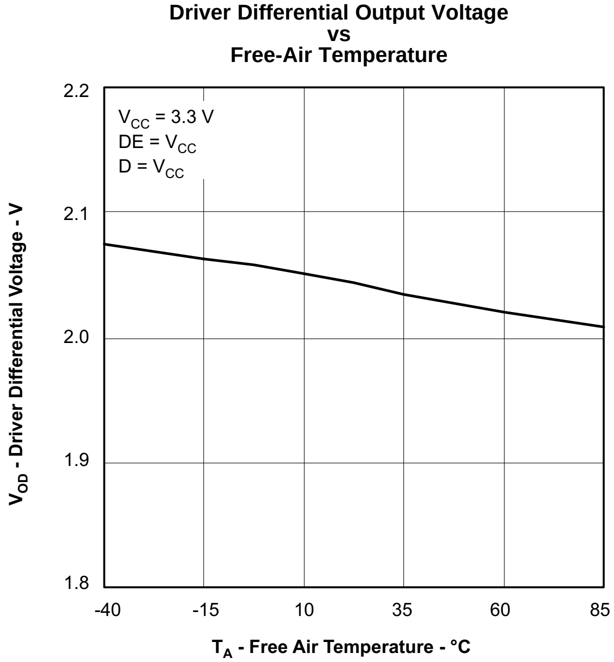


Figure 21.

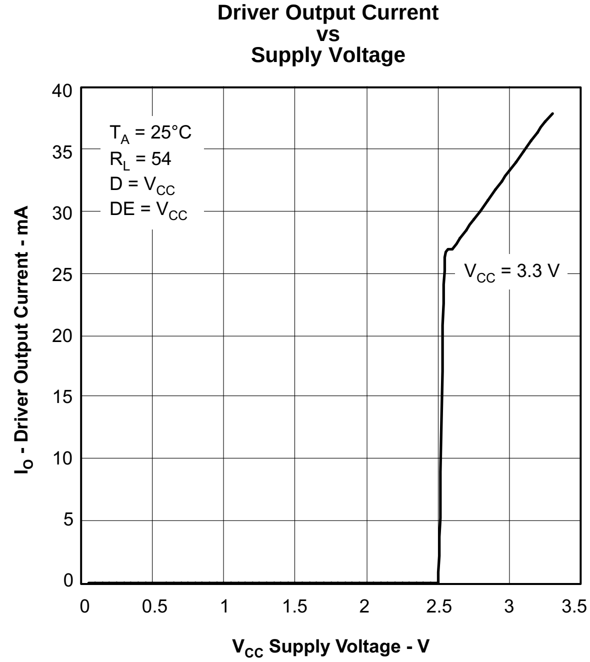


Figure 22.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD33D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD33DR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI
SN65HVD34D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD34DR	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD35D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI
SN65HVD35DR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65HVD33D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD34DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD35DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
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[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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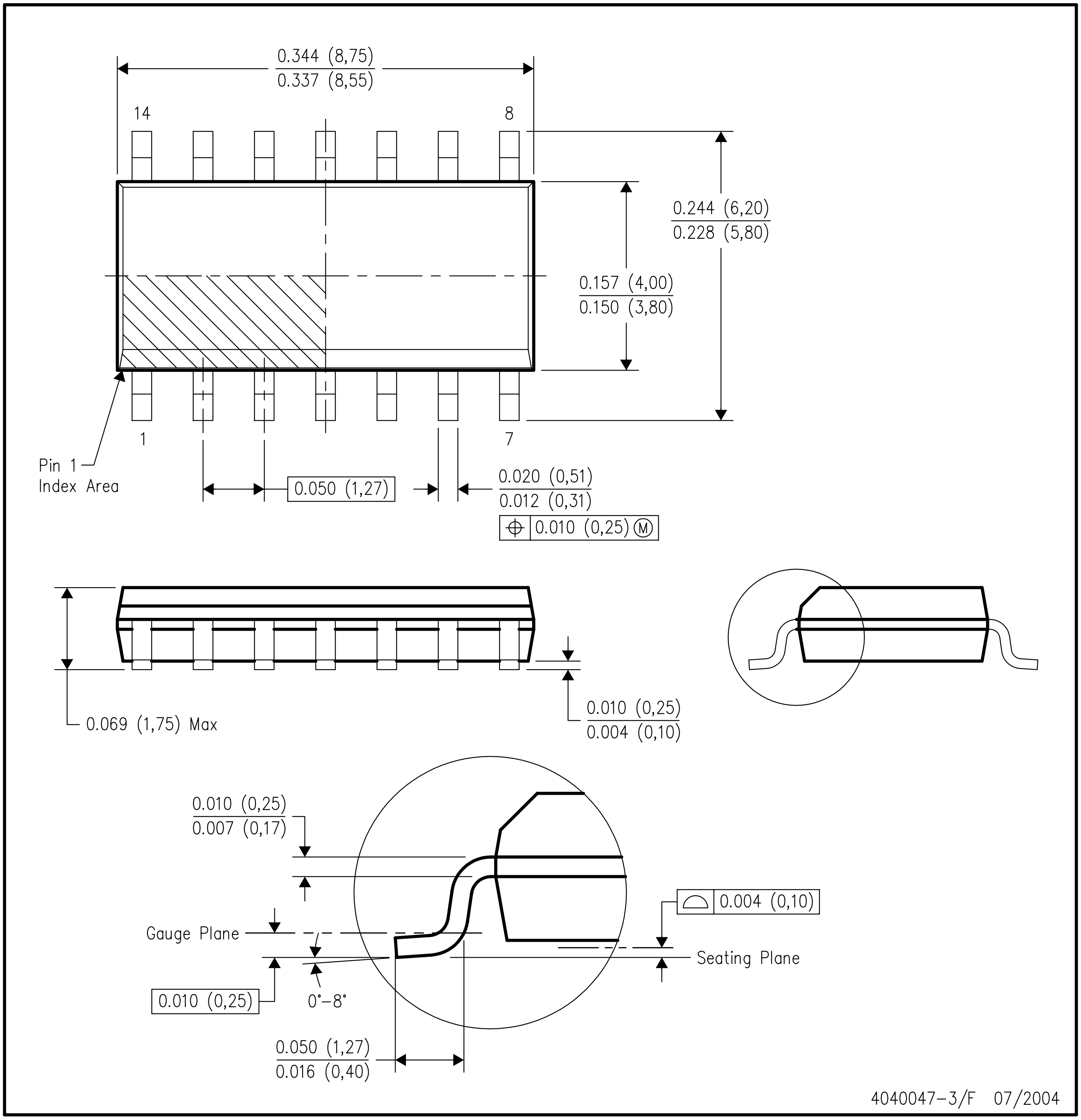
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

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