

### FEATURES

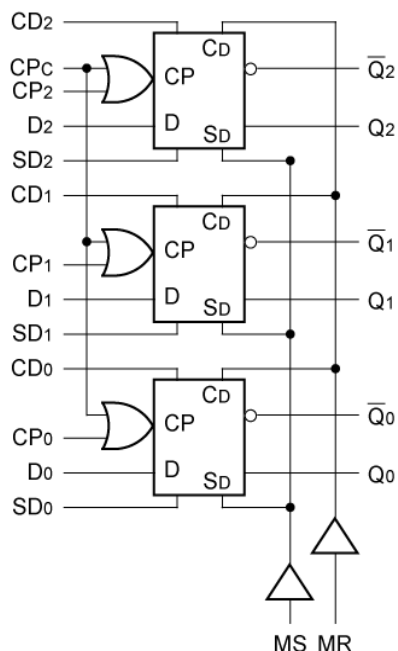
- Max. toggle frequency of 800MHz
- Differential outputs
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 150% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

### DESCRIPTION

The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CP<sub>c</sub>), as well as its own clock pulse (CP<sub>n</sub>). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CP<sub>c</sub> and CP<sub>n</sub> are LOW and enters the slave on the rising edge of either CP<sub>c</sub> or CP<sub>n</sub> (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SD<sub>n</sub>) and Direct Clear (CD<sub>n</sub>) signals. The MR, MS, SD<sub>n</sub> and DC<sub>n</sub> signals override the clock signals. The inputs on this device have 75kΩ pull-down resistors.

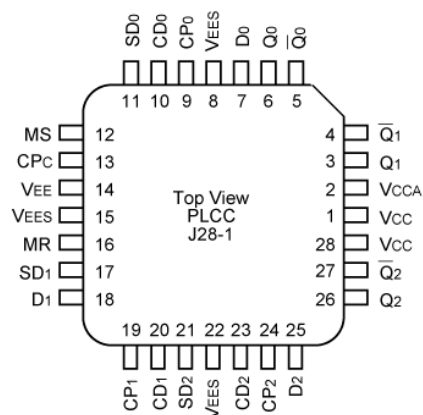
### BLOCK DIAGRAM



### PIN NAMES

Pin	Function
CP <sub>0</sub> – CP <sub>2</sub>	Individual Clock Inputs
CP <sub>c</sub>	Common Clock Input
D <sub>0</sub> – D <sub>2</sub>	Data Inputs
CD <sub>0</sub> – CD <sub>2</sub>	Individual Direct Clear Inputs
SD <sub>n</sub>	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q <sub>0</sub> – Q <sub>2</sub>	Data Outputs
Q <sub>0</sub> – Q <sub>2</sub>	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

## PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

## Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S331JC	J28-1	Commercial	SY100S331JC	Sn-Pb
SY100S331JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S331JC	Sn-Pb
SY100S331JZ <sup>(2)</sup>	J28-1	Commercial	SY100S331JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S331JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S331JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S331JY <sup>(2)</sup>	J28-1	Industrial	SY100S331JY with Pb-Free bar-line indicator	Matte-Sn
SY100S331JYTR <sup>(1, 2)</sup>	J28-1	Industrial	SY100S331JY with Pb-Free bar-line indicator	Matte-Sn

### Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

## TRUTH TABLES

Asynchronous Operation <sup>(1)</sup>					
Inputs					Outputs
D <sub>n</sub>	CP <sub>n</sub>	CP <sub>c</sub>	MS SD <sub>n</sub>	MR DC <sub>n</sub>	Q <sub>n</sub> (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

### NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

Synchronous Operation <sup>(1)</sup>					
Inputs					Outputs
D <sub>n</sub>	CP <sub>n</sub>	CP <sub>c</sub>	MS SD <sub>n</sub>	MR DC <sub>n</sub>	Q <sub>n</sub>
L	u	L	L	L	L
H	u	L	L	L	H
L	L	u	L	L	L
H	L	u	L	L	H
X	L	L	L	L	Q <sub>n</sub> (t)
X	H	X	L	L	Q <sub>n</sub> (t)
X	X	H	L	L	Q <sub>n</sub> (t)

### NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

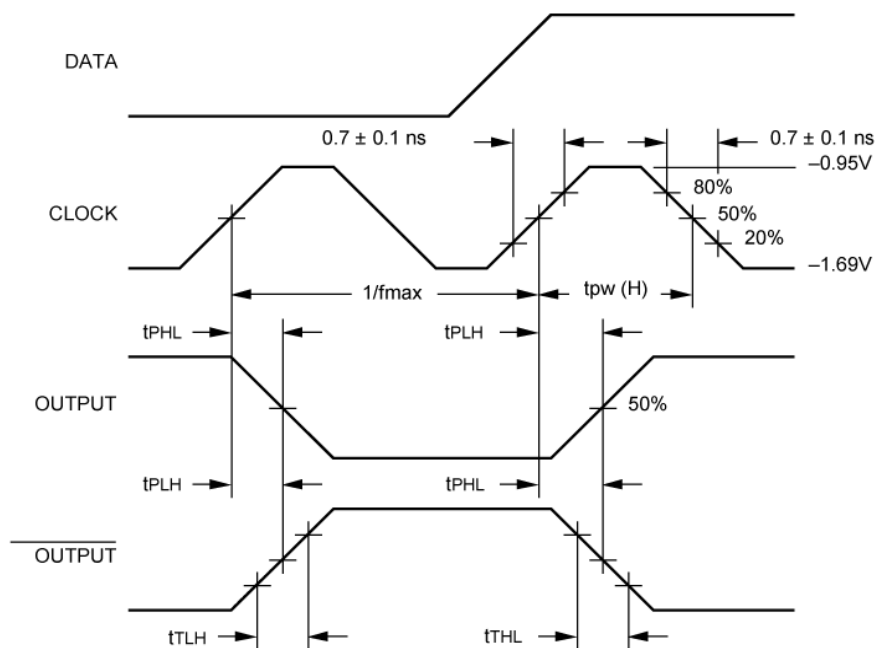
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$I_{IH}$	Input HIGH Current, All Inputs	—	—	200	$\mu A$	$V_{IN} = V_{IH} (Max.)$
$I_{EE}$	Power Supply Current	-80	-65	-35	mA	Inputs Open

## AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = -40^{\circ}C$		$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$f_{max}$	Toggle Frequency	800	—	800	—	800	—	800	—	MHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP <sub>c</sub> to Output	300	700	300	700	300	700	300	700	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP <sub>n</sub> to Output	300	700	300	700	300	700	300	700	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay CD <sub>n</sub> , SD <sub>n</sub> to Output	300	800	300	800	300	800	300	800	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay MS, MR to Output	300	900	300	900	300	900	300	900	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	300	900	ps	
$t_s$	Set-up Time D <sub>n</sub>	400	—	400	—	400	—	400	—	ps	
	CD <sub>n</sub> , SD <sub>n</sub> (Release Time)	500	—	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—	800	—		
$t_H$	Hold Time D <sub>n</sub>	300	—	300	—	300	—	300	—	ps	
$t_{pw} (H)$	Pulse Width HIGH CP <sub>n</sub> , CP <sub>c</sub> , DC <sub>n</sub> SD <sub>n</sub> , MR, MS	800	—	800	—	800	—	800	—	ps	

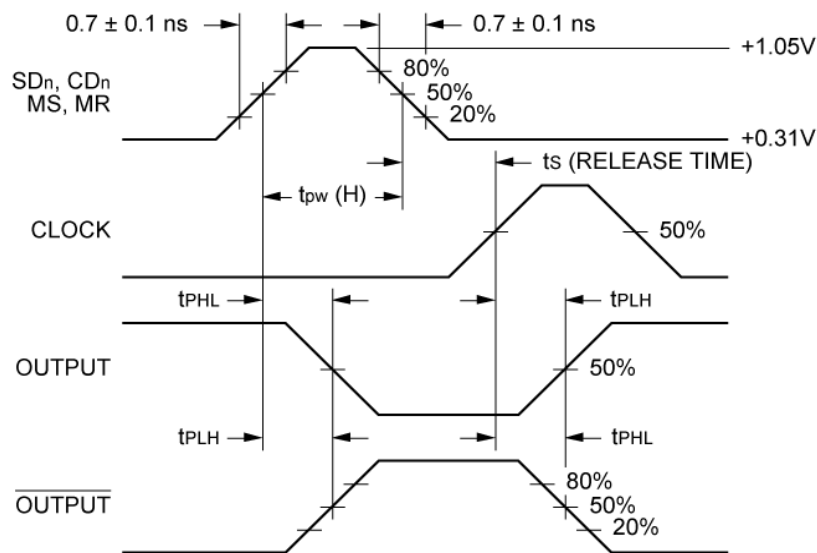
## TIMING DIAGRAMS



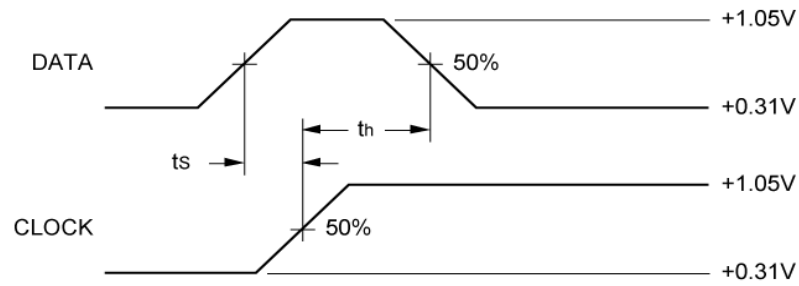
Propagation Delay (Clock) and Transition Times

**Note:**

$V_{\text{EE}} = -4.2\text{V}$  to  $-5.5\text{V}$  unless otherwise specified,  $V_{\text{CC}} = V_{\text{CCA}} = \text{GND}$



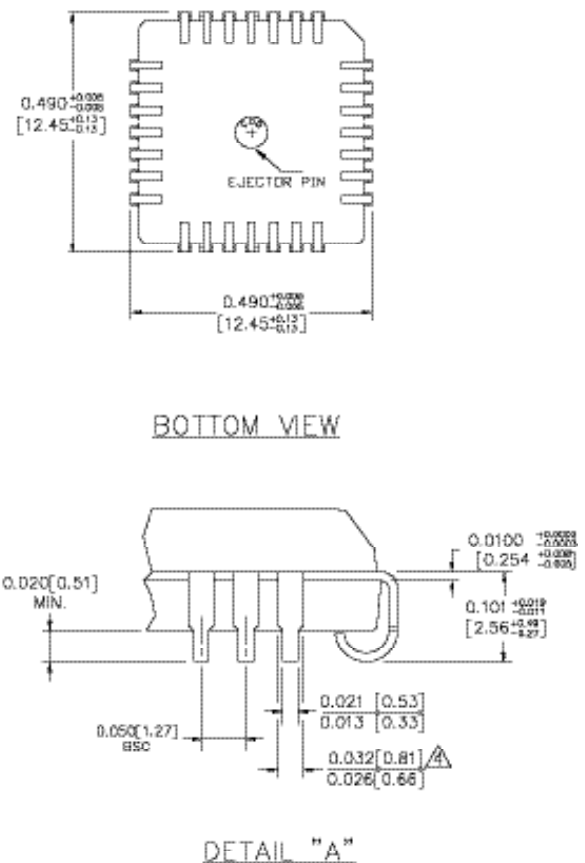
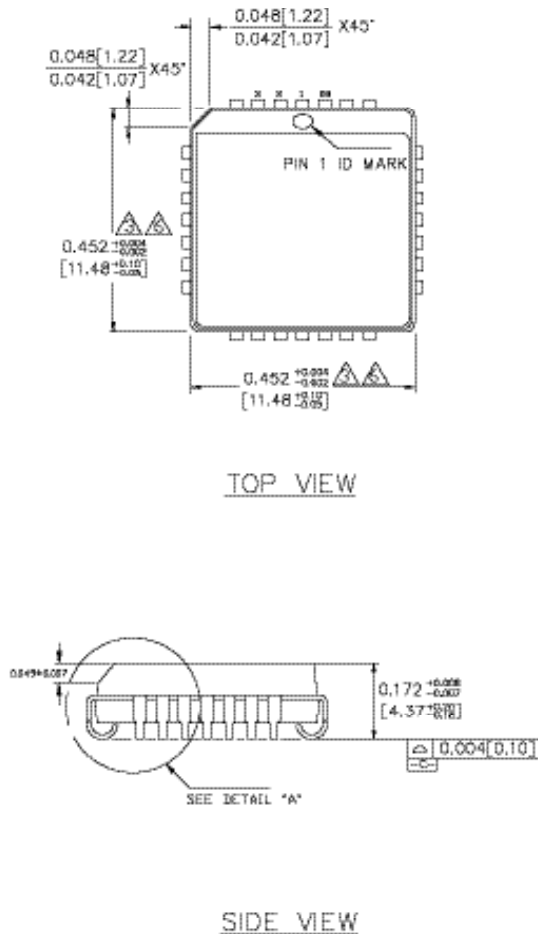
Propagation Delay (Sets and Resets)

**TIMING DIAGRAMS****Data Setup and Hold Time****Notes:**

$t_s$  is the minimum time before the transition of the clock that information must be present at the data input.

$t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

## 28-PIN PLCC (J28-1)



### NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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