RJM0404JSC

Silicon N/P Channel Power MOS FET (6 in 1 Type)
High Speed Power Switching

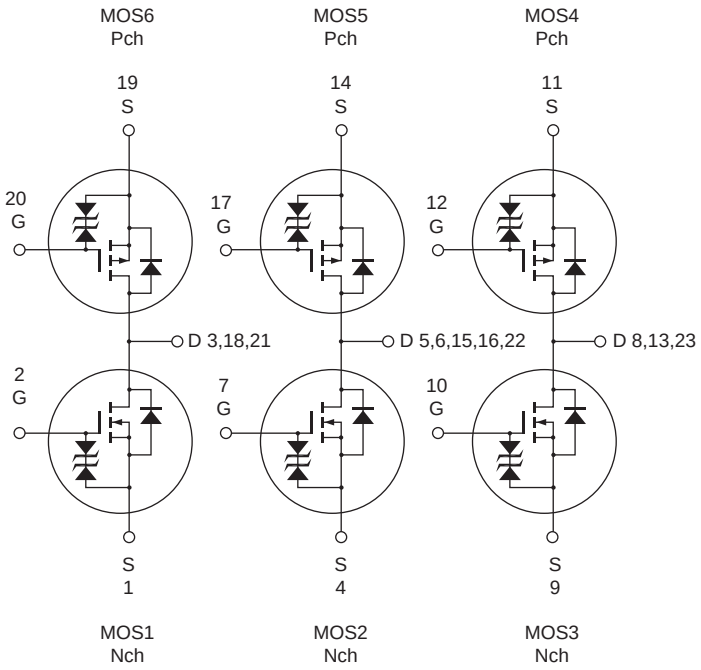
R07DS0338EJ0500
Rev.5.00
May 11, 2011

Features

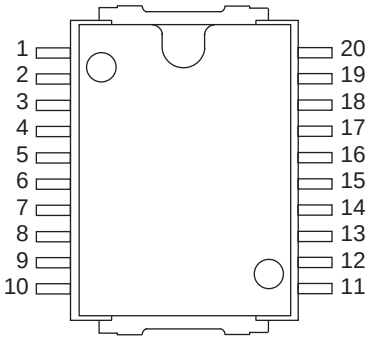
- For Automotive applications
- AEC-Q101 compliant
- N/P Channel MOS FET (6 in 1 Type). High density mounting
- Low on-resistance
- Capable of 4.5 V gate drive

Outline

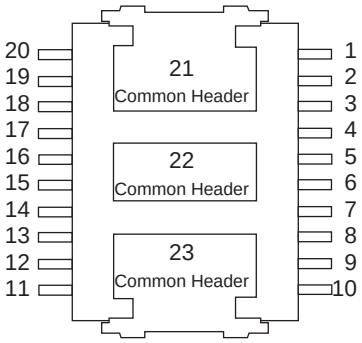
RENESAS Package Code: PRSP0020DF-A
(Package Name: HSOP-20)



Pin Arrangement

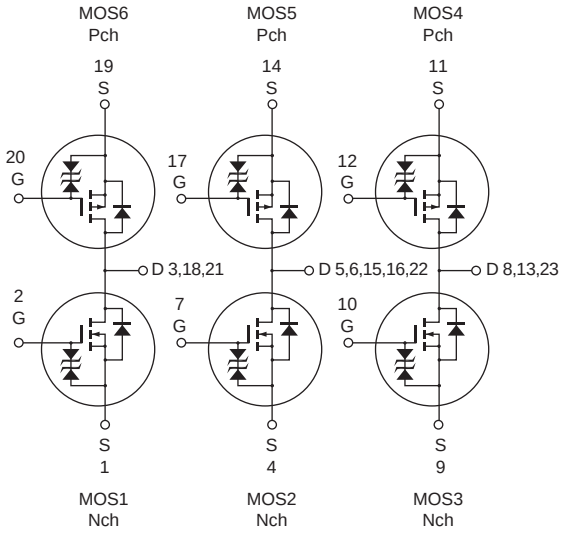


(Top View)



(Bottom View)

No.		
1	MOS1	Source
2	MOS1	Gate
3, 18	MOS1, 6	Drain
4	MOS2	Source
5, 6, 15, 16	MOS2, 5	Drain
7	MOS2	Gate
8, 13	MOS3, 4	Drain
9	MOS3	Source
10	MOS3	Gate
11	MOS4	Source
12	MOS4	Gate
14	MOS5	Source
17	MOS5	Gate
19	MOS6	Source
20	MOS6	Gate
21	MOS1, 6	Drain (Header)
22	MOS2, 5	Drain (Header)
23	MOS3, 4	Drain (Header)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2, 3 (Nch)	MOS4, 5, 6 (Pch)	
Drain to source voltage	V_{DSS}	40	–40	V
Gate to source voltage	V_{GSS}	+20 / –5	–20 / +5	V
Drain current	I_D	20	–20	A
Drain peak current	I_D (pulse) Note1	80	–80	A
Avalanche current	I_{AP} Note3	20	–20	A
Avalanche energy	E_{AR} Note3	53	53	mJ
Channel dissipation	Pch Note2	54	54	W
Channel temperature	Tch Note4	175	175	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10μs duty cycle ≤ 1%
2. Tc = 25°C : 1 Drive Operation.
3. Tch = 25°C, Rg ≥ 50 Ω
4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θch-c: 2.78°C/W

Electrical Characteristics

• MOS1, MOS2, MOS3 (N Channel)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	V_{DS} = 40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = +20 / –5 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	17	21	mΩ	I_D = 10 A, V_{GS} = 10 V Note5
		—	24	34	mΩ	I_D = 10 A, V_{GS} = 4.5 V Note5
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	230	—	pF	
Reverse transfer capacitance	Crss	—	100	—	pF	
Total gate charge	Qg	—	23	—	nC	V_{DD} = 25 V, V_{GS} = 10 V, I_D = 20 A
Gate to source charge	Qgs	—	3	—	nC	
Gate to drain charge	Qgd	—	4	—	nC	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 10 V, I_D = 10 A, V_{DD} ≅ 20 V, R_L = 2 Ω, R_G = 4.7 Ω
Rise time	t_r	—	35	—	ns	
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.92	1.2	V	I_F = 20 A, V_{GS} = 0 Note5
Body-drain diode reverse recovery time	t_{rr}	—	20	—	ns	I_F = 20 A, V_{GS} = 0, di_F/dt = 50 A/μs

Note: 5. Pulse test

• MOS4, MOS5, MOS6 (P Channel)

(Ta = 25°C)

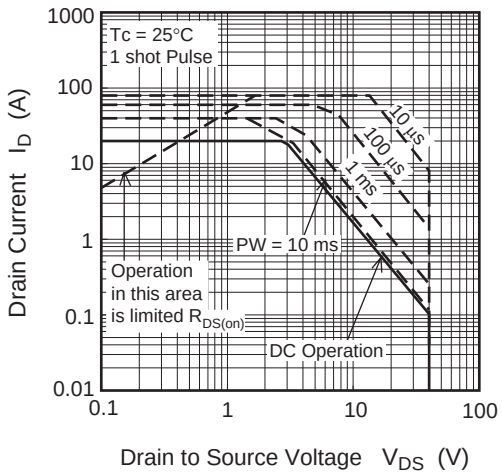
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I_{DSS}	—	—	–10	μA	V_{DS} = –40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = –20 / +5 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	34	42	mΩ	I_D = –10 A, V_{GS} = –10 V Note6
		—	48	68	mΩ	I_D = –10 A, V_{GS} = –4.5 V Note6
Input capacitance	Ciss	—	1500	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	230	—	pF	
Reverse transfer capacitance	Crss	—	140	—	pF	
Total gate charge	Qg	—	25	—	nC	V_{DD} = –25 V, V_{GS} = –10 V, I_D = –20 A
Gate to source charge	Qgs	—	5	—	nC	
Gate to drain charge	Qgd	—	4	—	nC	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	V_{GS} = –10 V, I_D= –10 A, V_{DD} ≅ –20 V, R_L =2 Ω, R_G = 4.7 Ω
Rise time	t_r	—	55	—	ns	
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	20	—	ns	
Body-drain diode forward voltage	V_{DF}	—	–0.97	–1.26	V	I_F = –20 A, V_{GS} = 0 Note6
Body-drain diode reverse recovery time	t_{rr}	—	30	—	ns	I_F = –20 A, V_{GS} = 0, di_F/dt = 50 A/μs

Note: 6. Pulse test

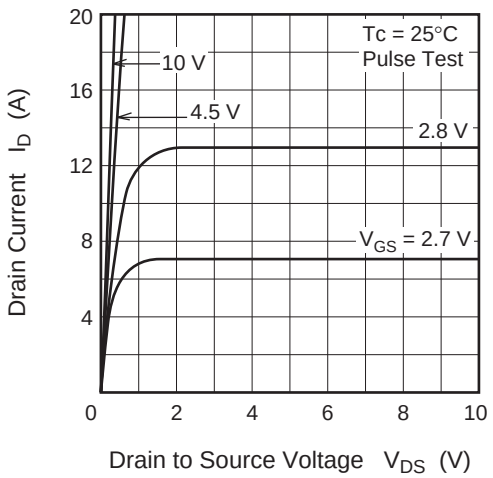
Main Characteristics

• **MOS1, 2, 3 (Nch)**

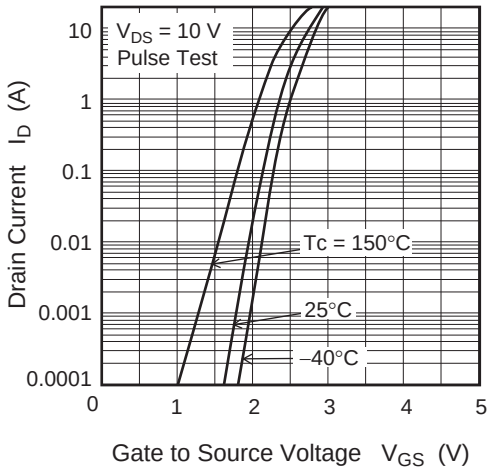
Maximum Safe Operation Area



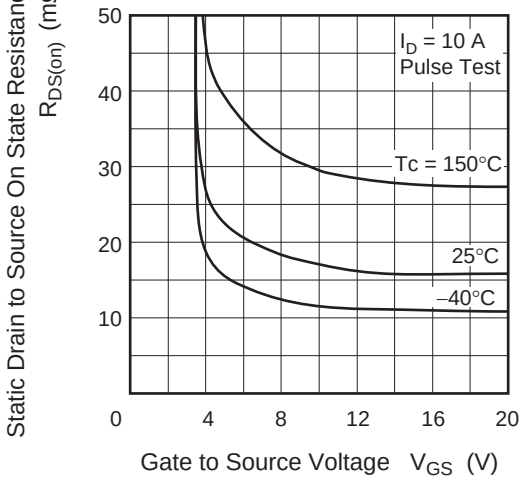
Typical Output Characteristics



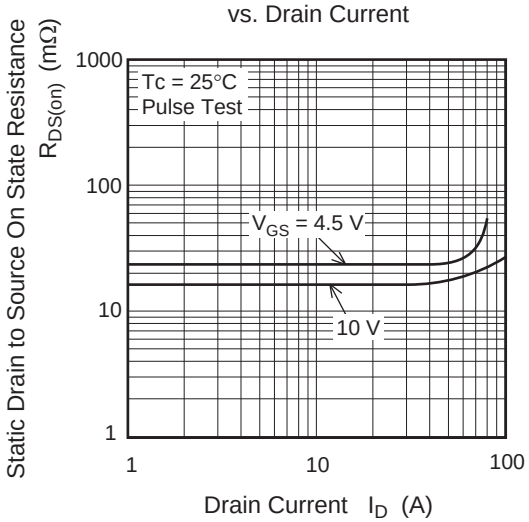
Typical Transfer Characteristics



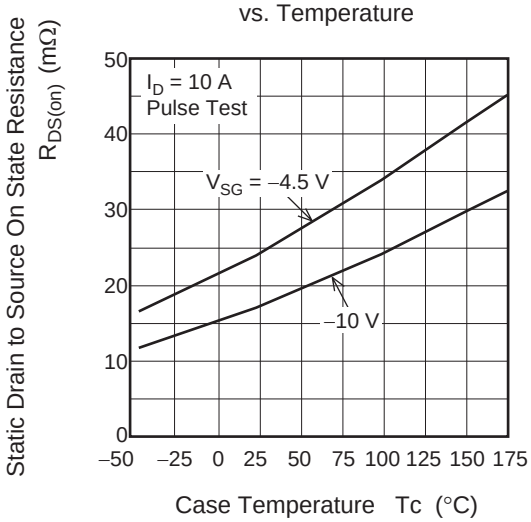
Static Drain to Source On State Resistance vs. Gate to Source Voltage



Static Drain to Source State On Resistance vs. Drain Current

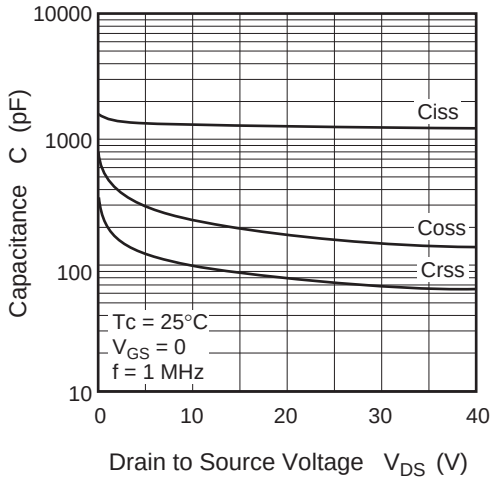


Static Drain to Source on State Resistance vs. Temperature

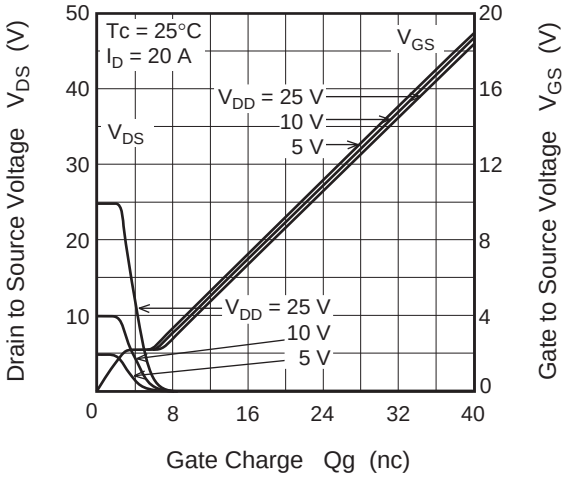


• **MOS1, 2, 3(Nch)**

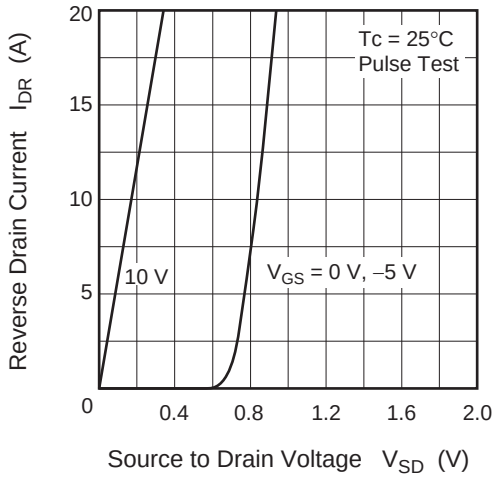
Typical Capacitance vs.
Drain to Source Voltage



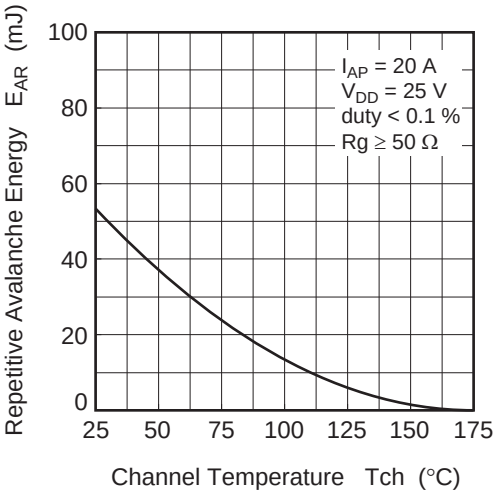
Dynamic Input Characteristics



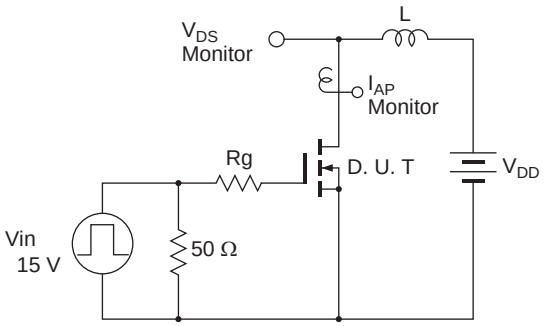
Reverse Drain Current vs.
Source to Drain Voltage



Avalanche Energy vs.
Channel Temperature Derating

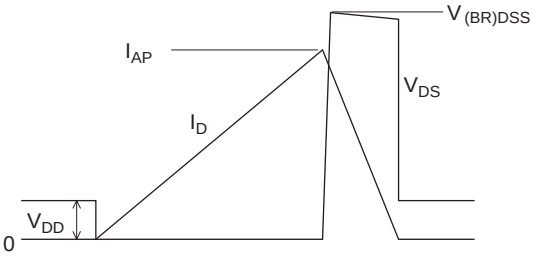


Avalanche Test Circuit



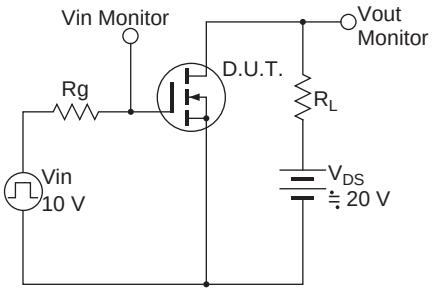
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

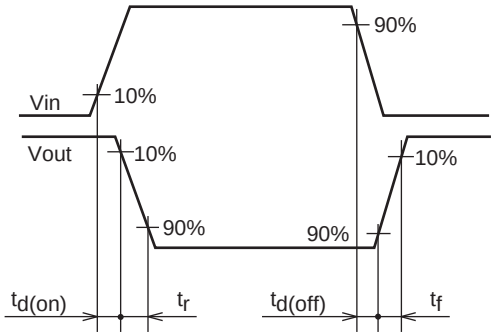


• **MOS1, 2, 3 (Nch)**

Switching Time Test Circuit

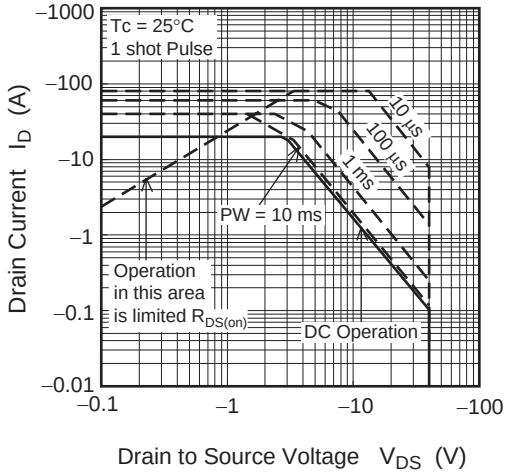


Switching Time Waveform

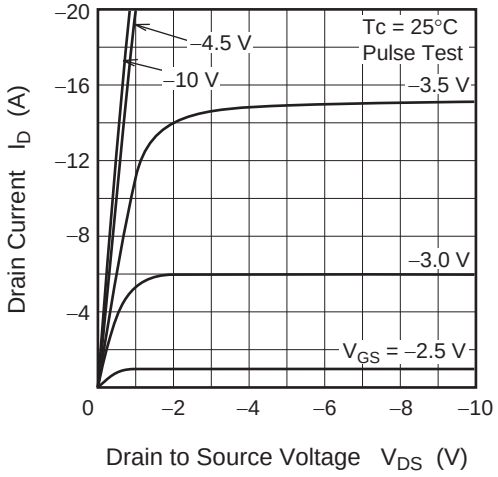


• MOS4, 5, 6 (Pch)

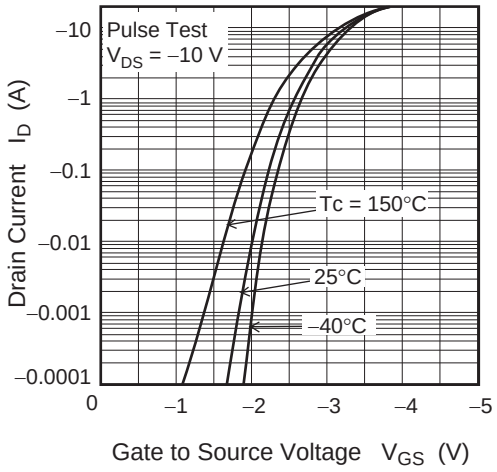
Maximum Safe Operation Area



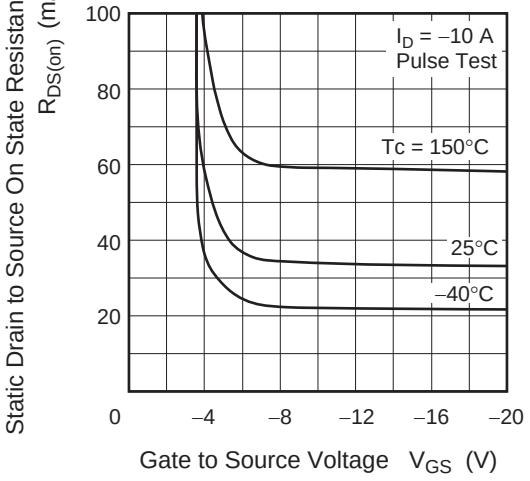
Typical Output Characteristics



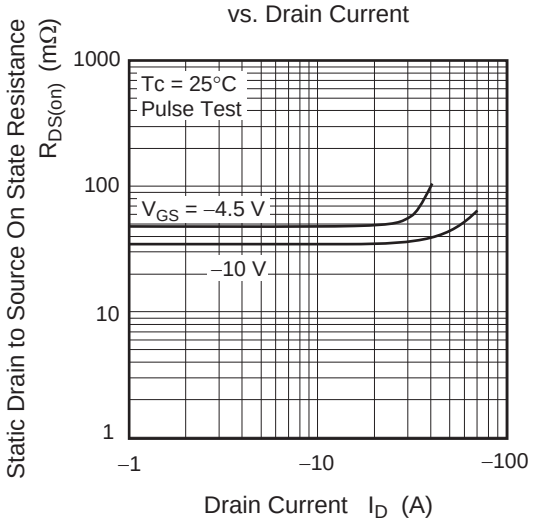
Typical Transfer Characteristics



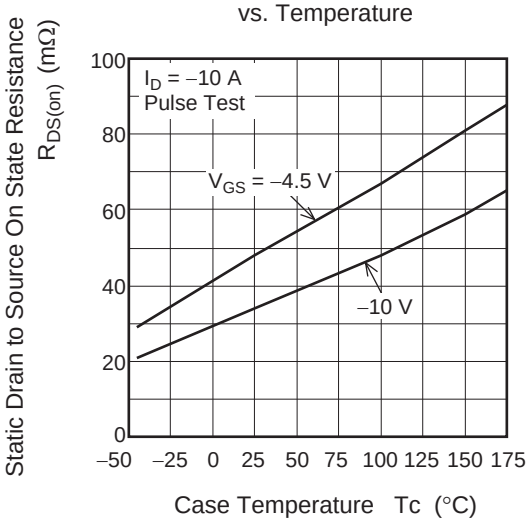
Static Drain to Source On State Resistance vs. Gate to Source Voltage



Static Drain to Source On State Resistance vs. Drain Current

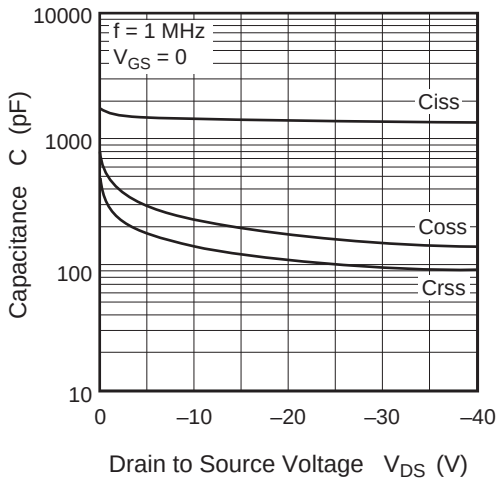


Static Drain to Source on State Resistance vs. Temperature

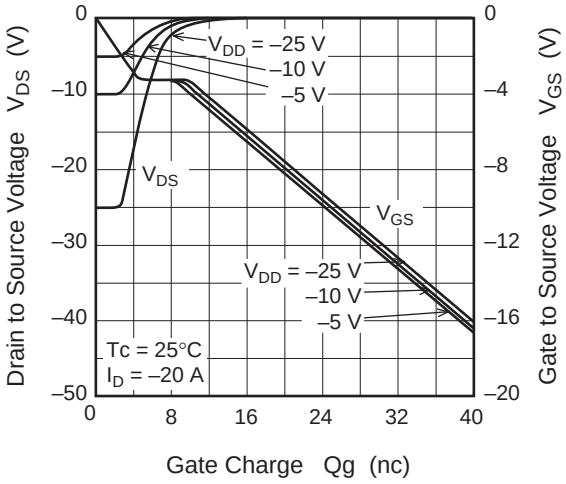


• MOS4, 5, 6 (Pch)

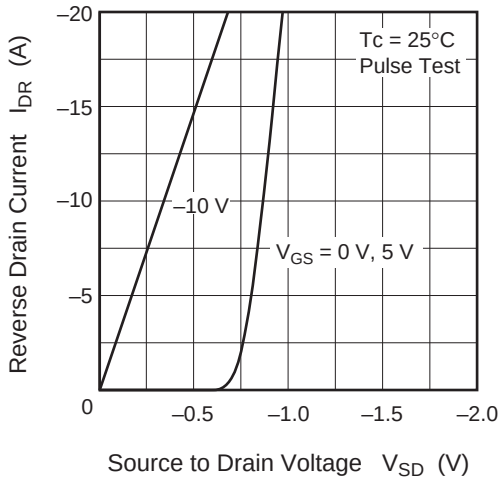
Typical Capacitance vs.
Drain to Source Voltage



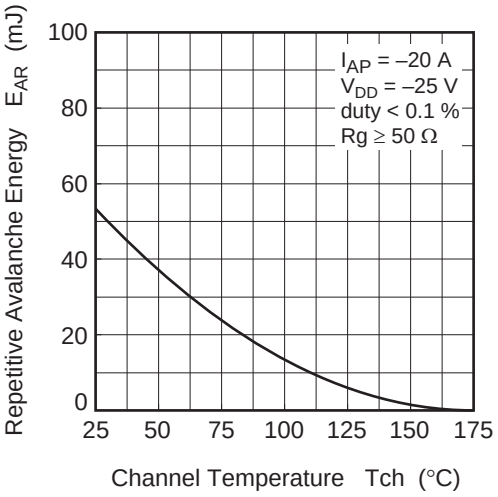
Dynamic Input Characteristics



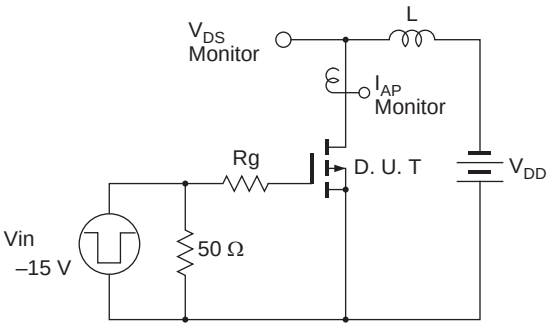
Reverse Drain Current vs.
Source to Drain Voltage



Avalanche Energy vs.
Channel Temperature Derating

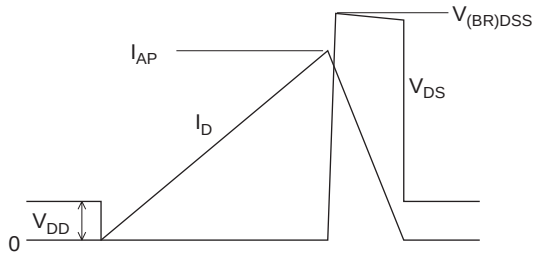


Avalanche Test Circuit



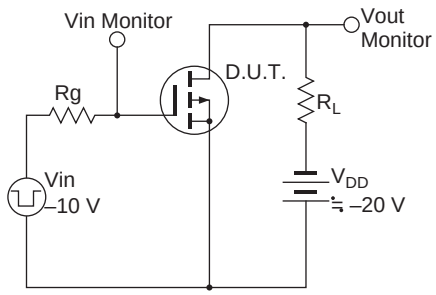
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

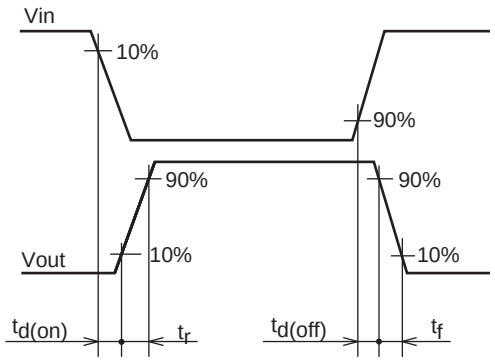


• **MOS4, 5, 6 (Pch)**

Switching Time Test Circuit

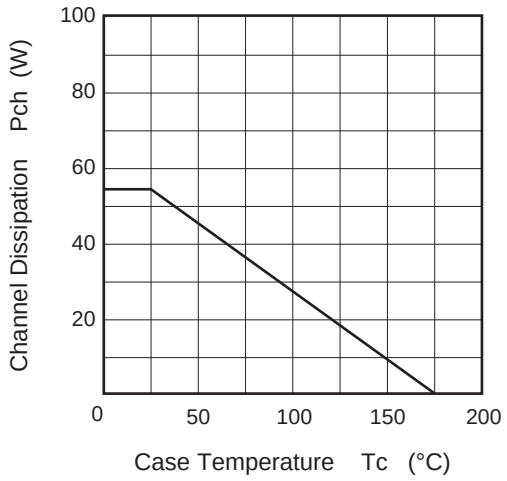


Switching Time Waveform

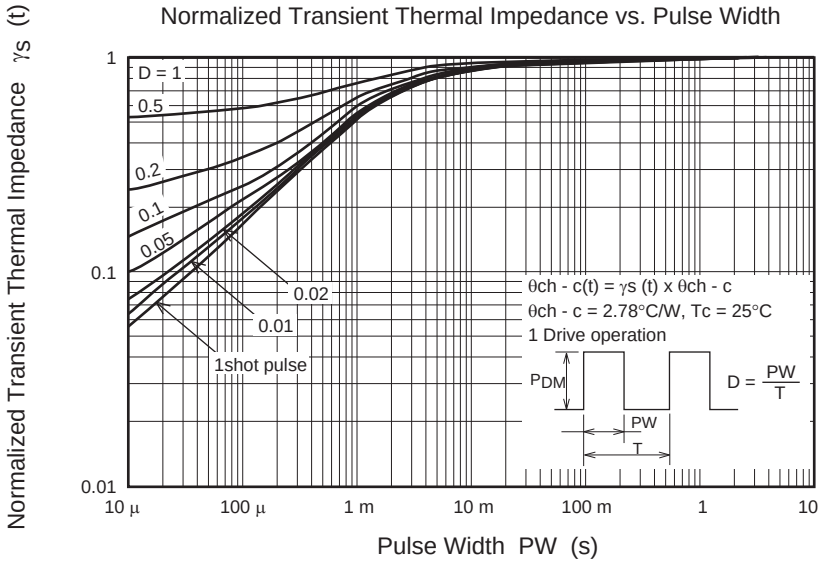


• Common

Power vs. Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
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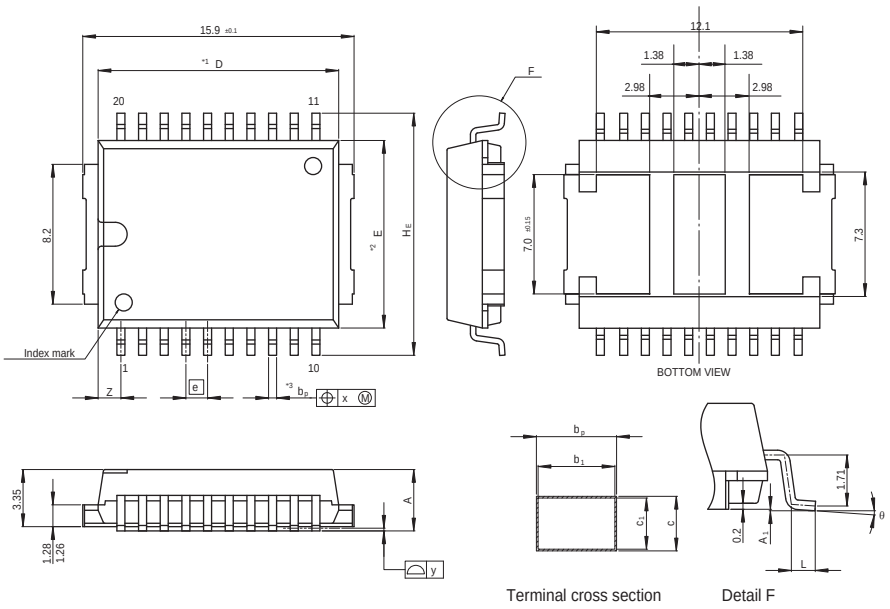

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.95	14.1	14.25
E	10.9	11.0	11.1
A_2	—	—	—
A_1	0.01	0.05	0.10
A	—	—	3.6
b_p	0.40	0.47	0.53
b_1	—	0.45	—
c	0.28	0.32	0.37
c_1	—	0.30	—
θ	0°	—	8°
H_E	14.0	14.2	14.4
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	1.8
L	0.65	0.8	0.95
L_1	—	—	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJM0404JSC-00-12	700 pcs	Tray

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SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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