

# RJK0632JPD

Silicon N Channel MOS FET  
High Speed Power Switching

R07DS0342EJ0100

Rev.1.00

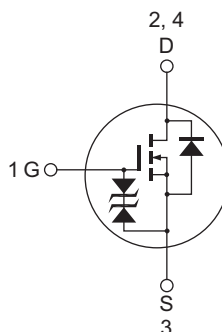
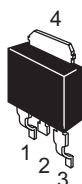
May 11, 2011

## Features

- For Automotive application
- AEC-Q101 compliant
- Low on-resistance :  $R_{DS(on)} = 29 \text{ m}\Omega$  typ.
- Capable of 4.5 V gate drive
- Low input capacitance :  $C_{iss} = 440 \text{ pF}$  typ.

## Outline

RENESAS Package code: PRSS0004ZD-C  
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

| Item                                        | Symbol                            | Value       | Unit             |
|---------------------------------------------|-----------------------------------|-------------|------------------|
| Drain to source voltage                     | $V_{DS}$                          | 60          | V                |
| Gate to source voltage                      | $V_{GS}$                          | $\pm 20$    | V                |
| Drain current                               | $I_D$                             | 20          | A                |
| Drain peak current                          | $I_D$ (pulse) <sup>Note1</sup>    | 80          | A                |
| Body-drain diode reverse drain current      | $I_{DR}$                          | 20          | A                |
| Body-drain diode reverse drain peak current | $I_{DR}$ (pulse) <sup>Note1</sup> | 80          | A                |
| Avalanche current                           | $I_{AP}$ <sup>Note2</sup>         | 14          | A                |
| Avalanche energy                            | $E_{AR}$ <sup>Note2</sup>         | 16.8        | mJ               |
| Channel dissipation                         | $P_{ch}$ <sup>Note3</sup>         | 25          | W                |
| Channel temperature                         | $T_{ch}$ <sup>Note4</sup>         | 175         | $^\circ\text{C}$ |
| Storage temperature                         | $T_{stg}$                         | -55 to +150 | $^\circ\text{C}$ |

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

2.  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$

3.  $T_c = 25^\circ\text{C}$

4. AEC-Q101 compliant

## Thermal Impedance Characteristics

- Channel to case thermal impedance  $\theta_{ch-c}$ :  $6.00^\circ\text{C/W}$

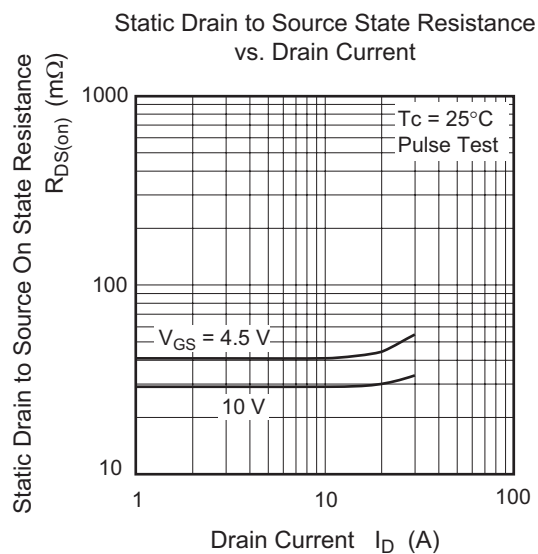
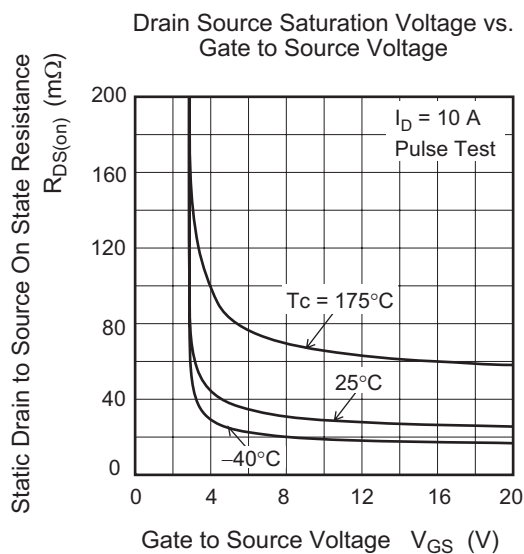
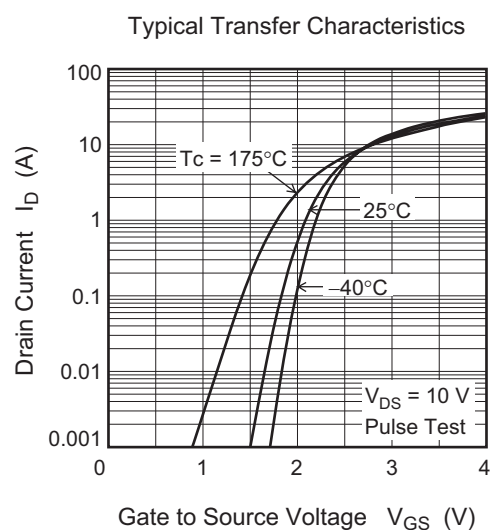
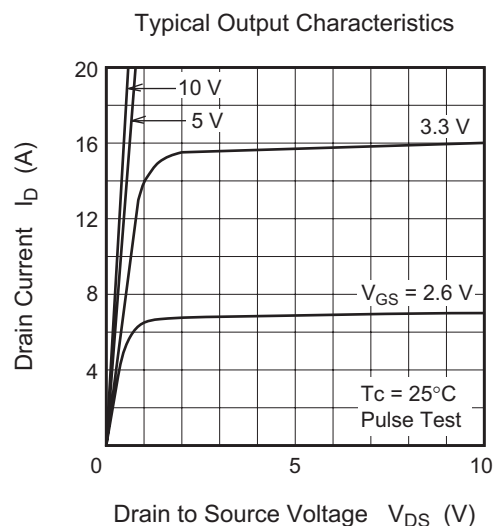
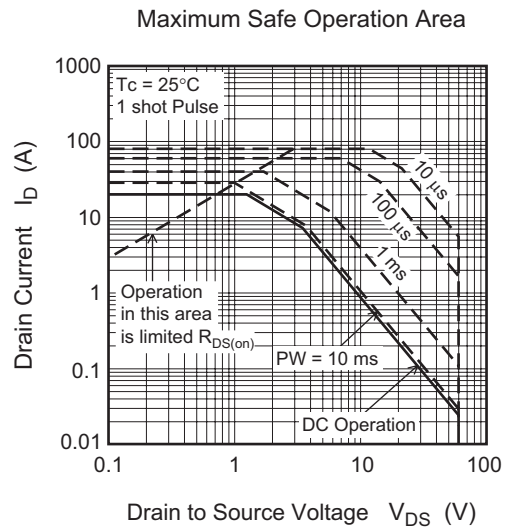
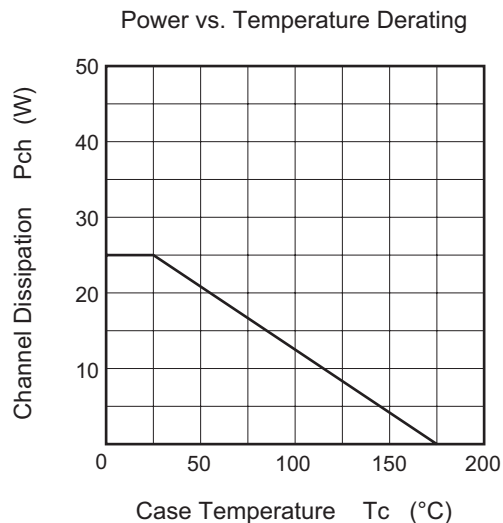
## Electrical Characteristics

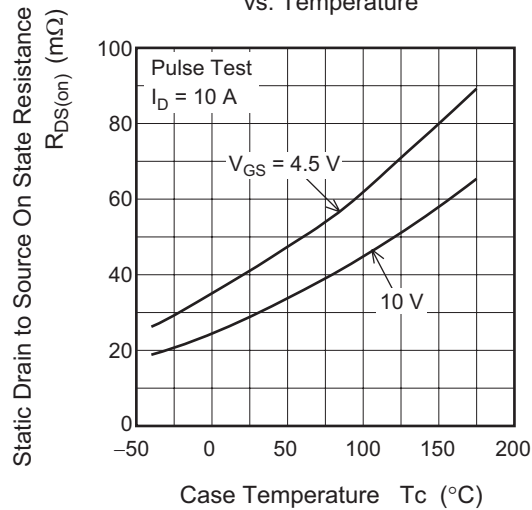
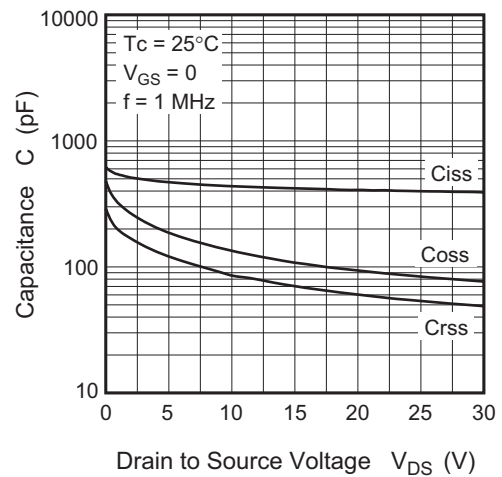
(Ta = 25°C)

| Item                                       | Symbol        | Min | Typ  | Max  | Unit | Test Conditions                                                                         |
|--------------------------------------------|---------------|-----|------|------|------|-----------------------------------------------------------------------------------------|
| Gate to source leak current                | $I_{GSS}$     | —   | —    | ±10  | μA   | $V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0$                                              |
| Zero gate voltage drain current            | $I_{DSS}$     | —   | —    | 1    | μA   | $V_{DS} = 60 \text{ V}$ , $V_{GS} = 0$                                                  |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 1.0 | —    | 2.0  | V    | $I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$                                          |
| Static drain to source on state resistance | $R_{DS(on)}$  | —   | 29   | 35   | mΩ   | $I_D = 10 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note5</sup>                         |
| Static drain to source on state resistance | $R_{DS(on)}$  | —   | 41   | 55   | mΩ   | $I_D = 10 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note5</sup>                        |
| Input capacitance                          | $C_{iss}$     | —   | 440  | —    | pF   | $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$<br>$f = 1 \text{ MHz}$                           |
| Output capacitance                         | $C_{oss}$     | —   | 135  | —    | pF   |                                                                                         |
| Reverse transfer capacitance               | $C_{rss}$     | —   | 85   | —    | pF   |                                                                                         |
| Total gate charge                          | $Q_g$         | —   | 10   | —    | nC   | $V_{DD} = 25 \text{ V}$ , $V_{GS} = 10 \text{ V}$ ,<br>$I_D = 20 \text{ A}$             |
| Gate to source charge                      | $Q_{gs}$      | —   | 1.4  | —    | nC   |                                                                                         |
| Gate to drain charge                       | $Q_{gd}$      | —   | 3.0  | —    | nC   |                                                                                         |
| Turn-on delay time                         | $t_{d(on)}$   | —   | 8.5  | —    | ns   | $I_D = 10 \text{ A}$ , $R_L = 3 \Omega$<br>$V_{GS} = 10 \text{ V}$ , $R_G = 4.7 \Omega$ |
| Rise time                                  | $t_r$         | —   | 12   | —    | ns   |                                                                                         |
| Turn-off delay time                        | $t_{d(off)}$  | —   | 40   | —    | ns   |                                                                                         |
| Fall time                                  | $t_f$         | —   | 11   | —    | ns   |                                                                                         |
| Body-drain diode forward voltage           | $V_{DF}$      | —   | 0.95 | 1.24 | V    | $I_F = 20 \text{ A}$ , $V_{GS} = 0$ <sup>Note5</sup>                                    |
| Body-drain diode reverse recovery time     | $t_{rr}$      | —   | 30   | —    | ns   | $I_F = 20 \text{ A}$ , $V_{GS} = 0$ ,<br>$di_F/dt = 100 \text{ A}/\mu\text{s}$          |

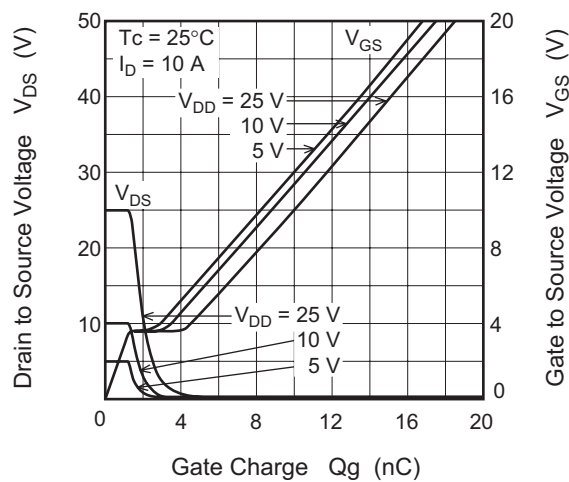
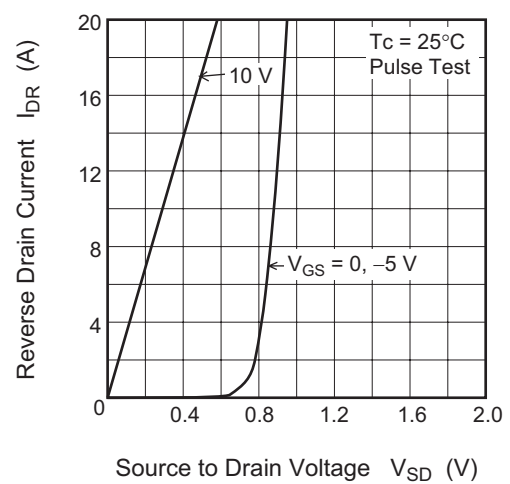
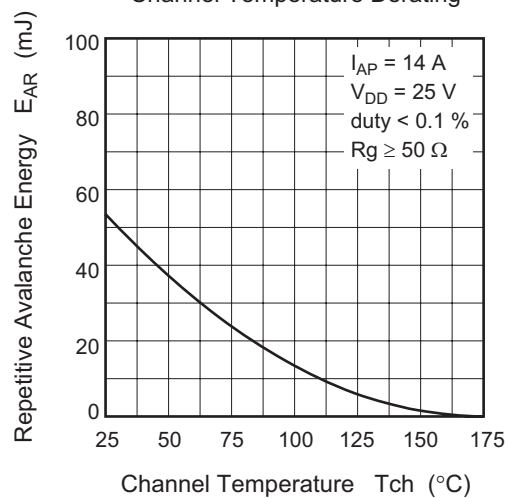
Note: 5. Pulse test

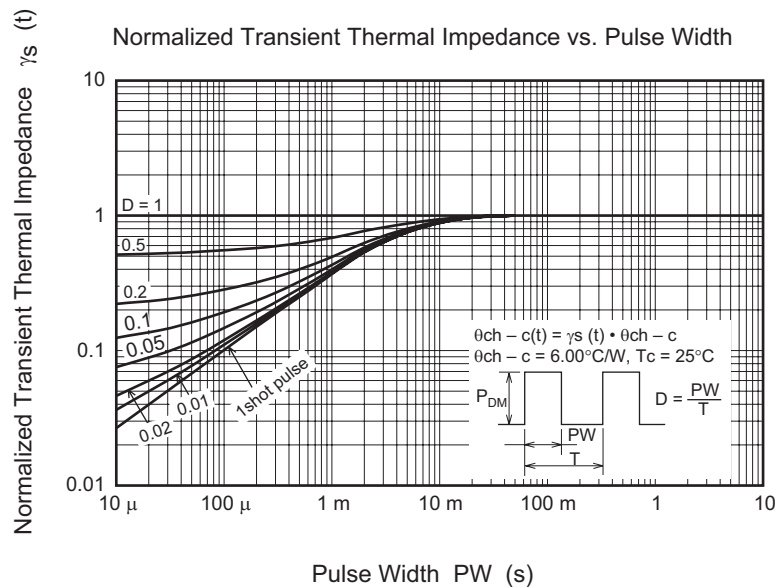
## Main Characteristics



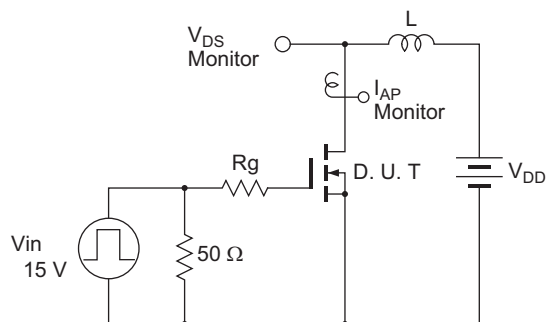
Static Drain to Source on State Resistance  
vs. TemperatureTypical Capacitance vs.  
Drain to Source Voltage

Dynamic Input Characteristics

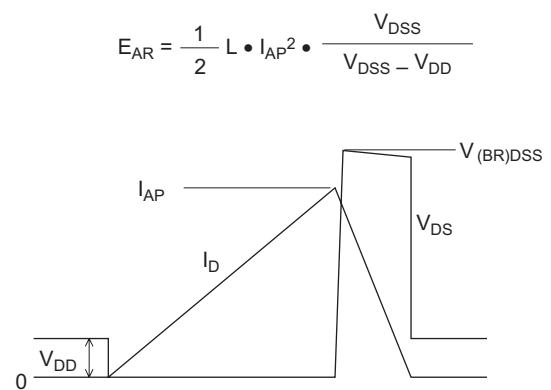
Reverse Drain Current vs.  
Source to Drain VoltageAvalanche Energy vs.  
Channel Temperature Derating



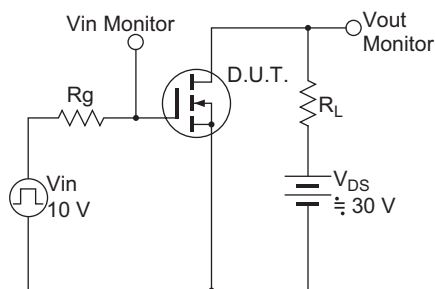
Avalanche Test Circuit



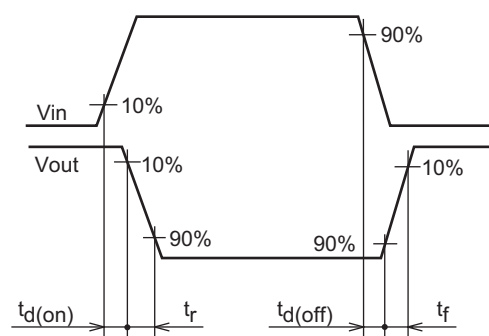
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform





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2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
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Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**  
11F., Samik Laviel' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141