



16-Port, 36V Constant-Current LED Driver

MAX6971

General Description

The MAX6971 serial-interfaced LED driver provides 16 open-drain, constant-current-sinking LED driver outputs rated at 36V. The MAX6971 operates from a 3V to 5.5V supply. The MAX6971 supply and the LEDs' supply or supplies can power up in any order. The constant-current outputs are programmed together to up to 55mA using a single external resistor. The MAX6971 operates with a 25Mb, industry-standard, 4-wire serial interface.

The MAX6971 uses the industry-standard, shift-register-plus-latch-type serial interface. The driver accepts data shifted into a 16-bit shift register using data input DIN and clock input CLK. Input data appears at the DOUT output 16 clock cycles later to allow cascading of multiple MAX6971s. The latch-enable input, LE, loads the 16 bits of shift register data into a 16-bit output latch to set which LEDs are on and which are off. The output-enable, $\overline{OE}$, gates all 16 outputs on and off, and is fast enough to be used as a PWM input for LED intensity control.

For applications requiring LED fault detection, refer to the MAX6983*, which automatically detects open-circuit LEDs.

For safety-related applications requiring a watchdog timer, refer to the MAX6983, which includes a fail-safe feature that blanks the display if the serial interface becomes inactive for more than 1s.

The MAX6971 is one of a family of 12 shift-register-plus-latch-type LED drivers. The family includes 8-port and 16-port types, with 5.5V- or 36V-rated LED outputs, with and without open-circuit LED detection and watchdog. All versions operate from a 3V to 5.5V supply, and are specified over the -40°C to +125°C temperature range.

Applications

Variable Message Signs
Marquee Displays
Point-of-Order Signs
Traffic Signs
Gaming Features
Architectural Lighting

*Future product—contact factory for availability.

Features

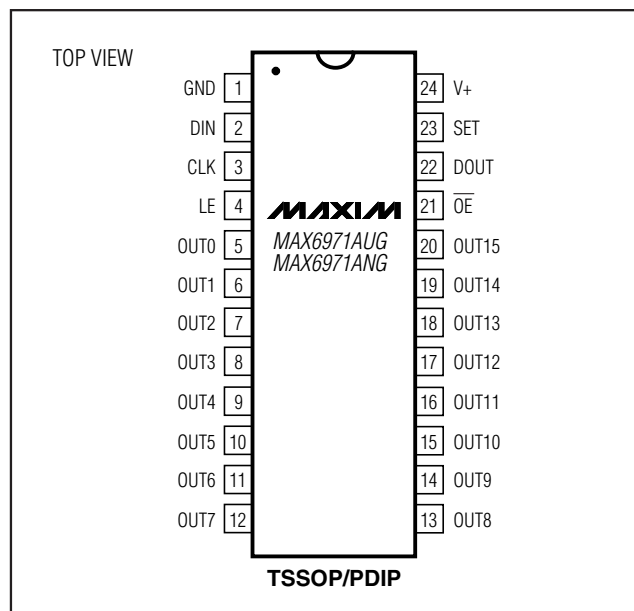
- ◆ 25Mb, Industry-Standard, 4-Wire Serial Interface
- ◆ 3V to 5.5V Logic Supply
- ◆ 16 Constant-Current LED Outputs Rated at 36V
- ◆ Up to 55mA Continuous Current per Output
- ◆ Output Current Programmed by Single Resistor
- ◆ 3% Current Matching Between Outputs
- ◆ 6% Current Matching Between ICs
- ◆ High-Dissipation, 24-Pin Packages
- ◆ -40°C to +125°C Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6971AUG	-40°C to +125°C	24 TSSOP
MAX6971ANG	-40°C to +125°C	24 Narrow PDIP

Typical Application Circuit and Selector Guide appear at end of data sheet.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

Voltage with respect to GND.

V+	-0.3V to +6V
OUT_	-0.3V to +40V
DIN, CLK, LE, $\overline{OE}$, SET	-0.3V to (V+ + 0.3V)
DOUT Current	±10mA
OUT_ Sink Current	60mA
Total GND Current	960mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

24-Pin TSSOP (derate 12.2mW/ $^\circ\text{C}$ over $+70^\circ\text{C}$)	975mW
24-Pin PDIP (derate 13.3mW/ $^\circ\text{C}$ over $+70^\circ\text{C}$)	1067mW
Operating Temperature Range	 -40°C to $+125^\circ\text{C}$
Junction Temperature	 $+150^\circ\text{C}$
Storage Temperature Range	 -65°C to $+150^\circ\text{C}$
Lead Temperature (soldering, 10s)	 $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, $V_+ = 3\text{V}$ to 5.5V , $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_+ = 5\text{V}$, $T_A = +25^\circ\text{C}$.)
(Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_+		3.0		5.5	V
Output Voltage	V_{OUT}				36	V
Standby Current (Interface Idle, All Output Ports High Impedance, $R_{\text{SET}} = 360\Omega$)	I_+	All logic inputs at V_+ or GND, DOUT unloaded		5.7	8	mA
Standby Current (Interface Running, All Output Ports High Impedance, $R_{\text{SET}} = 360\Omega$)	I_+	$f_{\text{CLK}} = 5\text{MHz}$, $\overline{OE} = V_+$, DIN and LE = V_+ or GND, DOUT unloaded		6	8.5	mA
Supply Current (Interface Idle, All Output Ports Active Low, $R_{\text{SET}} = 360\Omega$)	I_+	All logic inputs at V_+ or GND, DOUT unloaded		18	25	mA
Input High Voltage DIN, CLK, LE, $\overline{OE}$	V_{IH}		0.7 x V_+			V
Input Low Voltage DIN, CLK, LE, $\overline{OE}$	V_{IL}				0.3 x V_+	V
Hysteresis Voltage DIN, CLK, LE, $\overline{OE}$	ΔV_{I}			0.8		V
Input Leakage Current DIN, CLK, LE, $\overline{OE}$	$I_{\text{IH}}, I_{\text{IL}}$		-1		+1	μA
Output High-Voltage DOUT	V_{OH}	$I_{\text{SOURCE}} = 4\text{mA}$	V_+ - 0.5V			V
Output Low Voltage	V_{OL}	$I_{\text{SINK}} = 4\text{mA}$			0.5	V
Output Current OUT_	I_{OUT}	$V_+ = 3\text{V}$ to 5.5V , $V_{\text{OUT}} = 0.8\text{V}$ to 2.5V , $R_{\text{SET}} = 360\Omega$	37	50	61	mA
Output Leakage Current OUT_	I_{LEAK}	$\overline{OE} = V_+$			1	μA

Note 1: All parameters tested at $T_A = +25^\circ\text{C}$. Specifications over temperature are guaranteed by design.

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5V TIMING CHARACTERISTICS

(Typical Operating Circuit, $V_+ = 4.5V$ to $5.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Clock Period	t_{CP}		40			ns
CLK Pulse-Width High	t_{CH}		19			ns
CLK Pulse-Width Low	t_{CL}		19			ns
DIN Setup Time	t_{DS}		4			ns
DIN Hold Time	t_{DH}		8			ns
DOUT Propagation Delay	t_{DO}		12		32	ns
DOUT Rise and Fall Time	t_{DR}, t_{DF}	$C_{DOUT} = 10pF$, 20% to 80%			10	ns
LE Pulse-Width High	t_{LW}		20			ns
LE Setup Time	t_{LS}		10			ns
LE Rising to OUT_ Rising Delay	t_{LRR}	(Note 3)			100	ns
LE Rising to OUT_ Falling Delay	t_{LRF}	(Note 3)			300	ns
CLK Rising to OUT_ Rising Delay	t_{CRR}	(Note 3)			100	ns
CLK Rising to OUT_ Falling Delay	t_{CRF}	(Note 3)			310	ns
$\overline{OE}$ Rising to OUT_ Rising Delay	$t_{OE\overline{H}}$	(Note 3)			100	ns
$\overline{OE}$ Falling to OUT_ Falling Delay	$t_{OE\overline{L}}$	(Note 3)			320	ns
LED Output OUT_ Turn-On Fall Time	t_f	80% to 20%, pullup resistor = 65Ω			120	ns
LED Output OUT_ Turn-Off Rise Time	t_r	20% to 80%, pullup resistor = 65Ω			120	ns

Note 1: All parameters tested at $T_A = +25^\circ C$. Specifications over temperature are guaranteed by design.

Note 2: See Figure 3.

Note 3: A 65Ω pullup resistor connected from OUT_ to 5.5V.

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3.3V TIMING CHARACTERISTICS

(Typical Operating Circuit, $V_+ = 3V$ to $5.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Clock Period	t_{CP}		52			ns
CLK Pulse-Width High	t_{CH}		24			ns
CLK Pulse-Width Low	t_{CL}		24			ns
DIN Setup Time	t_{DS}		4			ns
DIN Hold Time	t_{DH}		8			ns
DOUT Propagation Delay	t_{DO}		12		50	ns
DOUT Rise and Fall Time	t_{DR}, t_{DF}	$C_{DOUT} = 10pF$, 20% to 80%			12	ns
LE Pulse-Width High	t_{LW}		20			ns
LE Setup Time	t_{LS}		15			ns
LE Rising to OUT_ Rising Delay	t_{LRR}	(Note 3)			120	ns
LE Rising to OUT_ Falling Delay	t_{LRF}	(Note 3)			310	ns
CLK Rising to OUT_ Rising Delay	t_{CRR}	(Note 3)			120	ns
CLK Rising to OUT_ Falling Delay	t_{CRF}	(Note 3)			330	ns
$\overline{OE}$ Rising to OUT_ Rising Delay	$t_{OE\uparrow}$	(Note 3)			120	ns
$\overline{OE}$ Falling to OUT_ Falling Delay	$t_{OE\downarrow}$	(Note 3)			330	ns
LED Output OUT_ Turn-On Fall Time	t_f	80% to 20% (Note 3)			120	ns
LED Output OUT_ Turn-Off Rise Time	t_r	20% to 80% (Note 3)			120	ns

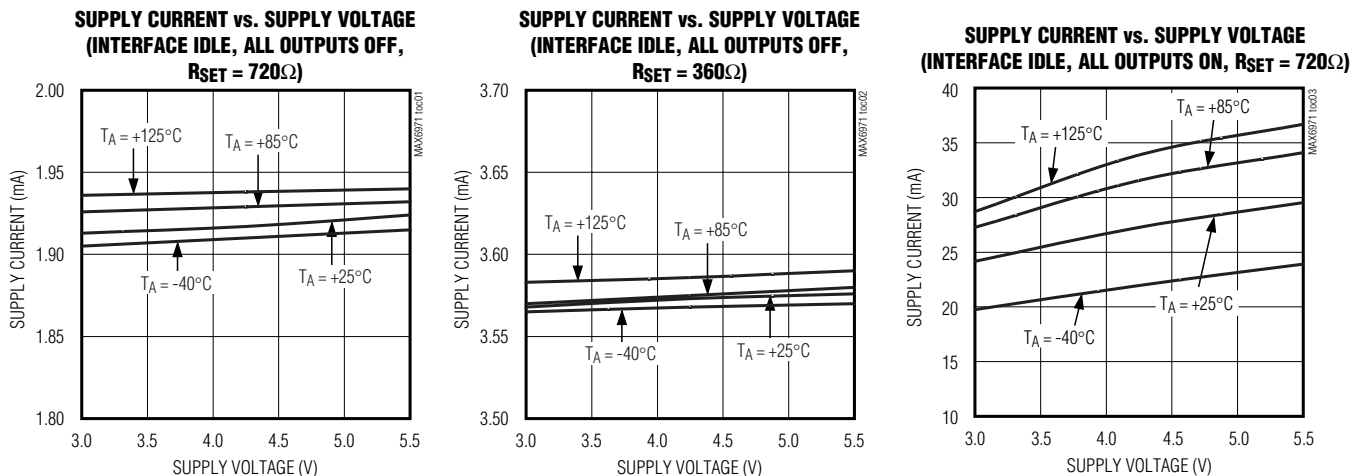
Note 1: All parameters tested at $T_A = +25^\circ\text{C}$. Specifications over temperature are guaranteed by design.

Note 2: See Figure 3.

Note 3: A 65Ω pullup resistor connected from OUT_ to $5.5V$.

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

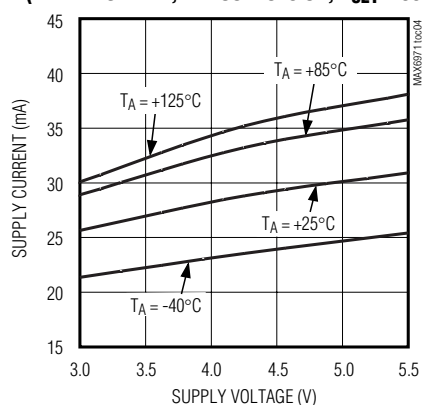


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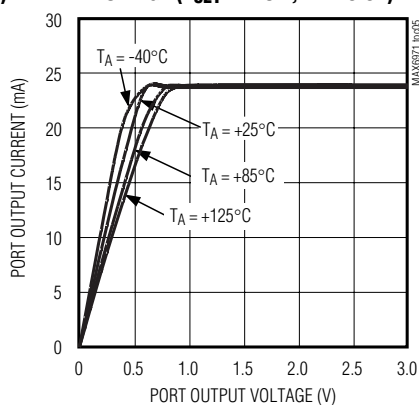
Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

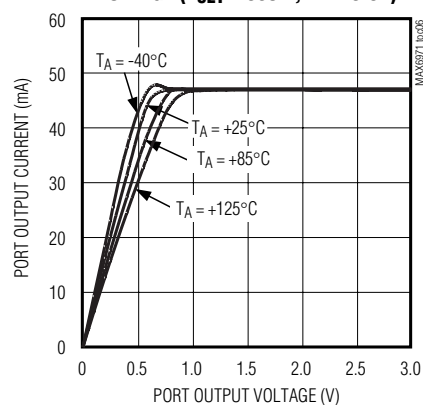
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(INTERFACE IDLE, ALL OUTPUTS ON, $R_{SET} = 360\Omega$)



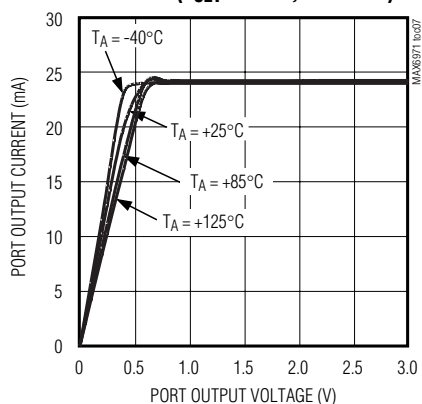
PORT OUTPUT CURRENT vs. PORT OUTPUT VOLTAGE ($R_{SET} = 720\Omega$, $V_+ = 3.3V$)



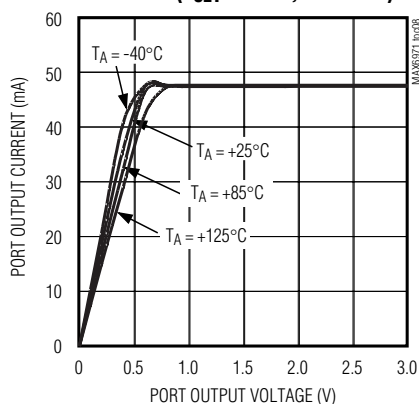
PORT OUTPUT CURRENT vs. PORT OUTPUT VOLTAGE ($R_{SET} = 360\Omega$, $V_+ = 3.3V$)



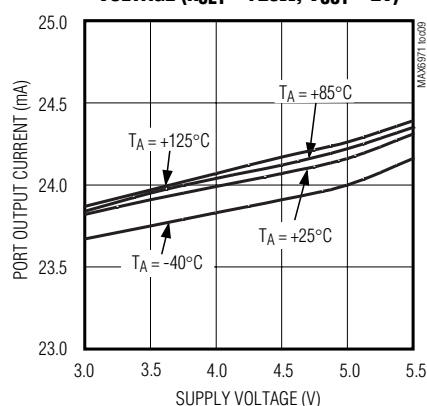
PORT OUTPUT CURRENT vs. PORT OUTPUT VOLTAGE ($R_{SET} = 720\Omega$, $V_+ = 5.0V$)



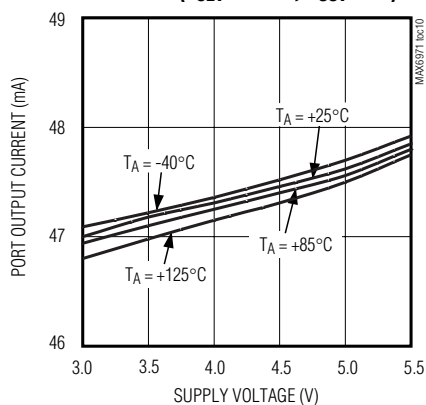
PORT OUTPUT CURRENT vs. PORT OUTPUT VOLTAGE ($R_{SET} = 360\Omega$, $V_+ = 5.0V$)



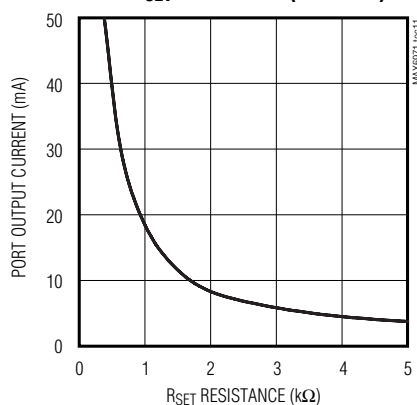
PORT OUTPUT CURRENT vs. SUPPLY VOLTAGE ($R_{SET} = 720\Omega$, $V_{OUT} = 2V$)



PORT OUTPUT CURRENT vs. SUPPLY VOLTAGE ($R_{SET} = 360\Omega$, $V_{OUT} = 2V$)



PORT OUTPUT CURRENT vs. R_{SET} RESISTANCE ($V_+ = 5.0V$)



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Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	DIN	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
3	CLK	Serial-Clock Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
4	LE	Load-Enable Input. Data is loaded transparently from the internal shift register(s) to the output latch(es) while LE is high. Data is latched into the output latch(es) on LE's falling edge, and retained while LE is low.
5–20	OUT0–OUT15	LED Driver Outputs. OUT0 to OUT15 are open-drain, constant-current-sinking outputs rated to 28V.
21	$\overline{OE}$	Output-Enable Input. High forces outputs OUT0 to OUT15 high impedance, without altering the contents of the output latches. Low enables outputs OUT0 to OUT15 to follow the state of the output latches.
22	DOUT	Serial-Data Output. Data is clocked out of the 16-bit internal shift register to DOUT on CLK's rising edge.
23	SET	LED Current Setting. Connect SET to GND through a resistor (R_{SET}) to set the maximum LED current.
24	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.1 μ F ceramic capacitor.

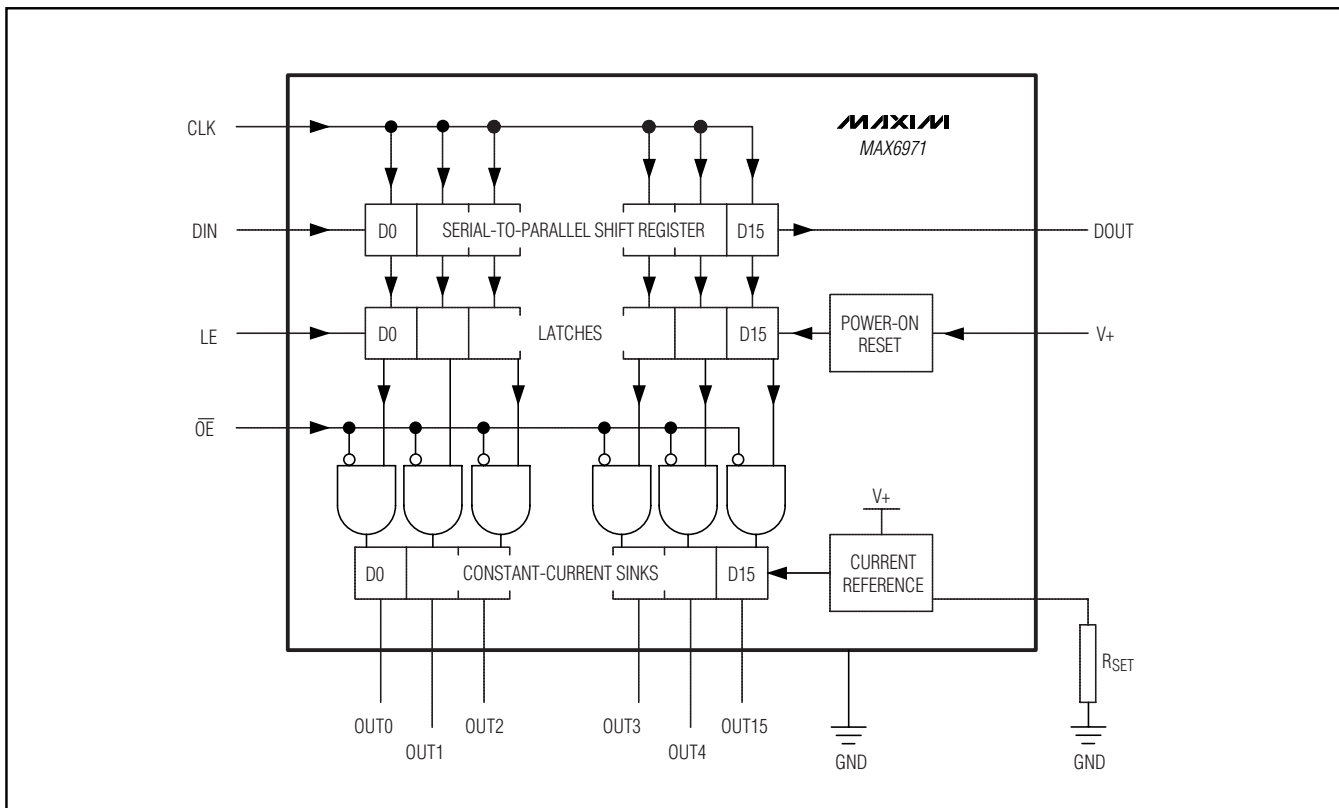


Figure 1. Block Diagram

16-Port, 36V Constant-Current LED Driver

Detailed Description

The MAX6971 LED driver comprises a 4-wire serial interface driving 16 constant-current-sinking, open-drain output ports. The outputs drive LEDs in either static or multiplex applications (Figure 1). The constant-current outputs are guaranteed for current accuracy not only with chip-supply voltage variations (5V $\pm$ 10% and 3V to 5.5V), but also over a realistic range of driver output voltage drop (0.8V to 2.5V). The drivers use current-sensing feedback circuitry (not simple current mirrors) to ensure very small current variations over the full allowed range of output voltage (see the *Typical Operating Characteristics*).

The 4-wire serial interface comprises a 16-bit shift register and a 16-bit transparent latch. The shift register is written through a clock input, CLK, and a data input, DIN, and the data propagates to a data output, DOUT. The data output allows multiple drivers to be cascaded and operated together. The contents of the 16-bit shift register are loaded into the transparent latch through a latch-enable input, LE. The latch is transparent to the shift register outputs when high, and latches the current state on the falling edge of LE.

Each driver output is an open-drain, constant-current sink that should be connected to the cathode of either a single LED or a series string of multiple LEDs. The LED anode can be connected to a supply voltage of up to 36V, independent of the MAX6971 supply, V_{+} . The constant-current capability is up to 55mA per output, set for all eight outputs by an external resistor, R_{SET} .

4-Wire Serial Interface

The serial interface on the MAX6971 is a 4-wire serial interface using four inputs (DIN, CLK, LE, $\overline{OE}$) and a data output (DOUT). This interface is used to write display data to the MAX6971. The serial-interface data word length is 16 bits, D0–D15. See Figure 2.

The functions of the five interface pins are as follows. DIN is the serial-data input, and must be stable when it is sampled on the rising edge of CLK. Data is shifted in, MSB first. This means that data bit D15 is clocked in first, followed by 15 more data bits finishing with the LSB, D0.

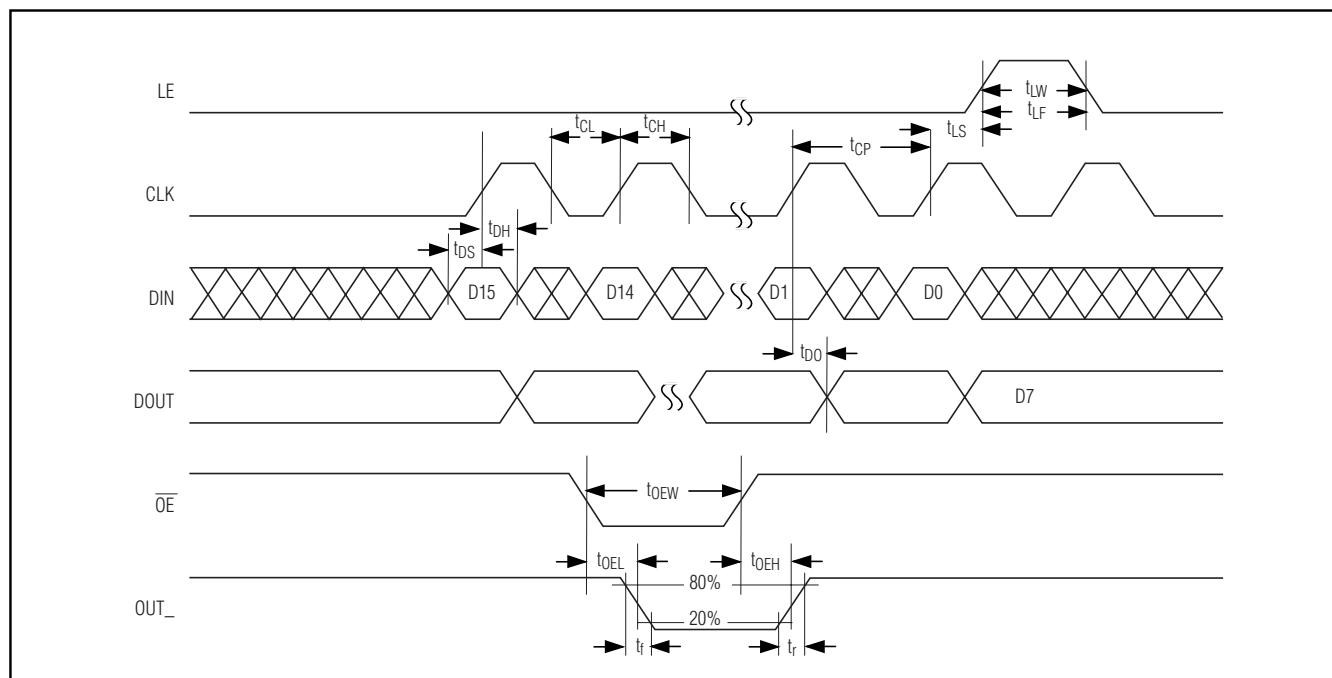


Figure 2. 4-Wire Serial-Interface Timing Diagram

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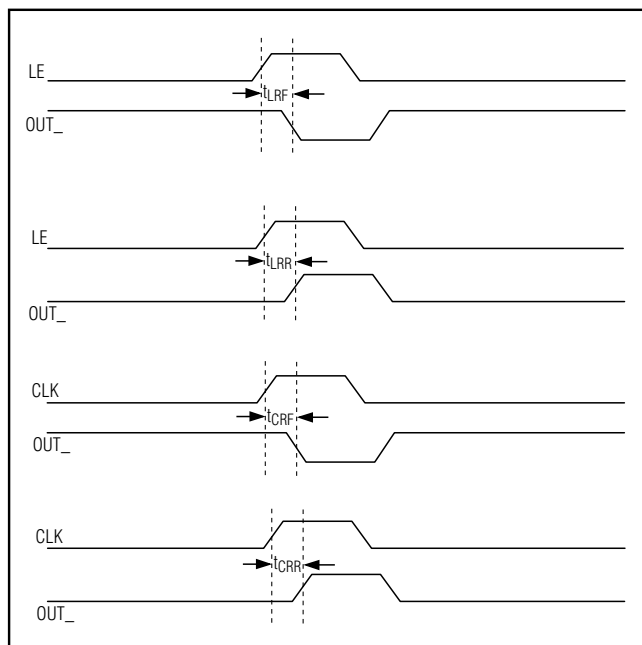


Figure 3. LE and CLK to OUT_ Timing

CLK is the serial-clock input, which shifts data at DIN into the MAX6971 16-bit shift register on its rising edge.

LE is the latch load input of the MAX6971 that transfers data from the MAX6971 16-bit shift register to its 16-bit latch when LE is high (transparent latch), and latches the data on the falling edge of LE (Figure 2).

The fourth input provides output-enable control of the output drivers. $\overline{OE}$ is high to force outputs OUT0–OUT15 high impedance, without altering the contents of the output latches, and low to enable outputs OUT0–OUT15 to follow the state of the output latches.

$\overline{OE}$ is independent of the operation of the serial interface. Data can be shifted into the serial-interface shift register and latched, regardless of the state of $\overline{OE}$.

DOUT is the serial-data output, which shifts data out from the MAX6971's 16-bit shift register on the rising edge of CLK. Data at DIN is propagated through the shift register and appears at DOUT 16 clock cycles later.

Table 1. 4-Wire Serial-Interface Truth Table

SERIAL DATA INPUT DIN	CLOCK INPUT CLK	SHIFT-REGISTER CONTENTS						LOAD INPUT LE	LATCH CONTENTS						BLANKING INPUT $\overline{OE}$	OUTPUT CONTENTS					
		D ₀	D ₁	D ₂	...	D _{n-1}	D _n		D ₀	D ₁	D ₂	...	D _{n-1}	D _n		D ₀	D ₁	D ₂	...	D _{n-1}	D _n
H		H	R ₁	R ₂	...	R _{n-2}	R _{n-1}	—	—	—	—	—	—	—	—	—	—	—	—	—	—
L		L	R ₁	R ₂	...	R _{n-2}	R _{n-1}	—	—	—	—	—	—	—	—	—	—	—	—	—	—
X		R ₀	R ₁	R ₂	...	R _{n-1}	R _n	—	—	—	—	—	—	—	—	—	—	—	—	—	—
—	—	X	X	X	...	X	X	H	R ₀	R ₁	R ₂	...	R _{n-1}	R _n	—	—	—	—	—	—	—
—	—	P ₁	P ₂	P ₃	...	P _{n-1}	P _n	L	P ₀	P ₁	P ₂	...	P _{n-1}	P _n	L	$\overline{P_0}$	$\overline{P_1}$	$\overline{P_2}$	...	$\overline{P_{n-1}}$	$\overline{P_n}$
—	—	—	—	—	...	—	—	—	X	X	X	...	X	X	H	Hi-Z	Hi-Z	Hi-Z	...	Hi-Z	Hi-Z

L = Low-logic level.

H = High-logic level.

X = Don't care.

P = Present state.

R = Previous state.

Hi-Z = High impedance.

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Applications Information

Selecting External Component R_{SET} to Set LED Output Current

The MAX6971 uses an external resistor, R_{SET} , to set the LED current for outputs OUT0–OUT15. The minimum allowed value of R_{SET} is 327.3Ω , which sets the output currents to 55mA. The maximum allowed value of R_{SET} is $5k\Omega$. The reference value, 360Ω , sets the output currents to 50mA. To set a different output current, use the formula:

$$R_{SET} = 18,000 / I_{OUT}$$

where I_{OUT} is the desired output current in mA.

Computing Power Dissipation

The upper limit for power dissipation (P_D) for the MAX6971 is determined by the following equation:

$$P_D = (V_+ \times I_+) + (V_{OUT} \times DUTY \times I_{OUT} \times N)$$

where:

V_+ = supply voltage

I_+ = operating supply current when sinking I_{OUT} LED drive current into N outputs

DUTY = PWM duty cycle applied to $\overline{OE}$

N = number of MAX6971 outputs driving LEDs at the same time (maximum is 16)

V_{OUT} = MAX6971 port output voltage when driving load LED(s)

I_{OUT} = LED drive current programmed by R_{SET}

P_D = power dissipation, in mW if currents are in mA

Dissipation example:

$$I_{OUT} = 20\text{mA}, N = 16, DUTY = 1, V_{OUT} = 2\text{V}, V_+ = 5.25\text{V}$$

$$P_D = (5.25\text{V} \times 25\text{mA}) + (2\text{V} \times 1 \times 20\text{mA} \times 16) = 0.77\text{W}$$

Thus, for a 24-pin TSSOP package ($T_{JA} = 1 / 0.0122 = +82^\circ\text{C/W}$ from the *Absolute Maximum Ratings*), the maximum allowed ambient temperature T_A is given by:

$$T_{J(\text{MAX})} = T_A + (P_D \times T_{JA}) = +150^\circ\text{C} = T_A + (0.77 \times 82^\circ\text{C/W})$$

so $T_A = +86^\circ\text{C}$.

Overtemperature Cutoff

The MAX6971 contains an internal temperature sensor that turns off all outputs when the die temperature exceeds approximately $+165^\circ\text{C}$. The outputs are enabled again when the die temperature drops below approximately $+140^\circ\text{C}$. Register contents are not affected, so when a driver is overdissipating, the external symptom is the load LEDs cycling between on and off as the driver repeatedly overheats and cools, alternately turning the LEDs off and then back on again.

Power-Supply Considerations

The MAX6971 operates with a chip supply V_+ , and one or more LED supplies. Bypass each supply to GND with a $0.1\mu\text{F}$ capacitor as close to the MAX6971 as possible. This is normally adequate for static LED driving. For multiplex or PWM applications, it is necessary to add an additional bulk electrolytic capacitor of $4.7\mu\text{F}$ or more to each supply for every 4 to 16 MAX6971s. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-interface speed. Inadequate V_+ decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.

Chip Information

PROCESS: BiCMOS

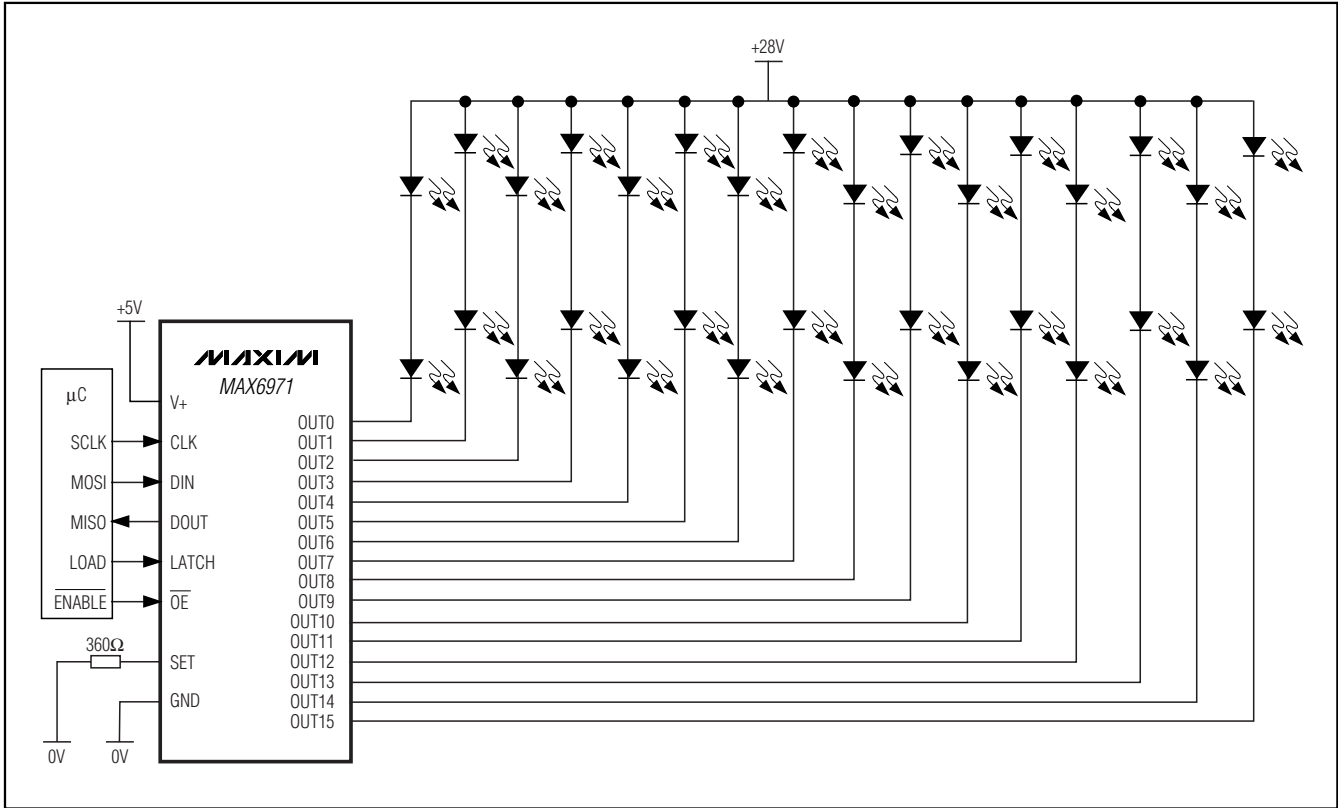
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Selector Guide

PART	NUMBER OF OUTPUTS	MAX OUTPUT VOLTAGE (V)	MAX OUTPUT CURRENT (mA)	LED FAULT DETECTION	WATCHDOG	
MAX6968	8	5.5	55	—	—	
MAX6977				Yes	—	
MAX6978				Yes	Yes	
MAX6970*	8	36		—	—	
MAX6981*				Yes	—	
MAX6980*				Yes	Yes	
MAX6969	16	5.5		—	—	
MAX6979				Yes	Yes	
MAX6971	16	36		—	—	
MAX6983				Yes	Yes	

*Future product—contact factory for availability.

Typical Application Circuit

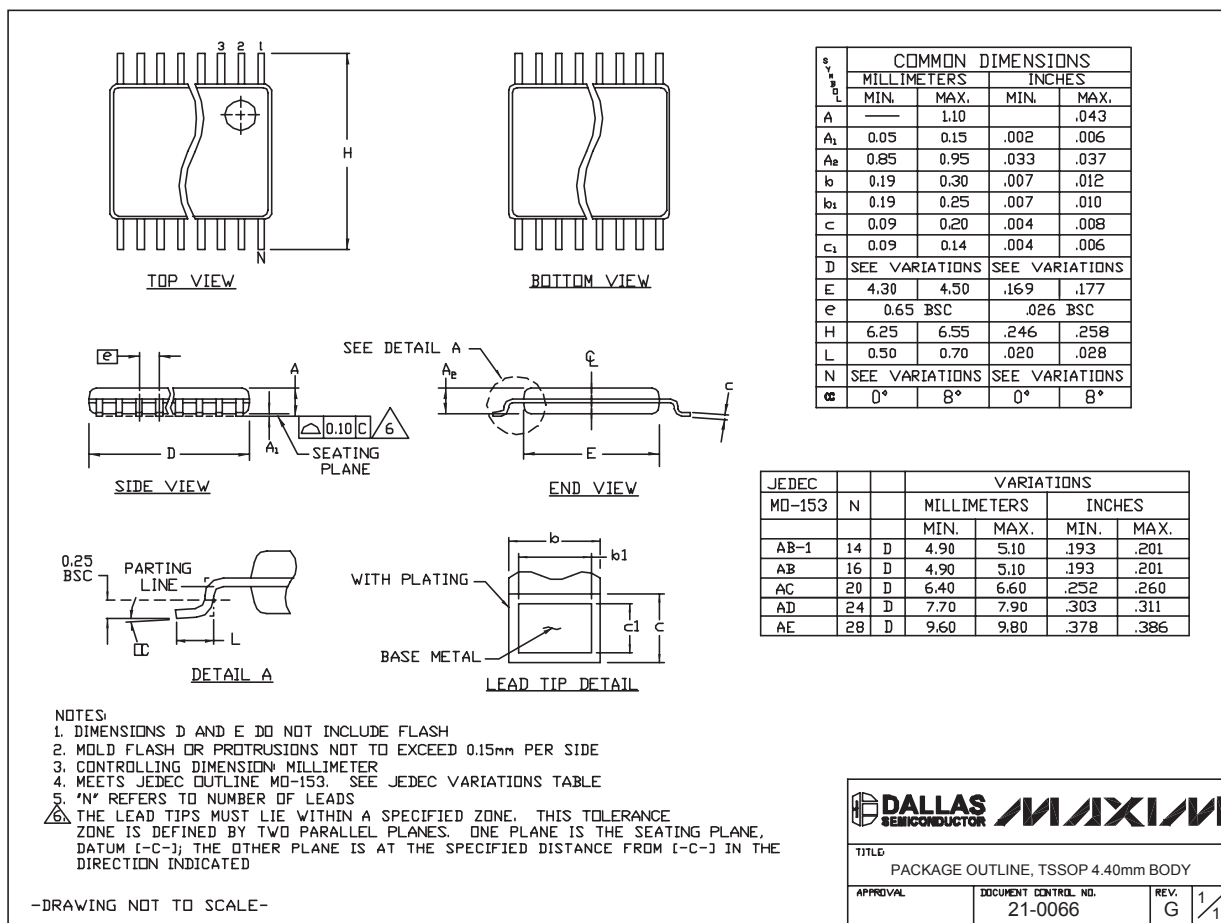


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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX6971

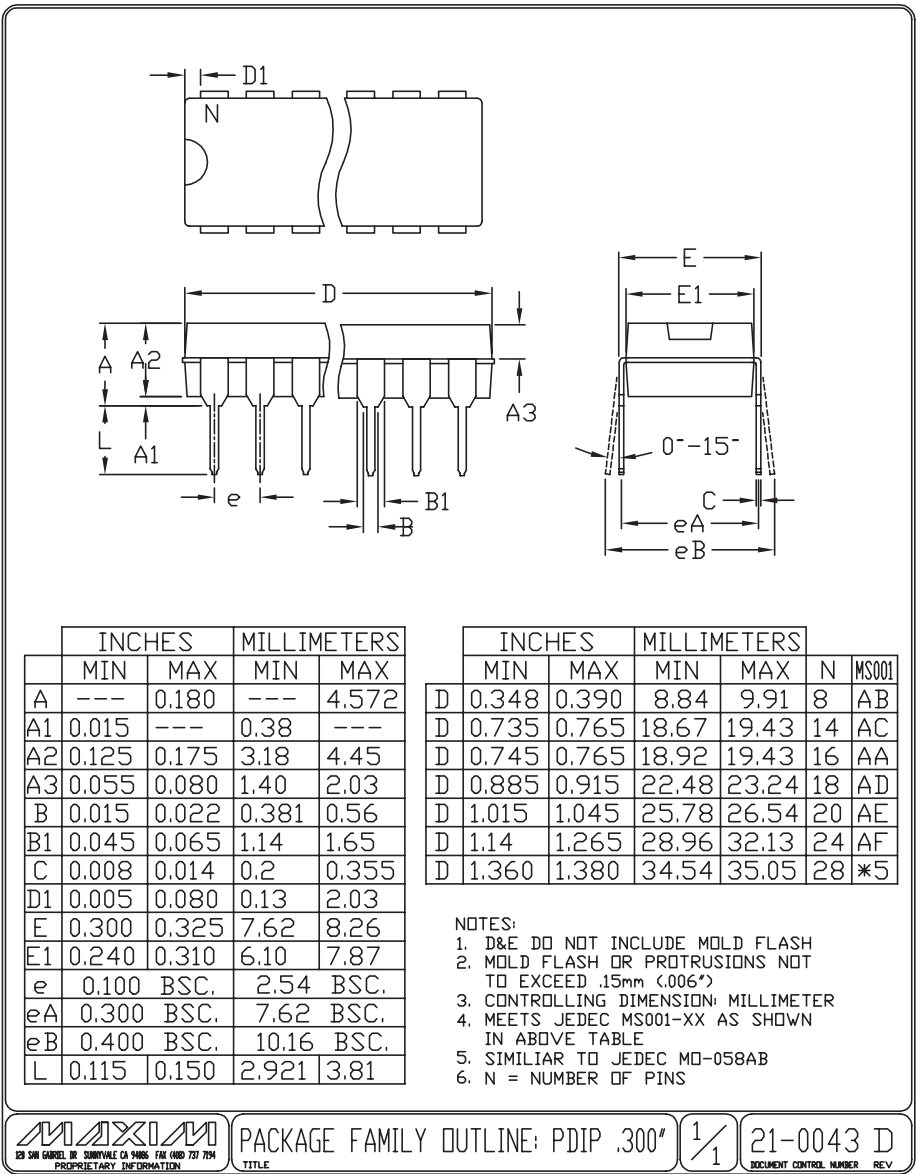


TSSOP4.40mm.EPS

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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



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