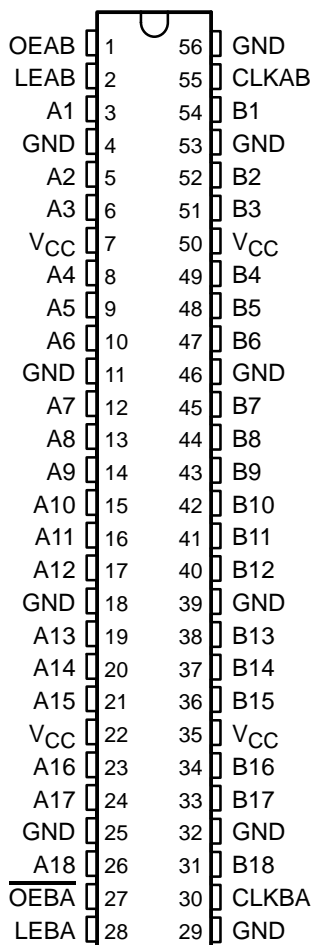


SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700E – JULY 1997 – REVISED NOVEMBER 2002

- **Members of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH16501 . . . WD PACKAGE
SN74LVTH16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'LVTH16501 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH16501DL	LVTH16501
		Tape and reel	SN74LVTH16501DLR	
–55°C to 125°C	TSSOP – DGG	Tape and reel	SN74LVTH16501DGGR	LVTH16501
	CFP – WD	Tube	SNJ54LVTH16501WD	SNJ54LVTH16501WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH16501, SN74LVTH16501

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB . When $\overline{\text{OEAB}}$ is high, the outputs are active. When $\overline{\text{OEAB}}$ is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA , and CLKBA . The output enables are complementary ($\overline{\text{OEAB}}$ is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0^\ddagger
H	L	L	X	B_0^\S

† A-to-B data flow is shown; B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA , and CLKBA .

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

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The diagram illustrates the logic for a 17-channel receiver. On the left, eight input signals are listed: OEAB (1), CLKAB (55), LEAB (2), LEBA (28), CLKBA (30), OEBA (27), A1 (3), and B1 (54). The OEAB, CLKAB, LEAB, and LEBA signals each pass through an inverter. The OEBA signal passes through an inverter and then a buffer. The A1 signal passes through a buffer. The B1 signal passes through a buffer. The outputs of these buffers are connected to two 1D C1 blocks. The first 1D C1 block has inputs 1D, C1, and CLK. The second 1D C1 block has inputs 1D, C1, and CLK. The outputs of these blocks are connected to a common bus labeled 'To 17 Other Channels'.

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16501	96 mA
SN74LVTH16501	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16501	48 mA
SN74LVTH16501	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

SN54LVTH16501, SN74LVTH16501

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recommended operating conditions (see Note 4)

			SN54LVTH16501		SN74LVTH16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μ s/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN54LVTH16501, SN74LVTH16501

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16501		SN74LVTH16501		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2		−1.2		V		
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2		V _{CC} −0.2		V		
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4		2.4				
		V _{CC} = 3 V		I _{OH} = −24 mA		2				
				I _{OH} = −32 mA					2	
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2		0.2	V	
				I _{OL} = 24 mA		0.5		0.5		
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4		0.4		
				I _{OL} = 32 mA		0.5		0.5		
				I _{OL} = 48 mA		0.55				
				I _{OL} = 64 mA				0.55		
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1		μA		
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10		10				
	A or B ports‡	V _{CC} = 3.6 V, V _I = 5.5 V		20		20				
		V _{CC} = 3.6 V, V _I = V _{CC}		1		1				
		V _{CC} = 3.6 V, V _I = 0		−5		−5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA		
I _I (hold)	A or B ports	V _{CC} = 3 V, V _I = 0.8 V		75		75		μA		
		V _{CC} = 3 V, V _I = 2 V		−75		−75				
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V				±500				
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		μA		
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		μA		
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.19		0.19	mA	
				Outputs low		5		5		
				Outputs disabled		0.19		0.19		
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA		
C _i		V _I = 3 V or 0		4		4		pF		
C _{io}		V _O = 3 V or 0		10		10		pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.



SN54LVTH16501, SN74LVTH16501

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVTH16501				SN74LVTH16501				UNIT	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency			150		150		150		150		MHz	
t_w	Pulse duration	LE high		3.3		3.3		3.3		3.3		ns	
		CLK high or low		3.3		3.3		3.3		3.3			
t_{su}	Setup time	A before CLKAB↑		2.5		2.8		2.1		2.4		ns	
		B before CLKBA↑		2.5		2.8		2.1		2.4			
		A or B before LE↓	CLK high		3.4		2.8		2.4		1.6		
			CLK low		2.2		1.3		1.4		0.5		
t_h	Hold time	A or B after CLK↑		2.2		1.5		1		0		ns	
		A or B after LE↓		2.1		1.9		1.7		1.7			

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

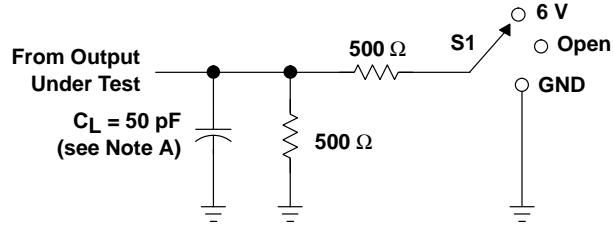
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16501				SN74LVTH16501				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150			150		MHz
t _{PLH}	B or A	A or B	1.2	4.3	4.7		1.3	2.7	3.7	4		ns
t _{PHL}			1.2	4.3	4.6		1.3	2.4	3.7	4		
t _{PLH}	LEBA or LEAB	A or B	1.4	6.2	6.6		1.5	3.4	5.1	5.7		ns
t _{PHL}			1.4	5.9	6.5		1.5	3.5	5.1	5.7		
t _{PLH}	CLKBA or CLKAB	A or B	1.2	6	6.7		1.3	3.5	5.1	5.7		ns
t _{PHL}			1.2	5.9	6.6		1.3	3.4	5.1	5.7		
t _{PZH}	OEBA or OEAB	A or B	1.2	5.5	5.9		1.3	3.4	4.8	5.5		ns
t _{PZL}			1.2	5.5	5.9		1.3	3.4	4.8	5.5		
t _{PHZ}	OEBA or OEAB	A or B	1.6	6.3	6.7		1.7	4.2	5.8	6.3		ns
t _{PLZ}			1.6	6.1	6.6		1.7	3.8	5.8	6.3		

\dagger All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

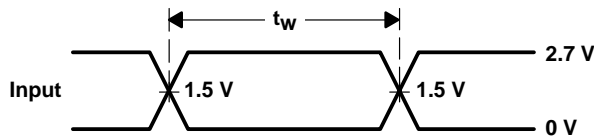
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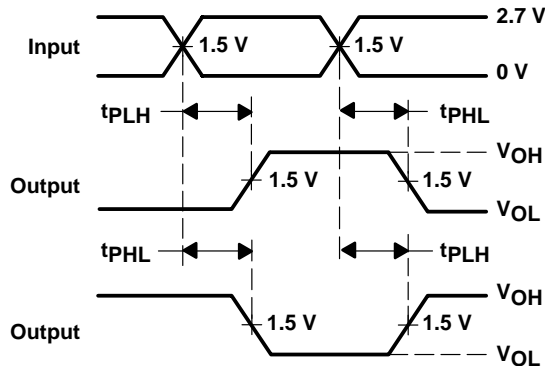
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

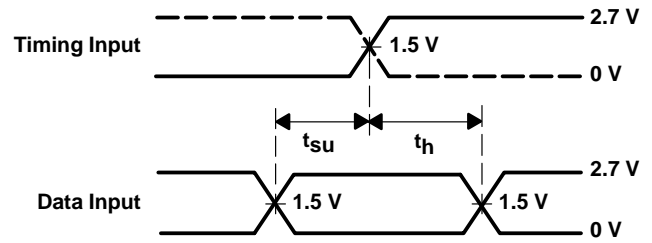


VOLTAGE WAVEFORMS
PULSE DURATION

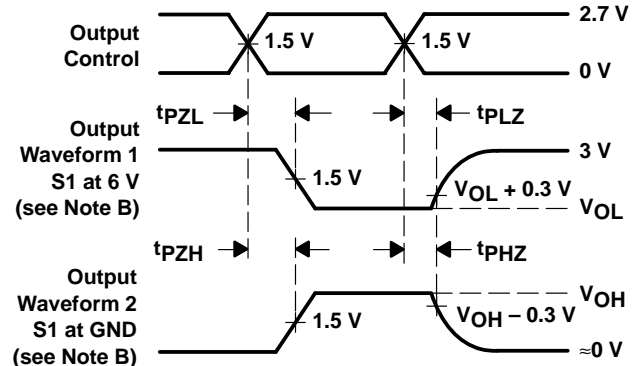


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9677701QXA	ACTIVE	CFP	WD	56	1	TBD	Call TI	Level-NC-NC-NC
74LVTH16501DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
74LVTH16501DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH16501DGGR	ACTIVE	TSSOP	DGG	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVTH16501DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH16501DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LVTH16501WD	ACTIVE	CFP	WD	56	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

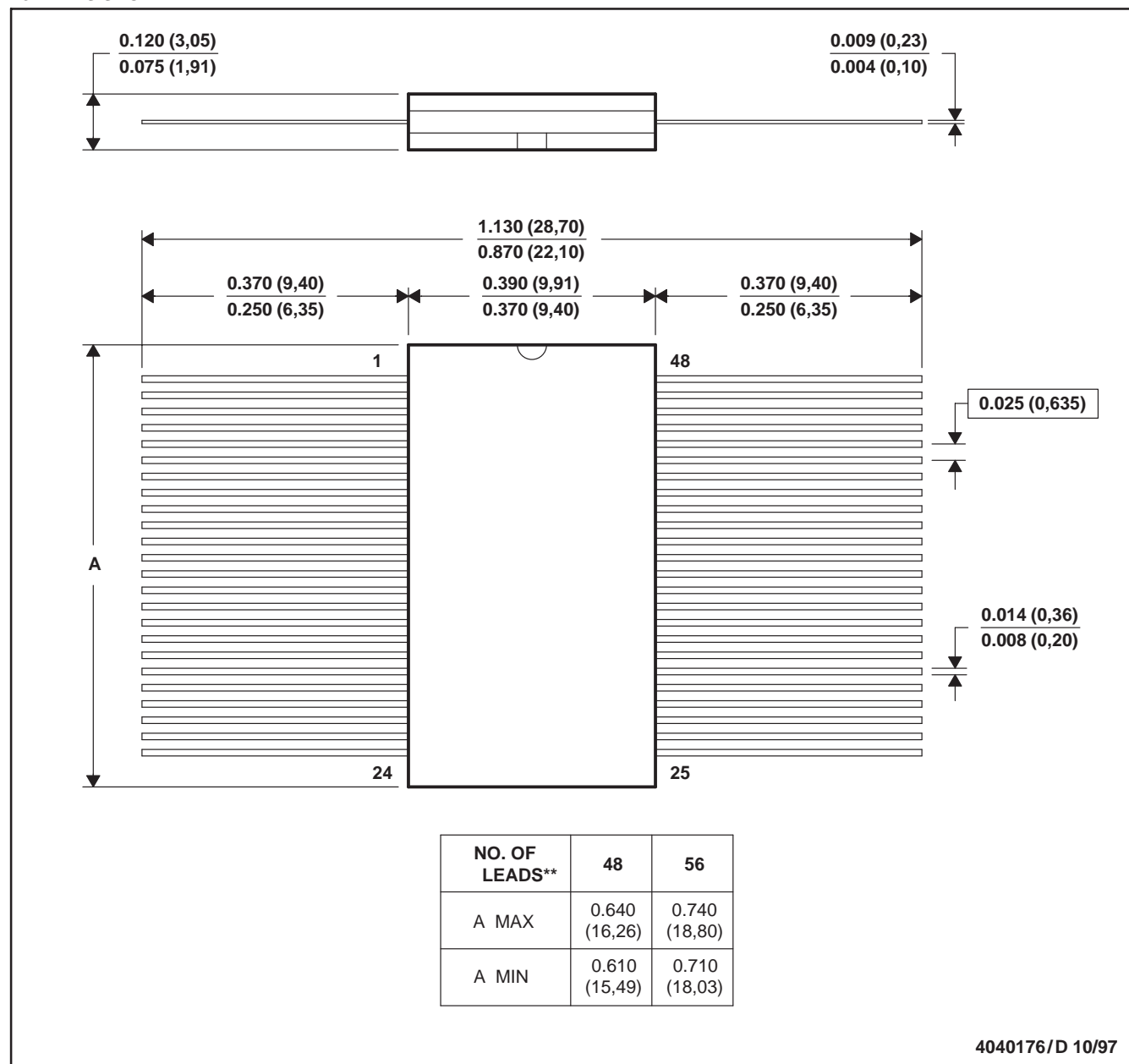
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WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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