

Optimized Multi-Phase PWM Controller with 6-Bit DAC for VR10.X Application

The ISL6556A controls microprocessor core voltage regulation by driving up to 4 synchronous-rectified buck channels in parallel. Multi-phase buck converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area.

The ISL6556A utilizes $r_{DS(ON)}$ current sensing in each phase for adaptive voltage positioning (droop), channel-current balancing, and overcurrent protection. To ensure droop accuracy, an external NTC compensation circuit can be used to completely nullify the effect of temperature related variation in $r_{DS(ON)}$.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds can be eliminated using the remote-sense amplifier. The precision threshold-sensitive enable input is available to accurately coordinate the start up of the ISL6556A with Intersil MOSFET driver IC. Dynamic-VID™ technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting. The ISL6556A uses 5V bias and has a built-in shunt regulator to allow 12V bias using only a small external limiting resistor.

Ordering Information

PART NUMBER*	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6556ACB	0 to 70	28 Ld SOIC	M28.3
ISL6556ACBZ (Note)	0 to 70	28 Ld SOIC (Pb-free)	M28.3
ISL6556ACR	0 to 70	32 Ld 5x5B QFN	L32.5x5B
ISL6556ACRZ (Note)	0 to 70	32 Ld 5x5B QFN (Pb-free)	L32.5x5B

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

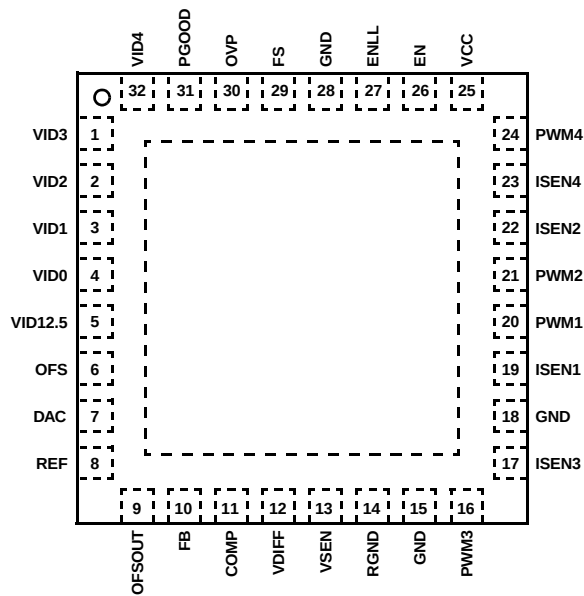
*Add "-T" suffix for tape and reel.

Features

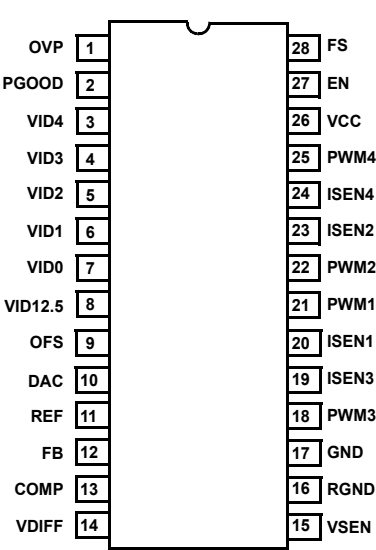
- Precision Multi-Phase Core Voltage Regulation
 - Differential Remote Voltage Sensing
 - $\pm 0.5\%$ System Accuracy Over Temperature and Life
 - Adjustable Reference-Voltage Offset
- Precision $r_{DS(ON)}$ Current Sensing
 - Accurate Load-Line Programming
 - Accurate Channel-Current Balancing
 - Low-Cost, Lossless Current Sensing
- Internal Shunt Regulator for 5V or 12V Biasing
- Microprocessor Voltage Identification Input
 - Dynamic VID™ Technology
 - 6-Bit VID Input
 - 0.8375V to 1.600V in 12.5mV Steps
- Threshold Enable Function for Precision Sequencing
- Overcurrent Protection
- Overvoltage Protection
 - No Additional External Components Needed
 - OVP Pin to drive optional Crowbar Device
- 2, 3, or 4 Phase Operation up to 1.5MHz per Phase
- QFN Package Option
 - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
 - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-free Available (RoHS Compliant)

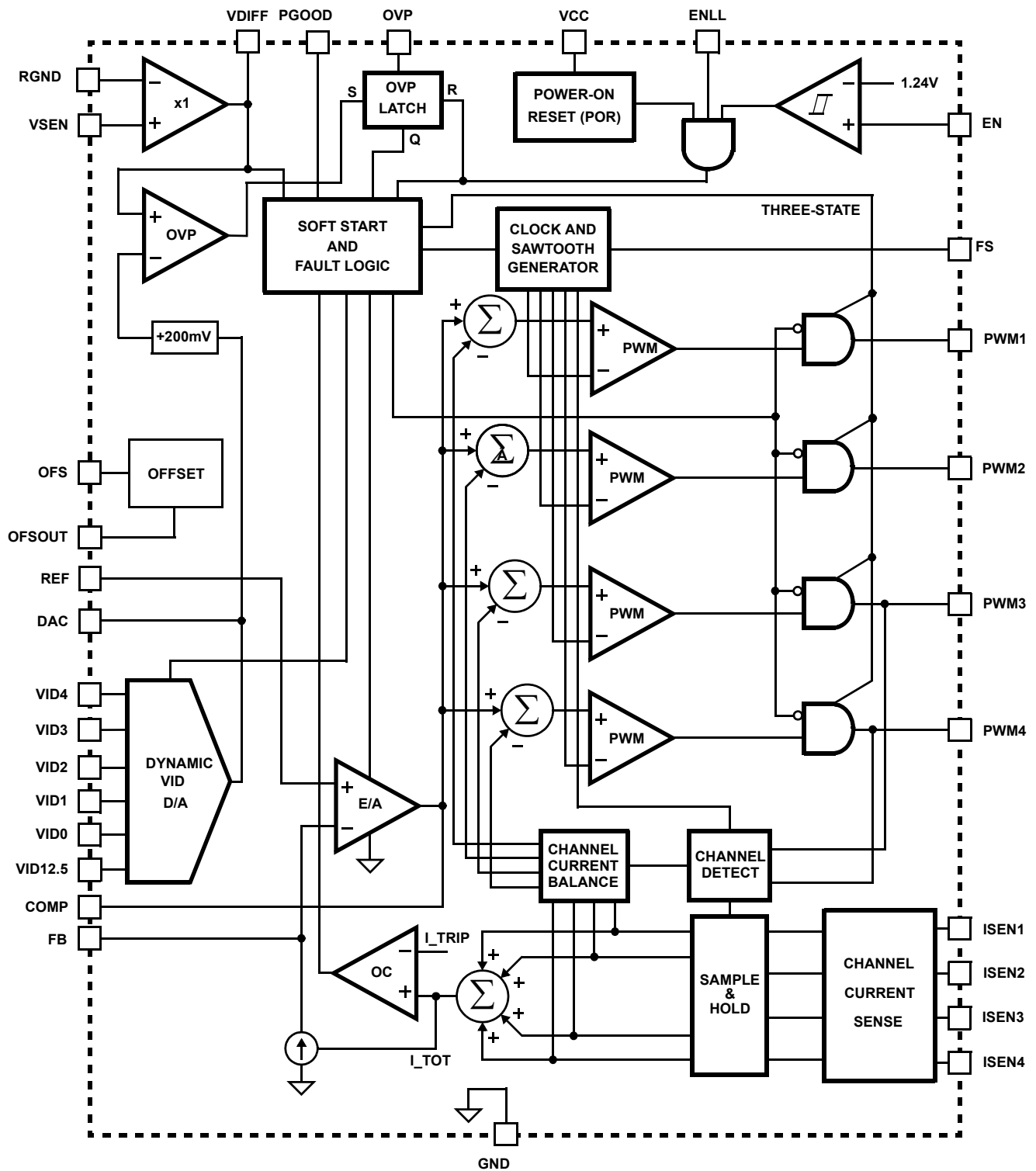
Pinouts

32 LEAD QFN
TOP VIEW

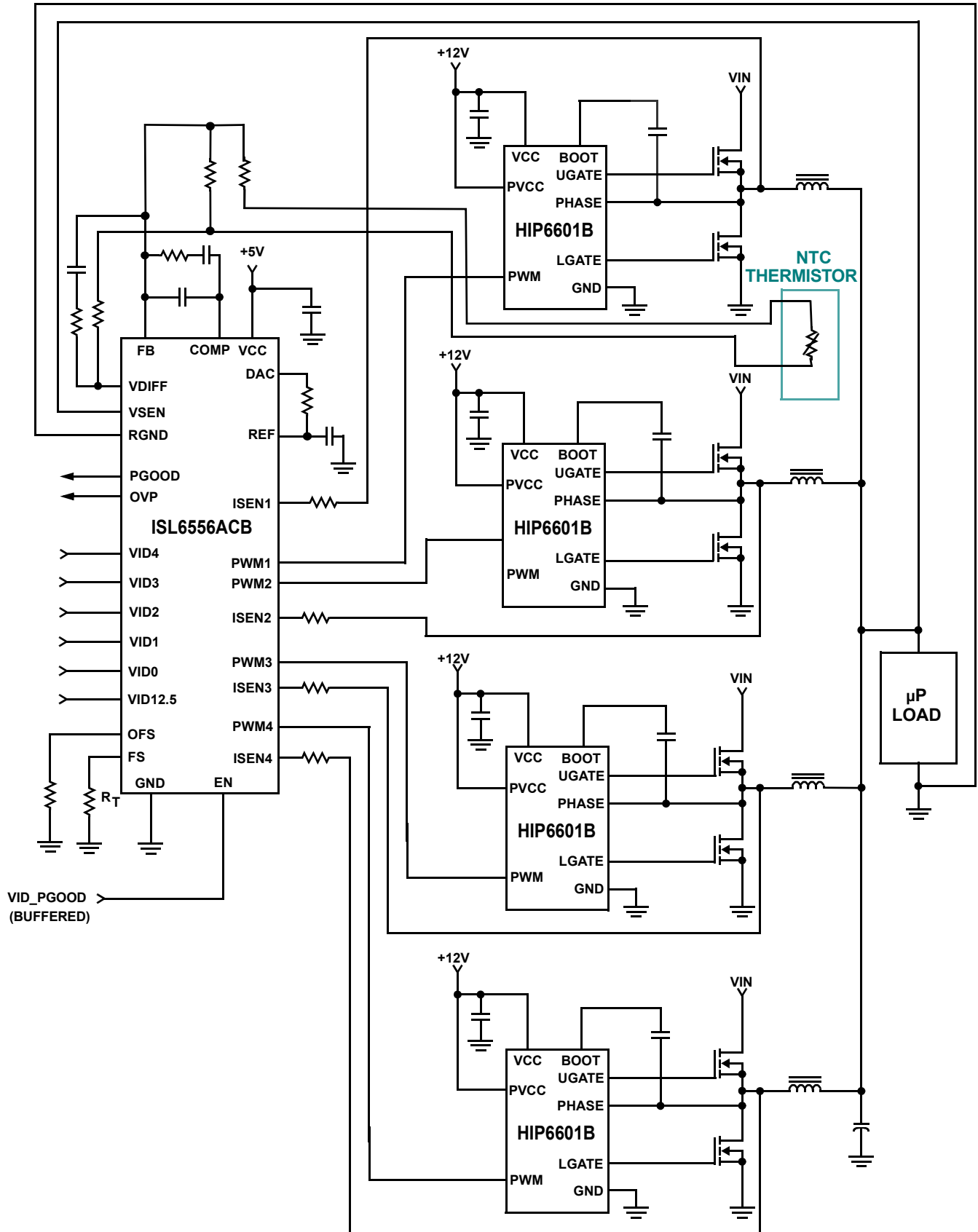


28 LEAD SOIC
TOP VIEW

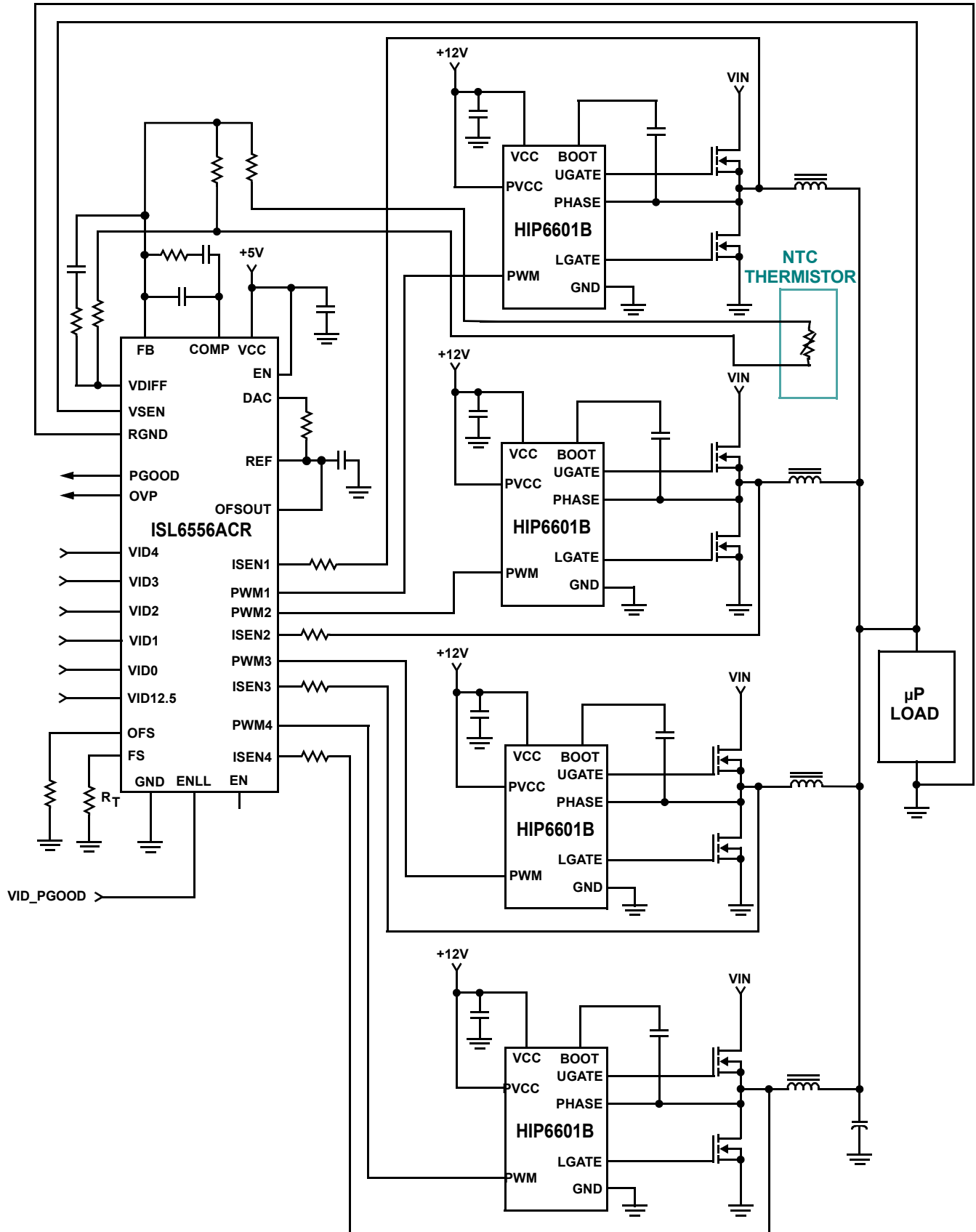


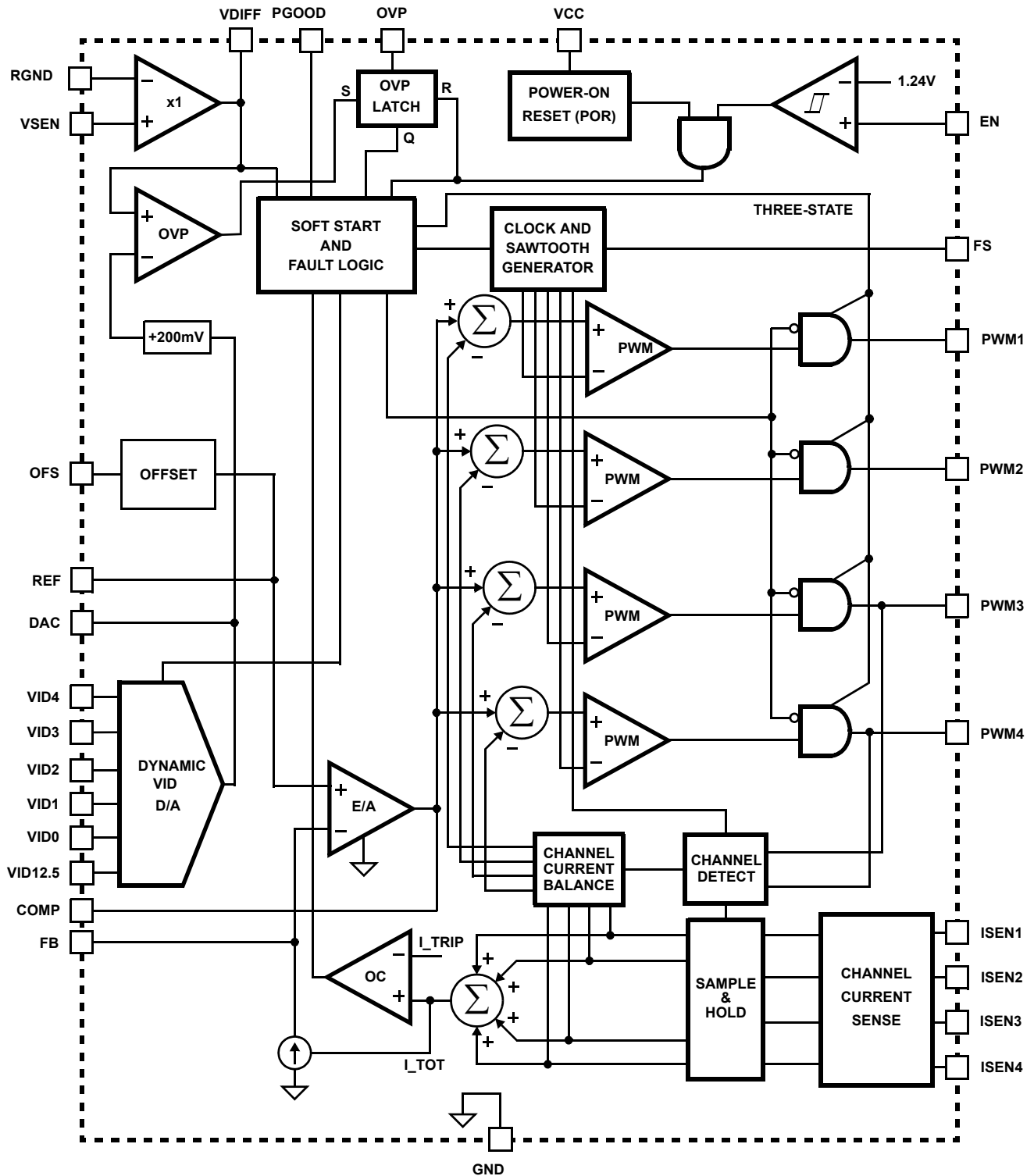
ISL6556ACR Block Diagram

Typical Application of ISL6556ACB



Typical Application of ISL6556ACR



ISL6556ACB Block Diagram

Absolute Maximum Ratings

Supply Voltage, VCC	+7V
Input, Output, or I/O Voltage (except OVP)	GND -0.3V to V _{CC} +0.3V
OVP Voltage	+15V
ESD (Human body model)	>4kV
ESD (Machine model)	>300V
ESD (Charged device model)	>2kV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	60	N/A
QFN Package (Notes 2, 3)	32	3.5
Maximum Junction Temperature	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)	

Operating Conditions

Supply Voltage, VCC (5V bias mode, Note 4)	+5V ±5%
Junction Temperature	0°C to 125°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V or ICC < 25mA (Note 4), T_J = 0°C to 105°C.
Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN = 5VDC; R _T = 100k Ω , ISEN1 = ISEN2 = ISEN3 = ISEN4 = -70 μ A	-	14	18	mA
Shutdown Supply	VCC = 5VDC; EN = 0VDC; R _T = 100k Ω	-	10	14	mA
SHUNT REGULATOR					
VCC Voltage	VCC tied to 12VDC through 300 Ω resistor, R _T = 100k Ω	5.6	5.9	6.2	V
VCC Sink Current	VCC tied to 12VDC through 300 Ω resistor, R _T = 100k Ω	-	-	25	mA
POWER-ON RESET AND ENABLE					
POR Threshold	VCC Rising	4.2	4.31	4.50	V
	VCC Falling	3.7	3.82	4.00	V
ENABLE Threshold	EN Rising	1.22	1.24	1.26	V
	Hysteresis	-	100	-	mV
	Fault Reset	1.10	1.14	1.18	V
ENLL Input Logic Low Level		-	-	0.4	V
ENLL input Logic High Level		0.8	-	-	V
ENLL Leakage Current	ENLL = 5V	-	-	1	μ A
REFERENCE VOLTAGE AND DAC					
System Accuracy (VID = 1.2V - 1.6V)	(Note 5)	-0.5	-	0.5	%VID
System Accuracy (VID = 0.8375V - 1.1875V)	(Note 5)	-0.8	-	0.8	%VID
VID Pull Up		-65	-50	-35	μ A
VID Input Low Level		-	-	0.4	V
VID Input High Level		0.8	-	-	V
DAC Source/Sink Current	VID = 010100	-200	-	200	μ A
OFSOUT Source/Sink Current	(ISL6556ACR Only)	-50	-	50	μ A
REF Source/Sink Current		-50	-	50	μ A

Electrical Specifications Operating Conditions: VCC = 5V or ICC < 25mA (Note 4), T_J = 0°C to 105°C.
Unless Otherwise Specified. (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PIN-ADJUSTABLE OFFSET					
Voltage at OFS pin	Offset resistor connected to ground	485	500	515	mV
	VCC=5.00V, offset resistor connected to VCC	2.91	3.00	3.09	V
OSCILLATOR					
Accuracy	R _T = 100kΩ	-10	-	10	%
Adjustment Range		0.08	-	1.5	MHz
Sawtooth Amplitude		-	1.5	-	V
Max Duty Cycle		-	66.7	-	%
ERROR AMPLIFIER					
Open-Loop Gain	R _L = 10kΩ to ground	-	80	-	dB
Open-Loop Bandwidth	C _L = 100pF, R _L = 10kΩ to ground	-	18	-	MHz
Slew Rate	C _L = 100pF	4.5	6.0	7.5	V/μs
Maximum Output Voltage		4.0	4.3	-	V
Output High Voltage @ 2mA		3.7	-	-	V
Output Low Voltage @ 2mA		-	-	1.35	V
REMOTE-SENSE AMPLIFIER					
Bandwidth		-	20	-	MHz
Output High Current	VSEN - RGND = 2.5V	-500	-	500	μA
Output High Current	VSEN - RGND = 0.6	-500	-	500	μA
PWM OUTPUT					
PWM Output Voltage LOW Threshold	I _{load} = ±500μA	-	-	0.3	V
PWM Output Voltage HIGH Threshold	I _{load} = ±500μA	4.3	-	-	V
SENSE CURRENT					
Sensed Current Tolerance	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 80μA, 0°C to 105°C	74	81	91	μA
Overcurrent Trip Level		98	110	122	μA
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I _{PGOOD} = 4mA	-	-	0.4	V
Undervoltage Offset From VID	VSEN Falling	72	74	76	%VID
Overvoltage Threshold	Voltage above VID, After Soft Start (Note 6)	180	200	220	mV
	Before Enable	-	1.63	-	V
	VCC < POR Threshold	1.7	1.8	1.87	V
Overvoltage Reset Voltage	VCC ≥ POR Threshold, VSEN Falling	-	0.6	-	V
	VCC < POR Threshold	-	1.5	-	V
OVP Drive Voltage	I _{OVP} = -100mA, VCC = 5V	-	1.9	-	V
Minimum VCC for OVP		1.4	-	-	V

NOTES:

- When using the internal shunt regulator, VCC is clamped to 6.02V (max). Current must be limited to 25mA or less.
- These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
- During soft start, VDAC rises from 0 to VID. The overvoltage trip level is the higher of 1.7V and VDAC + 0.2V.

Functional Pin Description

VCC

Supplies all the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply or through a series 300Ω resistor to a +12V supply.

GND

Bias and reference ground for the IC.

EN

This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN is driven above 1.24V, the ISL6556A is active depending on status of ENLL, the internal POR, and pending fault states. Driving EN below 1.14V will clear all fault states and prime the ISL6556 to soft start when re-enabled.

ENLL

This pin is implemented in QFN ISL6556A only. It's a logic-level enable input for the controller. When asserted to a logic high, the ISL6556A is active depending on status of EN, the internal POR, VID inputs and pending fault states. Deasserting ENLL will clear all fault states and prime the ISL6556A to soft start when re-enabled.

FS

A resistor, placed from FS to ground will set the switching frequency. There is an inverse relationship between the value of the resistor and the switching frequency. See Figure 13 and Equation 26.

VID4, VID3, VID2, VID1, VID0, and VID12.5

These are the inputs to the internal DAC that provides the reference voltage for output regulation. Connect these pins either to open-drain outputs with or without external pull-up resistors or to active-pull-up outputs. VID4-VID12.5 have 50μA internal pull-up current sources that diminish to zero as the voltage rises above the logic-high level. These inputs can be pulled up as high as VCC plus 0.3V.

VDIFF, VSEN, and RGND

VSEN and RGND form the precision differential remote-sense amplifier. This amplifier converts the differential voltage of the remote output to a single-ended voltage referenced to local ground. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and RGND to the sense pins of the remote load.

FB and COMP

Inverting input and output of the error amplifier respectively. FB is connected to VDIFF through a resistor. A negative current, proportional to output current is present on the FB pin. A properly sized resistor between VDIFF and FB sets the load line (droop). The droop scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(ON)}$. COMP is tied back to FB through an external R-C network to compensate the regulator.

DAC and REF

The DAC output pin is the output of the precision internal DAC reference. The REF input pin is the positive input of the error amplifier. In typical applications, a 1kΩ, 1% resistor is used between DAC and REF to generate a precise offset voltage. This voltage is proportional to the offset current determined by the offset resistor from OFS to ground or VCC. A capacitor is used between REF and ground to smooth the voltage transition during Dynamic VID™ operations.

PWM1, PWM2, PWM3, PWM4

Pulse-width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver IC. The number of active channels is determined by the state of PWM3 and PWM4. Tie PWM3 to VCC to configure for 2-phase operation. Tie PWM4 to VCC to configure for 3-phase operation.

ISEN1, ISEN2, ISEN3, ISEN4

Current sense inputs. The ISEN1, ISEN2, ISEN3, and ISEN4 pins are held to a virtual ground such that a resistor connected between them and the drain terminal of the associated lower MOSFET will carry a current proportional to the current flowing through the related channel. The current is determined by the negative voltage developed across the lower MOSFET's $r_{DS(ON)}$ which is the channel current scaled by the inverse of the $r_{DS(ON)}$. The current is used as a reference for channel balancing, protection, and load-line regulation (via the FB pin). Inactive channels should have their respective current sense inputs left open.

PGOOD

PGOOD is used as an indication of the end of soft-start per the microprocessor specification. It is an open-drain logic output that is low impedance until the soft start is completed. It will be pulled low again once the undervoltage point is reached.

OFS

The OFS pin provides a means to program a dc current for generating an offset voltage at the REF input. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unterminated.

OFSOUT (ISL6556ACR only)

OFSOUT is the output of the offset-current generating circuit. It must be connected either to REF (recommended) or FB to generate a dc offset.

OVP

Overvoltage protection pin. This pin pulls to VCC and is latched when an overvoltage condition is detected. Connect this pin to the gate of an SCR or MOSFET tied from V_{IN} or V_{OUT} to ground to prevent damage to the load. This pin may be pulled as high as 15V to ground with an external resistor. However, it is only capable of pulling low when VCC is above 2V.

Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6556A controller helps in simplifying the implementation by integrating vital functions and requiring minimal output components. The block diagrams on pages 2 and 3 provide top level views of multi-phase power conversion using the ISL6556ACB and ISL6556ACR controllers.

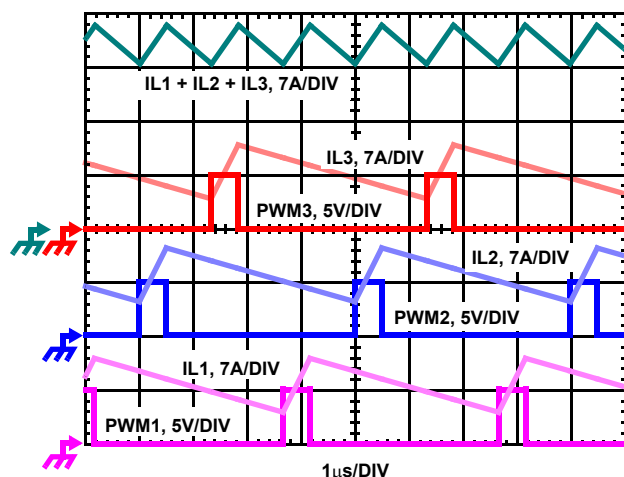


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the

ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents ($IL1$, $IL2$, and $IL3$) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) V_{OUT}}{L f_S V_{IN}} \quad (\text{EQ. 1})$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{L, PP} = \frac{(V_{IN} - N V_{OUT}) V_{OUT}}{L f_S V_{IN}} \quad (\text{EQ. 2})$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase

converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

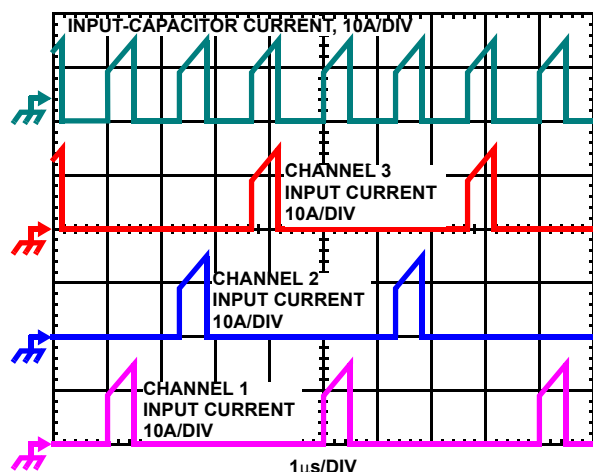


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 14, 15 and 16 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 17 shows the single phase input-capacitor RMS current for comparison.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL6556A is four. One switching cycle is defined as the time between PWM1 pulse termination signals. The pulse termination signal is the internally generated clock signal that triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands the channel-1 PWM output to go low. The PWM1 transition signals the channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/4 of a cycle after PWM1. The PWM3 output follows another 1/4 of a cycle after PWM2. PWM4 terminates another 1/4 of a cycle after PWM3.

If PWM3 is connected to VCC, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle later. Connecting PWM4 to VCC selects three channel operation and the pulse-termination times are spaced in 1/3 cycle increments.

Once a PWM signal transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to

ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP} , minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 4. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal, turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal remains high until the pulse termination signal commands the beginning of the next cycle by triggering the PWM signal low.

Current Sensing

During the forced off time following a PWM transition low, the controller senses channel current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$ (see Figure 3). A ground-referenced operational amplifier, internal to the ISL6556A, is connected to the PHASE node through a resistor, R_{ISEN} . The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L . The ISEN current is sampled and held after sufficient settling time every switching cycle. The sampled current, I_n , is used for channel-current balance, load-line regulation, overcurrent protection, and module current sharing. From Figure 3, the following equation for I_n is derived

$$I_n = I_L \frac{r_{DS(ON)}}{R_{ISEN}} \quad (\text{EQ. 3})$$

where I_L is the channel current.

If $r_{DS(ON)}$ sensing is not desired, an independent current-sense resistor in series with the lower MOSFET source can serve as a sense element. The circuitry shown in Figure 3 represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending upon the status of the PWM3 and PWM4 pins as described under *PWM Operation* section.

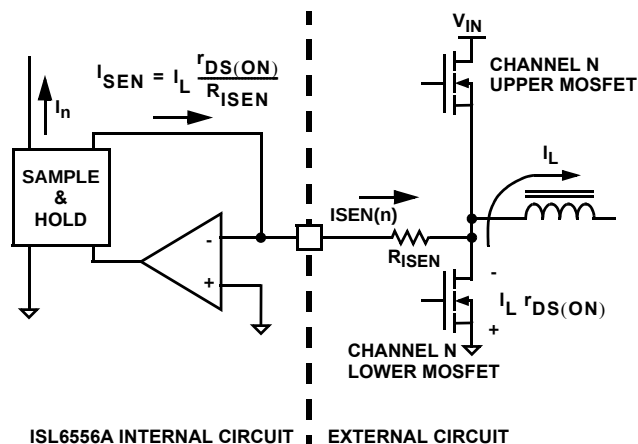


FIGURE 3. INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

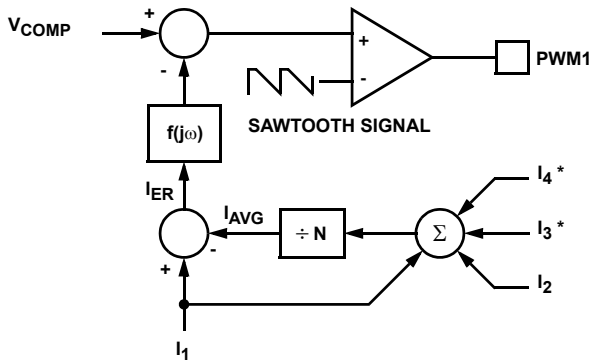
Channel-Current Balance

The sampled current, I_n , from each active channel is used to gauge both overall load current and the relative channel current carried in each leg of the converter. The individual sample currents are summed and divided by the number of active channels. The resulting average current, I_{AVG} , provides a measure of the total load current demand on the converter and the appropriate level of channel current. Using Figures 3 and 4, the average current is defined as

$$I_{AVG} = \frac{I_1 + I_2 + \dots + I_N}{N} \quad (\text{EQ. 4})$$

$$I_{AVG} = \frac{I_{OUT}}{N} \frac{r_{DS(ON)}}{R_{ISEN}}$$

where N is the number of active channels and I_{OUT} is the total load current.



NOTE: *Channels 3 and 4 are optional.

FIGURE 4. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

The average current is subtracted from the individual channel sample currents. The resulting error current, I_{ER} , is filtered to modify V_{COMP} . The modified V_{COMP} signal is compared to a sawtooth ramp signal to produce a modified pulse width which corrects for any unbalance and drives the error current toward zero. Figure 4 illustrates Intersil's patented current-balance method as implemented on channel-1 of a multi-phase converter.

Two considerations designers face are MOSFET selection and inductor design. Both are significantly improved when channel currents track at any load level. The need for complex drive schemes for multiple MOSFETs, exotic magnetic materials, and expensive heat sinks is avoided, resulting in a cost-effective and easy-to-implement solution relative to single-phase conversion. Channel-current balance insures that the thermal advantage of multi-phase conversion is realized. Heat dissipation in multiple channels is spread over a greater area than can easily be accomplished using the single phase approach.

In some circumstances, it may be necessary to deliberately design some channel-current unbalance into the system. In a highly compact design, one or two channels may be able

to cool more effectively than the other(s) due to nearby air flow or heat sinking components. The other channel(s) may have more difficulty cooling with comparatively less air flow and heat sinking. The hotter channels may also be located close to other heat-generating components tending to drive their temperature even higher. In these cases, the proper selection of the current sense resistors (R_{ISEN} in Figure 3) introduces channel current unbalance into the system. Increasing the value of R_{ISEN} in the cooler channels and decreasing it in the hotter channels moves all channels into thermal balance at the expense of current balance.

Voltage Regulation

The integrating compensation network shown in Figure 5 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6556A to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP} , is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage. The internal and external circuitry that controls voltage regulation is illustrated in Figure 5.

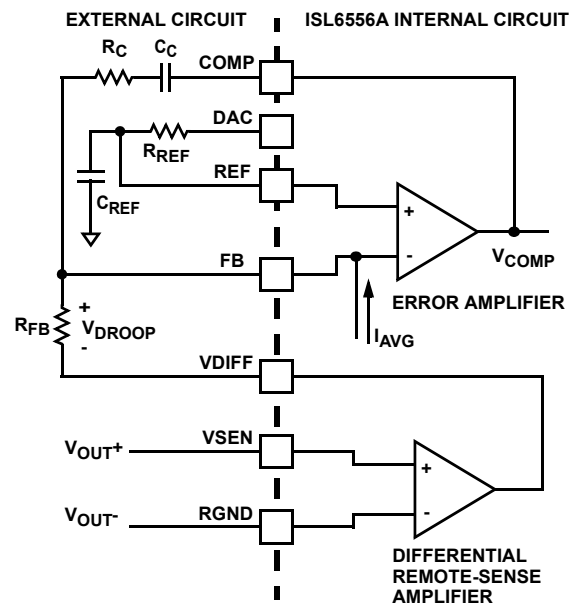


FIGURE 5. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

The ISL6556A incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-

inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense output, V_{DIFF} , is connected to the inverting input of the error amplifier through an external resistor.

A digital to analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID4 through VID12.5. The DAC decodes the 6-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 20 μ A pull-up to an internal 2.5V source for use with open-drain outputs. The pull-up current diminishes to zero above the logic threshold to protect voltage-sensitive output devices. External pull-up resistors can augment the pull-up current sources in case leakage into the driving device is greater than 20 μ A.

TABLE 1. VOLTAGE IDENTIFICATION (VID) CODES

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.8500V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.8750V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.9000V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.9250V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.9500V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.9750V
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.0000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.0250V
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.0500V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.0750V
0	0	0	0	0	0	1.0875V
1	1	1	1	1	1	OFF
1	1	1	1	1	0	OFF
1	1	1	1	0	1	1.1000V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.1250V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.1500V

TABLE 1. VOLTAGE IDENTIFICATION (VID) CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.1750V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.2000V
1	1	0	1	0	0	1.2125V
1	1	0	0	1	1	1.2250V
1	1	0	0	1	0	1.2475V
1	1	0	0	0	1	1.2500V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.2750V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.3000V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.3250V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.3500V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.3750V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.4000V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.4250V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.4500V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.4750V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.5000V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.5250V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.5500V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.5750V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Load-Line Regulation

Some microprocessor manufacturers require a precisely-controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can be level in the direction that works to control the voltage spike coincident with fast load current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 5, a current proportional to the average current in all active channels, I_{AVG} , flows from FB through a load-line regulation resistor, R_{FB} . The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as:

$$V_{DROOP} = I_{AVG} R_{FB} \quad (EQ. 5)$$

In most cases, each channel uses the same R_{ISEN} value to sense current. A more complete expression for V_{DROOP} is derived by combining Equations 4 and 5.

$$V_{DROOP} = \frac{I_{OUT}}{N} \frac{r_{DS(ON)}}{R_{ISEN}} R_{FB} \quad (EQ. 6)$$

Output-Voltage Offset Programming

The ISL6556A allows the designer to accurately adjust the offset voltage. When a resistor, R_{OFS} , is connected between OFS and VCC, the voltage across it is regulated to 2.0V. This causes a proportional current (I_{OFS}) to flow into OFS. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.5V, and I_{OFS} flows out of OFS. A resistor between DAC and REF, R_{REF} , is selected so that the product ($I_{OFS} \times R_{REF}$) is equal to the desired offset voltage. These functions are shown in Figures 6 and 7.

As evident in Figure 7, the OFSOUT pin must be connected to the REF pin for this current injection to function in ISL6556ACR. The current flowing through R_{REF} creates an offset at the REF pin, which is ultimately duplicated at the output of the regulator.

Once the desired output offset voltage has been determined, use the following formulae to set R_{OFS} :

For Positive Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{2 \times R_{REF}}{V_{OFFSET}} \quad (EQ. 7)$$

For Negative Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.5 \times R_{REF}}{V_{OFFSET}} \quad (EQ. 8)$$

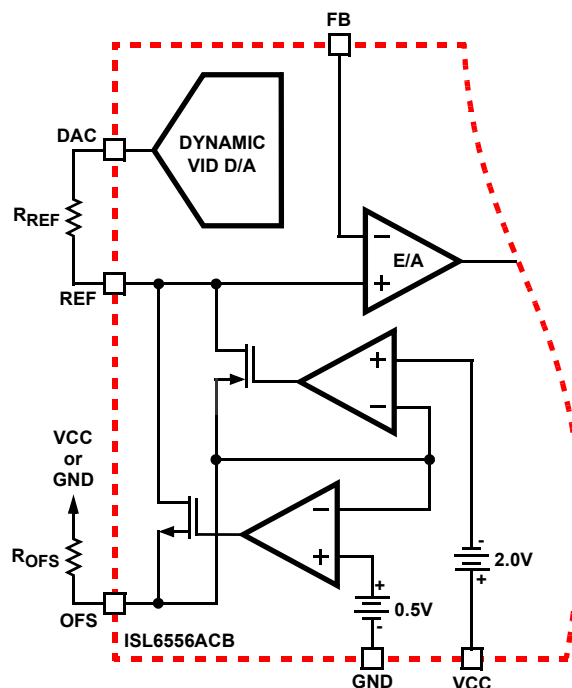


FIGURE 6. OUTPUT VOLTAGE OFFSET PROGRAMMING WITH ISL6556ACB (28-LEAD SOIC)

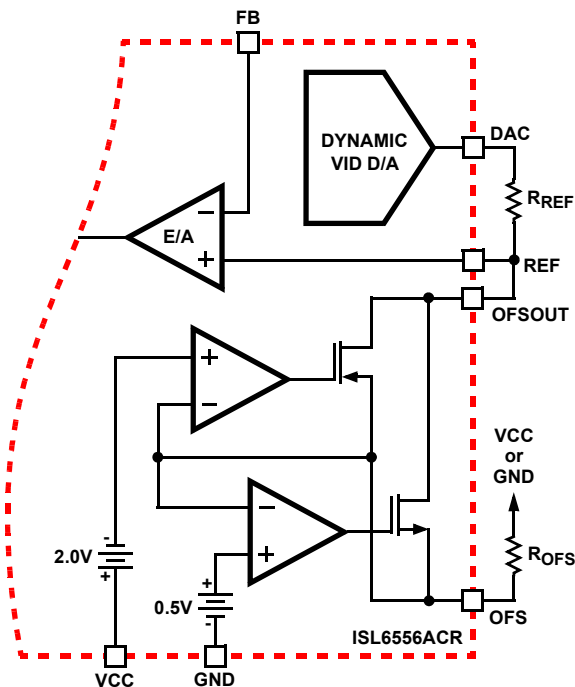


FIGURE 7. OUTPUT VOLTAGE OFFSET PROGRAMMING WITH ISL6556ACR (32-LEAD QFN)

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs during regulator operation. The power management solution is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption is a necessary function of the core-voltage regulator.

The ISL6556A checks the VID inputs six times every switching cycle. If the VID code is found to have changed, the controller waits half of a complete cycle before executing a 12.5mV change. If during the half-cycle wait period, the difference between DAC level and the new VID code changes sign, no change is made. If the VID code is more than 1 bit higher or lower than the DAC (not recommended), the controller will execute 12.5mV changes six times per cycle until VID and DAC are equal. It is for this reason that it is important to carefully control the rate of VID stepping in 1-bit increments.

In order to ensure the smooth transition of output voltage during VID change, a VID step change smoothing network composed of R_{REF} and C_{REF} is required for an ISL6556A based voltage regulator. The selection of R_{REF} is based on the desired offset as detailed above in *Output-Voltage Offset Programming*. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID} , the relationship between the time constant of R_{REF} and C_{REF} network and T_{VID} is given by Equation 9.

$$C_{REF} R_{REF} = 4 T_{VID} \quad (\text{EQ. 9})$$

Typically R_{REF} is selected to be 1k Ω , so with a VID step change rate of 5 μ s per bit, the value of C_{REF} is 22nF based on Equation 9.

Initialization

Prior to initialization, proper conditions must exist on the enable inputs and VCC. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, PGOOD asserts logic 1.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met before the ISL6556A is released from shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6556A is guaranteed. Hysteresis between the

rising and falling thresholds assure that once enabled, the ISL6556A will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

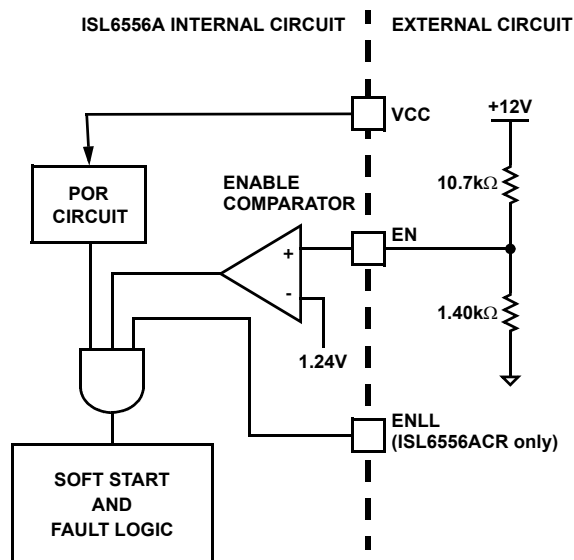


FIGURE 8. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

2. The ISL6556A features an enable input (EN) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6556A in shutdown until the voltage at EN rises above 1.24V. The enable comparator has about 100mV of hysteresis to prevent bounce. It is important that the driver ICs reach their POR level before the ISL6556A becomes enabled. The schematic in Figure 8 demonstrates sequencing the ISL6556A with the HIP660X family of Intersil MOSFET drivers, which require 12V bias.
3. (ISL6556ACR only) The voltage on ENLL must be logic high to enable the controller. This pin is typically connected to the VID_PGOOD. The ISL6556ACB has this signal internally connected high.
4. The VID code must not be 111111 or 111110. These codes signal the controller that no load is present. The controller will enter shut-down mode after receiving either of these codes and will execute soft start upon receiving any other code. These codes can be used to enable or disable the controller but it is not recommended. After receiving one of these codes, the controller executes a 2-cycle delay before changing the overvoltage trip level to the shut-down level and disabling PWM. Overvoltage shutdown cannot be reset using one of these codes.

To enable the controller, VCC must be greater than the POR threshold; the voltage on EN must be greater than 1.24V; for ISL6556ACR, ENLL must be logic high; and VID cannot be equal to 111111 or 111110. When each of these conditions is true, the controller immediately begins the soft-start sequence.

Soft-Start

During soft start, the DAC voltage ramps linearly from zero to the programmed VID level. The PWM signals remain in the high-impedance state until the controller detects that the ramping DAC level has reached the output-voltage level. This protects the system against the large, negative inductor currents that would otherwise occur when starting with a pre-existing charge on the output as the controller attempted to regulate to zero volts at the beginning of the soft-start cycle. The soft-start time, t_{SS} , begins with a delay period equal to 64 switching cycles followed by a linear ramp with a rate determined by the switching period, $1/f_{SW}$.

$$t_{SS} = \frac{64 + 1280 \cdot VID}{f_{SW}} \quad (\text{EQ. 10})$$

For example, a regulator with 250kHz switching frequency having VID set to 1.35V has t_{SS} equal to 6.912ms.

A 100mV offset exists on the remote-sense amplifier at the beginning of soft start and ramps to zero during the first 640 cycles of soft start (704 cycles following enable). This prevents the large inrush current that would otherwise occur should the output voltage start out with a slight negative bias.

During the first 640 cycles of soft start (704 cycles following enable) the DAC voltage increments the reference in 25mV steps. The remainder of soft start sees the DAC ramping with 12.5mV steps.

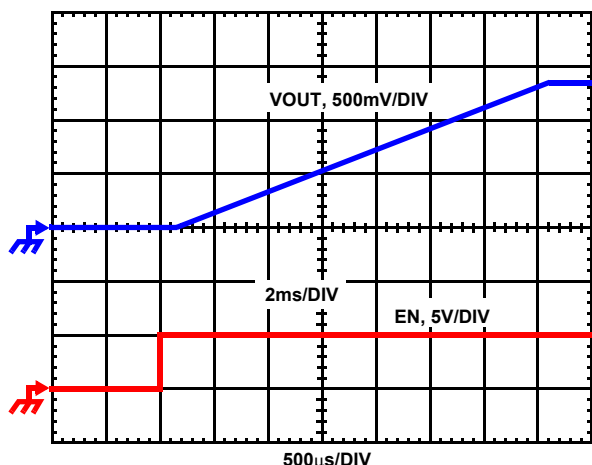


FIGURE 9. SOFT-START WAVEFORMS WITH AN UN-BIASED OUTPUT. FSW = 500kHz

Fault Monitoring and Protection

The ISL6556A actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 10 outlines the interaction between the fault monitors and the power good signal.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output that transitions high when the converter is operating after soft start.

PGOOD pulls low during shutdown and releases high after a successful soft start. PGOOD only transitions low when an undervoltage condition is detected or the controller is disabled by a reset from EN, ENLL, POR, or one of the no-CPU VID codes. After an undervoltage event, PGOOD will return high unless the controller has been disabled. PGOOD does not automatically transition low upon detection of an overvoltage condition.

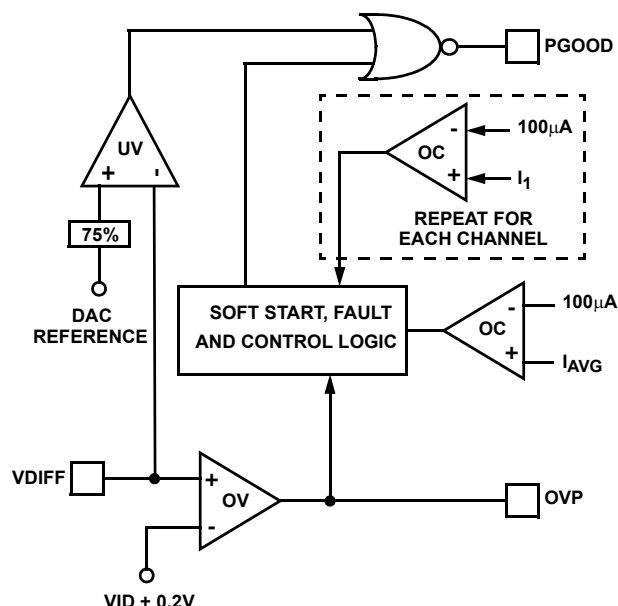


FIGURE 10. POWER GOOD AND PROTECTION CIRCUITRY

Undervoltage Detection

The undervoltage threshold is set at 75% of the VID code. When the output voltage at VSEN is below the undervoltage threshold, PGOOD gets pulled low.

Overvoltage Protection

When VCC is above 1.4V, but otherwise not valid as defined under **Power on Reset** in *Electrical Specifications*, the overvoltage trip circuit is active using auxiliary circuitry. In this state, an overvoltage trip occurs if the voltage at VSEN exceeds 1.8V.

With valid VCC, the overvoltage circuit is sensitive to the voltage at VDIFF. In this state, the trip level is 1.7V prior to valid enable conditions being met as described in *Enable and Disable*. The only exception to this is when the IC has been disabled by an overvoltage trip. In that case the overvoltage trip point is VID plus 200mV. During soft start, the overvoltage trip level is the higher of 1.7V or VID plus 200mV. Upon successful soft start, the overvoltage trip level is 200mV above VID. Two actions are taken by the

ISL6556A to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low until the voltage at VSEN falls below 0.6V with valid VCC or 1.5V otherwise. This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level that might cause damage to the load. The PWM outputs remain low until VDIFF falls to the programmed DAC level when they enter a high-impedance state. The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, the ISL6556A will again command the lower MOSFETs to turn on. The ISL6556A will continue to protect the load in this fashion as long as the overvoltage condition recurs.

Simultaneous to the protective action of the PWM outputs, the OVP pin pulls to VCC delivering up to 100mA to the gate of a crowbar MOSFET or SCR placed either on the input rail or the output rail. Turning on the MOSFET or SCR collapses the power rail and causes a fuse placed further up stream to blow. The fuse must be sized such that the MOSFET or SCR will not overheat before the fuse blows. The OVP pin is tolerant to 12V (see *Absolute Maximum Ratings*), so an external resistor pull up can be used to augment the driving capability. If using a pull up resistor in conjunction with the internal overvoltage protection function, care must be taken to avoid nuisance trips that could occur when VCC is below 2V. In that case, the controller is incapable of holding OVP low.

Once an overvoltage condition is detected, normal PWM operation ceases until the ISL6556A is reset. Cycling the voltage on EN or ENLL or VCC below the POR-falling threshold will reset the controller. Cycling the VID codes will not reset the controller.

Overcurrent Protection

ISL6556A has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition on a delayed basis, while the combined phase currents are protected on an instantaneous basis.

In instantaneous protection mode, the ISL6556A takes advantage of the proportionality between the load current and the average current, I_{AVG} to detect an overcurrent condition. See the *Channel-Current Balance* section for more detail on how the average current is measured. The average current is continually compared with a constant 100 μ A reference current as shown in Figure 10. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown.

In individual overcurrent protection mode, the ISL6556A continuously compares the current of each channel with the same 100 μ A reference current. If any channel current exceeds the reference current continuously for eight consecutive cycles, the comparator triggers the converter to shutdown.

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft start. If the fault remains, trip-retry cycles continue indefinitely as shown in Figure 11 until either controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard during this kind of operation.

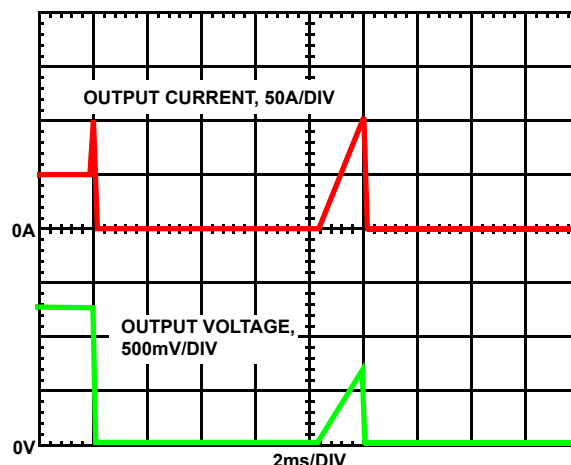


FIGURE 11. OVERCURRENT BEHAVIOR IN HICCUP MODE.
 $F_{SW} = 500\text{kHz}$

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power-supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15 and 20A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current may be pushed as high as above 30A per phase, but these designs

require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 11, I_M is the maximum continuous output current; I_{PP} is the peak-to-peak inductor current (see Equation 1); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = r_{DS(ON)} \left[\left(\frac{I_M}{N} \right)^2 (1-d) + \frac{I_{L,PP}^2 (1-d)}{12} \right] \quad (EQ. 11)$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M , $V_{D(ON)}$; the switching frequency, f_S ; and the length of dead times, t_{d1} and t_{d2} , at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} f_S \left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2} \right) t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2} \right) t_{d2} \right] \quad (EQ. 12)$$

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times; the lower-MOSFET body-diode reverse-recovery charge, Q_{rr} ; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 13,

the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN} \left(\frac{I_M}{N} + \frac{I_{PP}}{2} \right) \left(\frac{t_1}{2} \right) f_S \quad (EQ. 13)$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2 . In Equation 14, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN} \left(\frac{I_M}{N} - \frac{I_{PP}}{2} \right) \left(\frac{t_2}{2} \right) f_S \quad (EQ. 14)$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr} . Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can draw all of Q_{rr} , it is conducted through the upper MOSFET across V_{IN} . The power dissipated as a result is $P_{UP,3}$ and is approximately

$$P_{UP,3} = V_{IN} Q_{rr} f_S \quad (EQ. 15)$$

Finally, the resistive part of the upper MOSFETs is given in Equation 16 as $P_{UP,4}$.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 13, 14, 15 and 16. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

$$P_{UP,4} \approx r_{DS(ON)} \left[\left(\frac{I_M}{N} \right)^2 d + \frac{I_{PP}^2}{12} \right] \quad (EQ. 16)$$

Current Sensing

The ISEN pins are denoted ISEN1, ISEN2, ISEN3 and ISEN4. The resistors connected between these pins and the respective phase nodes determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point. Select values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs; the full-load operating current, I_{FL} ; and the number of phases, N using Equation 17 (see also Figure 3).

$$R_{ISEN} = \frac{r_{DS(ON)} I_{FL}}{70 \times 10^{-6} N} \quad (EQ. 17)$$

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistor. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of R_{ISEN} for the affected phases (see the section entitled *Channel-Current Balance*). Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad (EQ. 18)$$

In Equation 18, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 18 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load-Line Regulation Resistor

The load-line regulation resistor is labeled R_{FB} in Figure 5. Its value depends on the desired full-load droop voltage (V_{DROOP} in Figure 5). If Equation 17 is used to select each ISEN resistor, the load-line regulation resistor is as shown in Equation 19.

$$R_{FB} = \frac{V_{DROOP}}{70 \times 10^{-6}} \quad (\text{EQ. 19})$$

If one or more of the ISEN resistors is adjusted for thermal balance, as in Equation 18, the load-line regulation resistor should be selected according to Equation 20 where I_{FL} is the full-load operating current and $R_{ISEN(n)}$ is the ISEN resistor connected to the n^{th} ISEN pin.

$$R_{FB} = \frac{V_{DROOP}}{I_{FL} r_{DS(ON)}} \sum_n R_{ISEN(n)} \quad (\text{EQ. 20})$$

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in *Load-Line Regulation*.

COMPENSATING LOAD-LINE REGULATED CONVERTER

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C .

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator by compensating the L-C poles and the ESR zero of the voltage-mode approximation yields a solution that is always stable with very close to ideal transient performance.

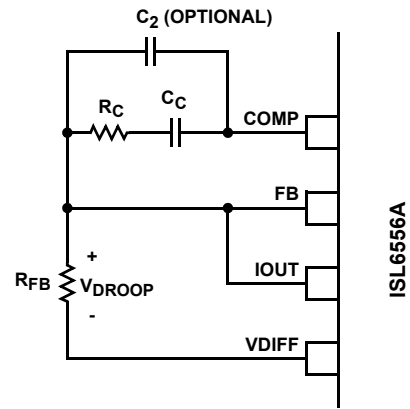


FIGURE 12. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6556A CIRCUIT

The feedback resistor, R_{FB} , has already been chosen as outlined in *Load-Line Regulation Resistor*. Select a target bandwidth for the compensated system, f_0 . The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

Case 1: $\frac{1}{2\pi\sqrt{LC}} > f_0$

$$R_C = R_{FB} \frac{2\pi f_0 V_{PP} \sqrt{LC}}{0.75 V_{IN}}$$

$$C_C = \frac{0.75 V_{IN}}{2\pi V_{PP} R_{FB} f_0}$$

Case 2: $\frac{1}{2\pi\sqrt{LC}} \leq f_0 < \frac{1}{2\pi C(ESR)}$

$$R_C = R_{FB} \frac{V_{PP}(2\pi)^2 f_0^2 LC}{0.75 V_{IN}} \quad (\text{EQ. 21})$$

$$C_C = \frac{0.75 V_{IN}}{(2\pi)^2 f_0^2 V_{PP} R_{FB} \sqrt{LC}}$$

Case 3: $f_0 > \frac{1}{2\pi C(ESR)}$

$$R_C = R_{FB} \frac{2\pi f_0 V_{PP} L}{0.75 V_{IN}(ESR)}$$

$$C_C = \frac{0.75 V_{IN}(ESR) \sqrt{C}}{2\pi V_{PP} R_{FB} f_0 \sqrt{L}}$$

In Equations 21, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 4 and *Electrical Specifications*.

Once selected, the compensation values in Equations 21 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C . Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equations 21 unless some performance issue is noted.

The optional capacitor C_2 , is sometimes needed to bypass noise away from the PWM comparator (see Figure 12). Keep a position available for C_2 , and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading-edge jitter problem is noted.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI ; the load-current slew rate, di/dt ; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX} . Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx (ESL) \frac{di}{dt} + (ESR) \Delta I \quad (EQ. 22)$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output

voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}$ (ESR). Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR) \frac{(V_{IN} - N V_{OUT}) V_{OUT}}{f_S V_{IN} V_{PP(MAX)}} \quad (EQ. 23)$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX} . This places an upper limit on inductance.

Equation 24 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 25 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually

$$L \leq \frac{2NCV_O}{(\Delta I)^2} [\Delta V_{MAX} - \Delta I(ESR)] \quad (EQ. 24)$$

$$L \leq \frac{(1.25)NC}{(\Delta I)^2} [\Delta V_{MAX} - \Delta I(ESR)] (V_{IN} - V_O) \quad (EQ. 25)$$

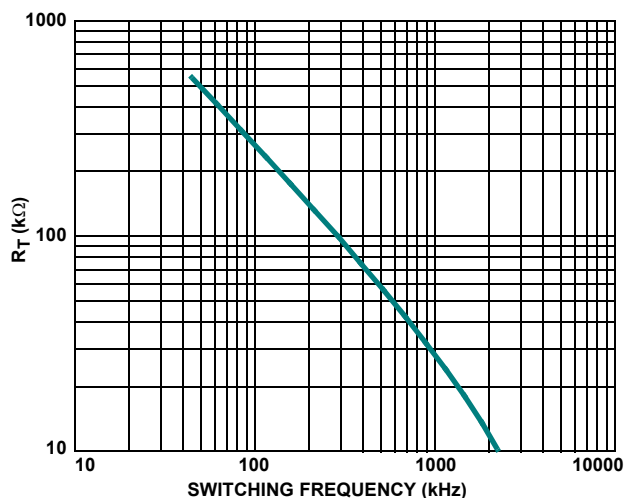
less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

Input Supply Voltage Selection

The VCC input of the ISL6556A can be connected either directly to a +5V supply or through a current limiting resistor to a +12V supply. An integrated 5.8V shunt regulator maintains the voltage on the VCC pin when a +12V supply is used. A 300 Ω resistor is suggested for limiting the current into the VCC pin to a worst-case maximum of approximately 25mA.

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Output Filter Design*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

FIGURE 13. R_T vs SWITCHING FREQUENCY

Switching frequency is determined by the selection of the frequency-setting resistor, R_T (see the figures labeled *Typical Application* on pages 4 and 5). Figure 13 and Equation 26 are provided to assist in selecting the correct value for R_T .

$$R_T = 1.0203(10)^{[10.6258 - (1.03167)\log(f_s)] - 1200} \quad (\text{EQ. 26})$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

For a two phase design, use Figure 14 to determine the input-capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L,PP}$) to I_O . Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

Figures 15 and 16 provide the same input RMS current information for three and four phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as described above.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize suppression.

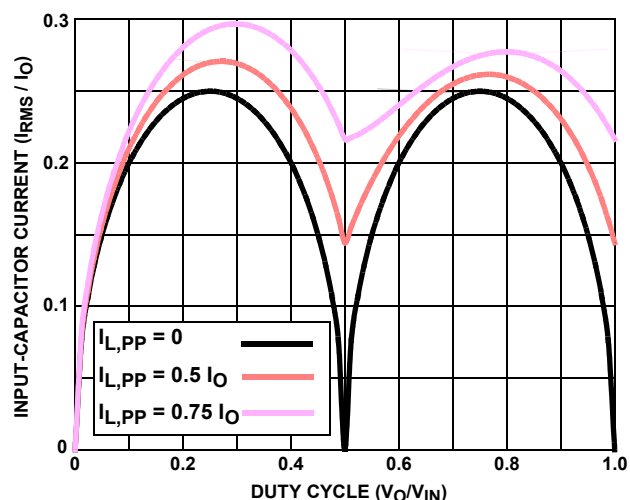


FIGURE 14. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

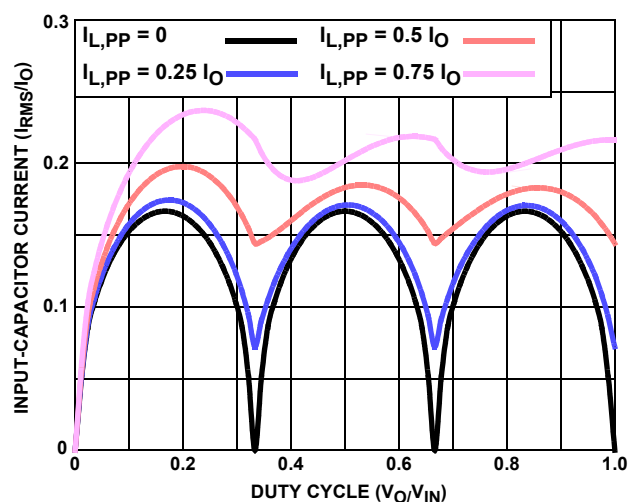


FIGURE 15. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

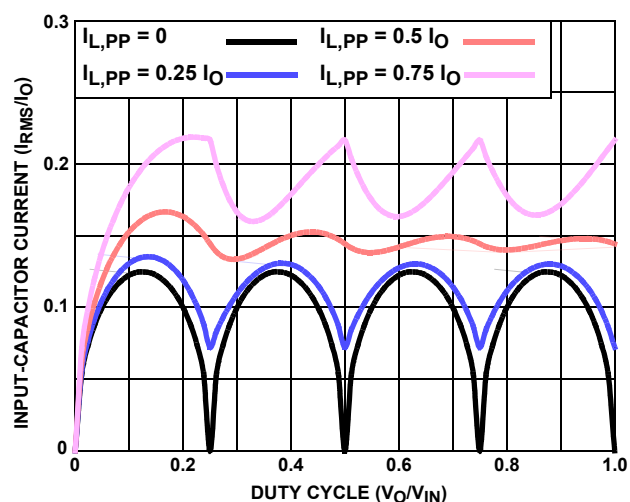


FIGURE 16. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

MULTI-PHASE RMS IMPROVEMENT

Figure 17 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multi-phase topology. For example, compare the input RMS current requirements of a two-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{C,PP}$ to I_O of 0.5. The single phase converter would require 17.3 Arms current capacity while the two-phase converter would only require 10.9 Arms. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

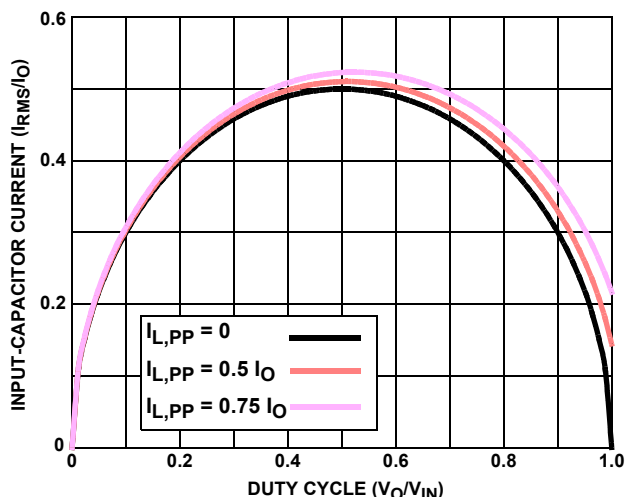


FIGURE 17. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

Layout Considerations

The following layout strategies are intended to minimize the impact of board parasitic impedances on converter performance and to optimize the heat-dissipating capabilities of the printed-circuit board. These sections highlight some important practices which should not be overlooked during the layout process.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position one high-frequency ceramic input capacitor next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

The ISL6556A can be placed off to one side or centered relative to the individual phase switching components. Routing of sense lines and PWM signals will guide final placement. Critical small signal components to place close to the controller include the ISEN resistors, R_T resistor, feedback resistor, and compensation components.

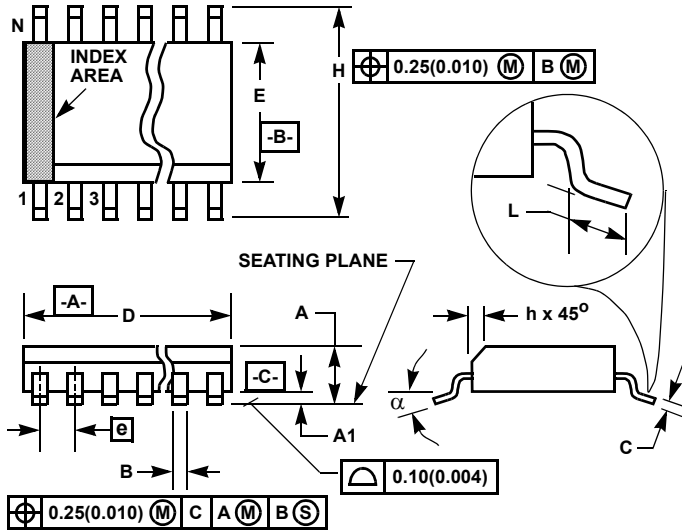
Bypass capacitors for the ISL6556A and HIP660X driver bias supplies must be placed next to their respective pins. Trace parasitic impedances will reduce their effectiveness.

Plane Allocation and Routing

Dedicate one solid layer, usually a middle layer, for a ground plane. Make all critical component ground connections with vias to this plane. Dedicate one additional layer for power planes; breaking the plane up into smaller islands of common voltage. Use the remaining layers for signal wiring.

Route phase planes of copper filled polygons on the top and bottom once the switching component placement is set. Size the trace width between the driver gate pins and the MOSFET gates to carry 1A of current. When routing components in the switching path, use short wide traces to reduce the associated parasitic impedances.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

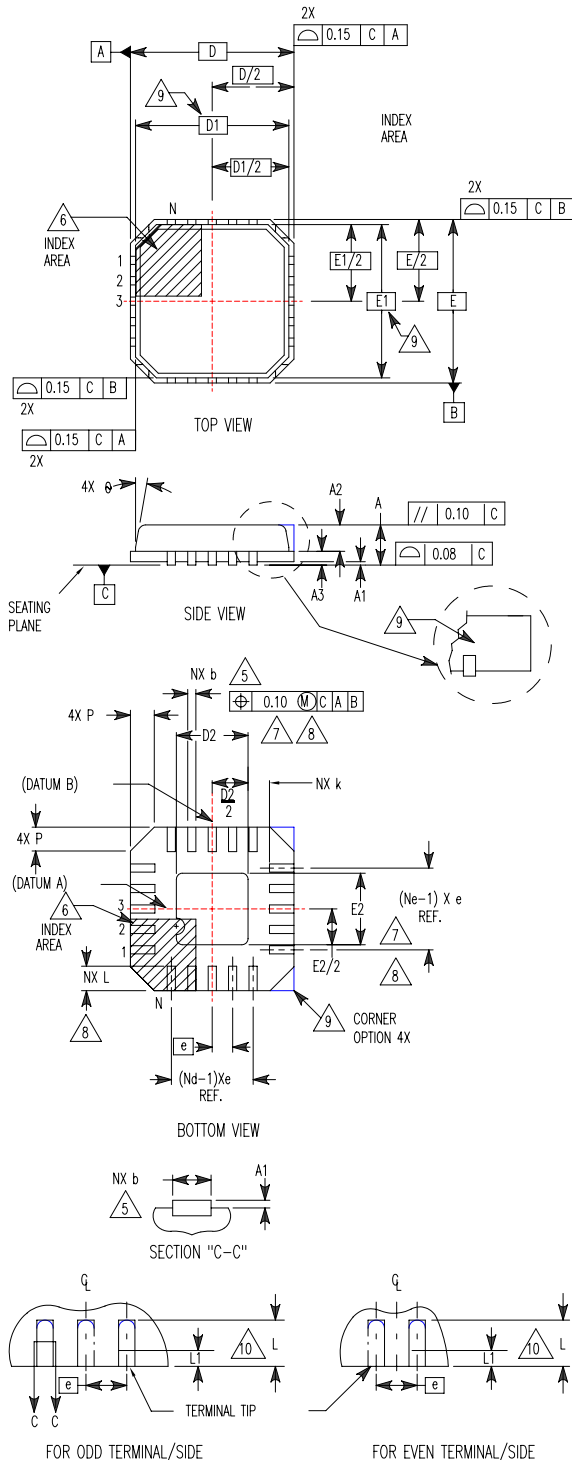
M28.3 (JEDEC MS-013-AE ISSUE C)

28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

**Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)**



L32.5x5B

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5,8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	3.15	3.30	3.45	7,8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	3.15	3.30	3.45	7,8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N	32			2
Nd	8			3
Ne	8			3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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