



## MILITARY HIGH SPEED 32K x 8 CMOS PROM/RPROM

### KEY FEATURES

- **Ultra-Fast Access Time**
  - 45 ns
- **Low Power Consumption**
- **Fast Programming**
- **Immune to Latch-UP**
  - Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Available in 300 and 600 Mil DIP and CLLCC**

### GENERAL DESCRIPTION

The WS57C71C is a High Performance 256K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology and utilizes WSI's patented self-aligned split gate EPROM cell.

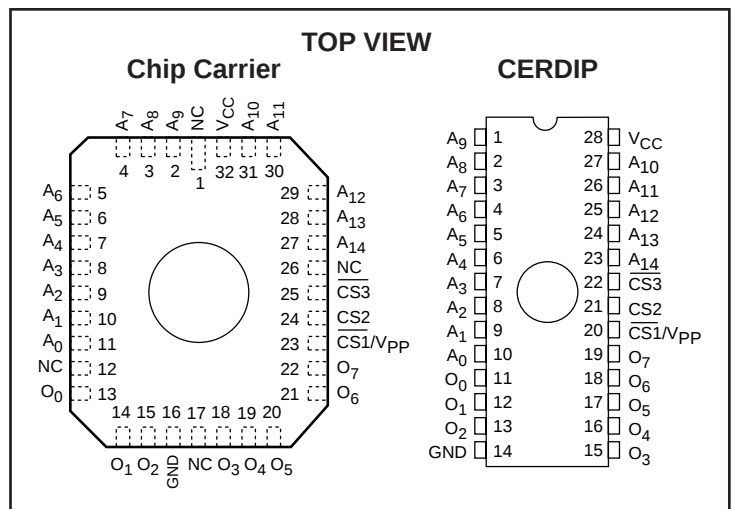
The industry standard PROM pin configuration of the WS57C71C provides an easy upgrade path from a 16K x 8 device.

This RPPROM is capable of operating at speeds as fast as 35 ns address access time, which enables it to be used directly with today's fast microprocessors and DSP processors without introducing any wait states. All inputs and outputs are TTL compatible. The WS57C71C is a low power device even when operated at its fastest speed. The DIP version is packaged in a 300 mil wide DIP package saving board space for the user.

### MODE SELECTION

| MODE \ PINS     | $\overline{CS1}/V_{PP}$ | CS2      | $\overline{CS3}$ | $V_{CC}$ | OUTPUTS   |
|-----------------|-------------------------|----------|------------------|----------|-----------|
| Read            | $V_{IL}$                | $V_{IH}$ | $V_{IL}$         | $V_{CC}$ | $D_{OUT}$ |
| Output Disable  | $V_{IH}$                | X        | X                | $V_{CC}$ | High Z    |
| Output Disable  | X                       | $V_{IL}$ | X                | $V_{CC}$ | High Z    |
| Output Disable  | X                       | X        | $V_{IH}$         | $V_{CC}$ | High Z    |
| Program         | $V_{PP}$                | X        | $V_{IH}$         | $V_{CC}$ | $D_{IN}$  |
| Program Verify  | $V_{IL}$                | $V_{IH}$ | $V_{IL}$         | $V_{CC}$ | $D_{OUT}$ |
| Program Inhibit | $V_{PP}$                | X        | $V_{IL}$         | $V_{CC}$ | HIGH Z    |

### PIN CONFIGURATION



### PRODUCT SELECTION GUIDE

| PARAMETER                     | WS57C71C-45 | WS57C71C-55 | WS57C71C-70 |
|-------------------------------|-------------|-------------|-------------|
| Address Access Time (Max)     | 45 ns       | 55 ns       | 70 ns       |
| CS to Output Valid Time (Max) | 20 ns       | 20 ns       | 30 ns       |

**ORDERING INFORMATION**

| PART NUMBER    | SPEED (ns) | PACKAGE TYPE        | PACKAGE DRAWING | OPERATING TEMPERATURE RANGE | WSI MANUFACTURING PROCEDURE |
|----------------|------------|---------------------|-----------------|-----------------------------|-----------------------------|
| WS57C71C-45TMB | 45         | 28 Pin CERDIP, 0.3" | T2              | Military                    | MIL-STD-883C                |
| WS57C71C-55CMB | 55         | 32 Pad CLLCC        | C2              | Military                    | MIL-STD-883C                |
| WS57C71C-55DMB | 55         | 28 Pin CERDIP, 0.6" | D2              | Military                    | MIL-STD-883C                |
| WS57C71C-55TMB | 55         | 28 Pin CERDIP, 0.3" | T2              | Military                    | MIL-STD-883C                |
| WS57C71C-70TMB | 70         | 28 Pin CERDIP, 0.3" | T2              | Military                    | MIL-STD-883C                |

**NOTE:** 9. The actual part marking will not include the initials "WS."

**PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS**

**REFER TO  
PAGE 5-1**

The WS57C71C is programmed using Algorithm D shown on page 5-9.

*For complete data sheet and electrical specifications see page 2-55.*

