Very Low Power/Voltage CMOS SRAM
512K X 8 bit

BS62LV4007

■ FEATURES

- Vcc operation voltage : 4.5V ~ 5.5V
- Very low power consumption :
  Vcc = 5.0V C-grade: 68mA (@55ns) operating current
  I -grade: 70mA (@55ns) operating current
  C-grade: 58mA (@70ns) operating current
  I -grade: 60mA (@70ns) operating current
  2.0uA (Typ.) CMOS standby current
- High speed access time :
  -55 55ns
  -70 70ns
- Automatic power down when chip is deselected
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options
- Three state outputs and TTL compatible

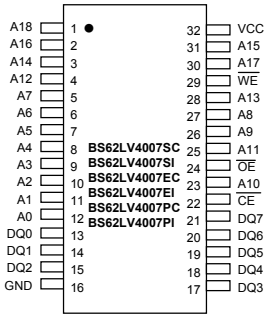
■ DESCRIPTION

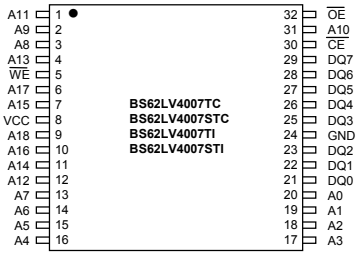
The BS62LV4007 is a high performance, very low power CMOS Static Random Access Memory organized as 524,288 words by 8 bits and operates from a range of 4.5V to 5.5V supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 2.0uA at 5.0V/25°C and maximum access time of 55ns at 5.0V/85°C.
Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) , and active LOW output enable ($\overline{OE}$) and three-state output drivers.
The BS62LV4007 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The BS62LV4007 is available in the JEDEC standard 32L SOP, TSOP , PDIP, TSOP II and STSOP package.

■ PRODUCT FAMILY

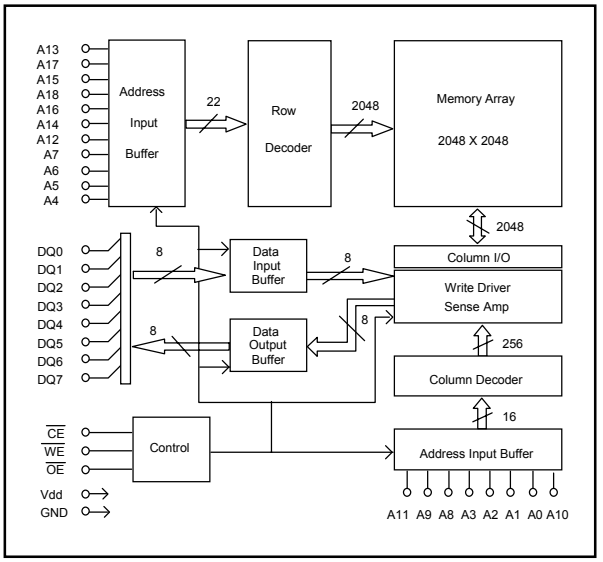
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION			PKG TYPE
				STANDBY (I_{CCSB1} , Max)	Operating (I_{CC} , Max)		
			55ns:4.5~5.5V 70ns:4.5~5.5V	Vcc =5.0V	Vcc = 5.0V 55ns	Vcc =5.0V 70ns	
BS62LV4007TC	+0 ° C to +70 ° C	4.5V ~ 5.5V	55 / 70	30uA	68mA	58mA	TSOP- 32
BS62LV4007STC							STSOP-32
BS62LV4007SC							SOP -32
BS62LV4007EC							TSOP2-32
BS62LV4007PC							PDIP -32
BS62LV4007TI	-40 ° C to +85 ° C	4.5V ~ 5.5V	55 / 70	60uA	70mA	60mA	TSOP-32
BS62LV4007STI							STSOP-32
BS62LV4007SI							SOP -32
BS62LV4007EI							TSOP2-32
BS62LV4007PI							PDIP -32

■ PIN CONFIGURATIONS





■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A18 Address Input	These 19 address inputs select one of the 524,288 x 8-bit words in the RAM
$\overline{CE}$ Chip Enable Input	$\overline{CE}$ is active LOW. Chip enables must be active when data read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
DQ0-DQ7 Data Input/Output Ports	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
GND	Ground

■ TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	Vcc CURRENT
Not selected	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	DOUT	I_{CC}
Write	L	L	X	DIN	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TBIAS	Temperature Under Bias	-40 to +85	^{O}C
TSTG	Storage Temperature	-60 to +150	^{O}C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0 ^{O}C to +70 ^{O}C	4.5V ~ 5.5V
Industrial	-40 ^{O}C to +85 ^{O}C	4.5V ~ 5.5V

■ CAPACITANCE (1) (TA = 25ºC, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	VI/O=0V	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = -40 to + 85°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS			MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(3)			Vcc = 5.0 V	-0.5	--	0.8	V
V_{IH}	Guaranteed Input High Voltage(3)			Vcc = 5.0 V	2.2	--	Vcc+0.3	V
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc			--	--	1	uA
I_{LO}	Output Leakage Current	Vcc = Max, $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc			--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL} = 2.0mA		Vcc = 5.0 V	--	--	0.4	V
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -1.0mA		Vcc = 5.0 V	2.4	--	--	V
I_{CC} (5)	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, F=Fmax(2)	Vcc = 5.0 V	55ns	--	--	70	mA
				70ns			60	
I_{CCSB}	Standby Current-TTL	$\overline{CE}$ = V_{IH}, I_{DQ} = 0mA		Vcc = 5.0 V	--	--	1.0	mA
I_{CCSB1} (4)	Standby Current-CMOS	$\overline{CE}$ ≧ Vcc-0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V		Vcc = 5.0 V	--	2.0	60	uA

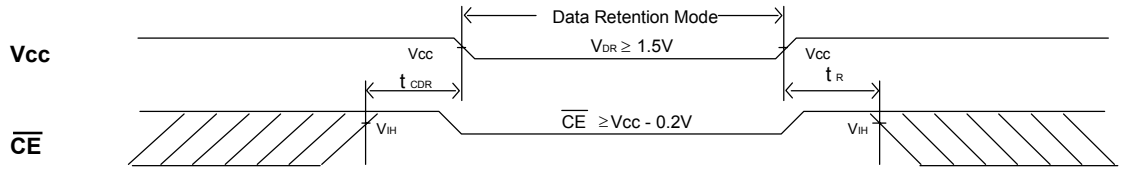
1. Typical characteristics are at TA = 25°C.
2. Fmax = $1/t_{RC}$.
3. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
4. $I_{CCSB1\_MAX.}$ is 30uA at Vcc=5.0V and TA=70°C.
5. $I_{CC\_MAX.}$ is 68mA(@55ns) / 58mA(@70ns) at Vcc=5.0V and TA=0~70°C.

■ DATA RETENTION CHARACTERISTICS (TA = -40 to + 85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE}$ ≧ Vcc - 0.2V V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.5	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≧ Vcc - 0.2V V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	0.3	1.3	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.5V, T_A = + 25°C
2. t_{RC} = Read Cycle Time
3. $I_{CCDR\_MAX.}$ is 0.8uA at TA=70°C.

■ LOW V_{CC} DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



■AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels	Vcc / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	C_L = 30pF+1TTL C_L = 100pF+1TTL

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

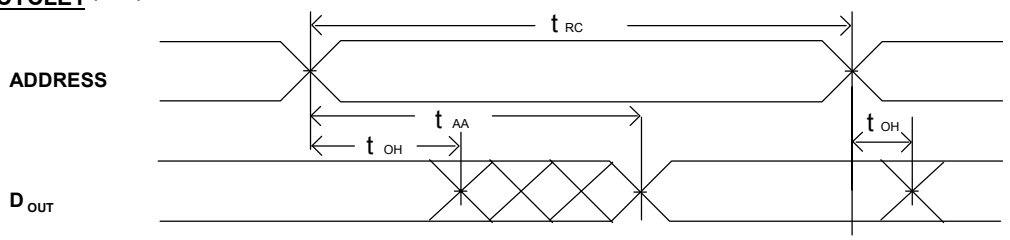
■ AC ELECTRICAL CHARACTERISTICS (TA = -40 to + 85°C)

READ CYCLE

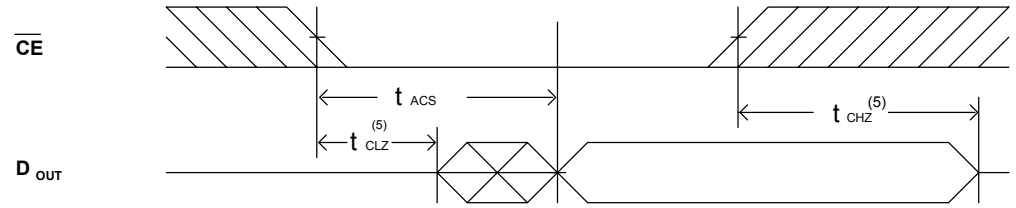
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns (Vcc = 4.5~5.5V) MIN.	TYP.	MAX.	CYCLE TIME : 70ns (Vcc = 4.5~5.5V) MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	55	--	--	70	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time	--	--	55	--	--	70	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time	--	--	55	--	--	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	30	--	--	35	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10	--	--	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	10	--	--	10	--	--	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	--	--	30	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t_{AXOX}	t_{OH}	Data Hold from Address Change	10	--	--	10	--	--	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

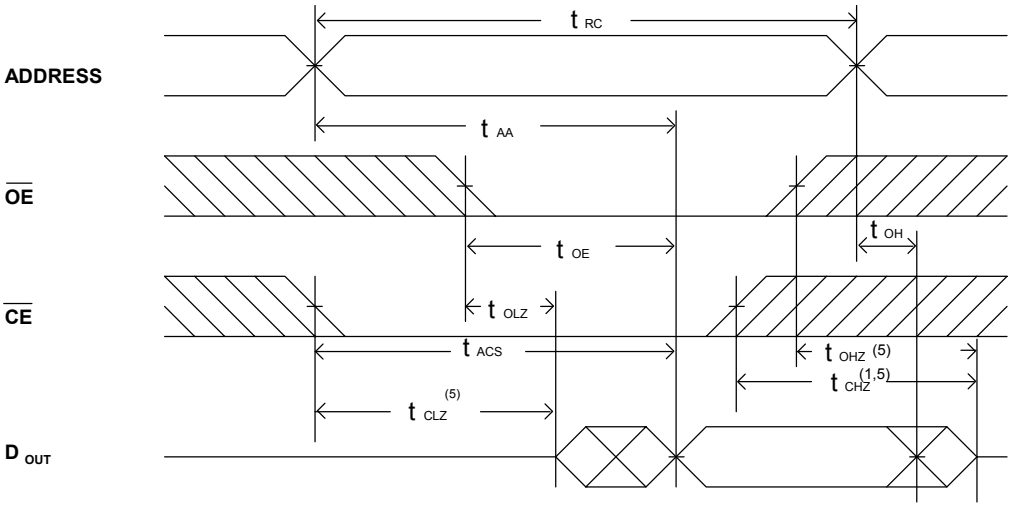
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL} .
5. The parameter is guaranteed but not 100% tested.

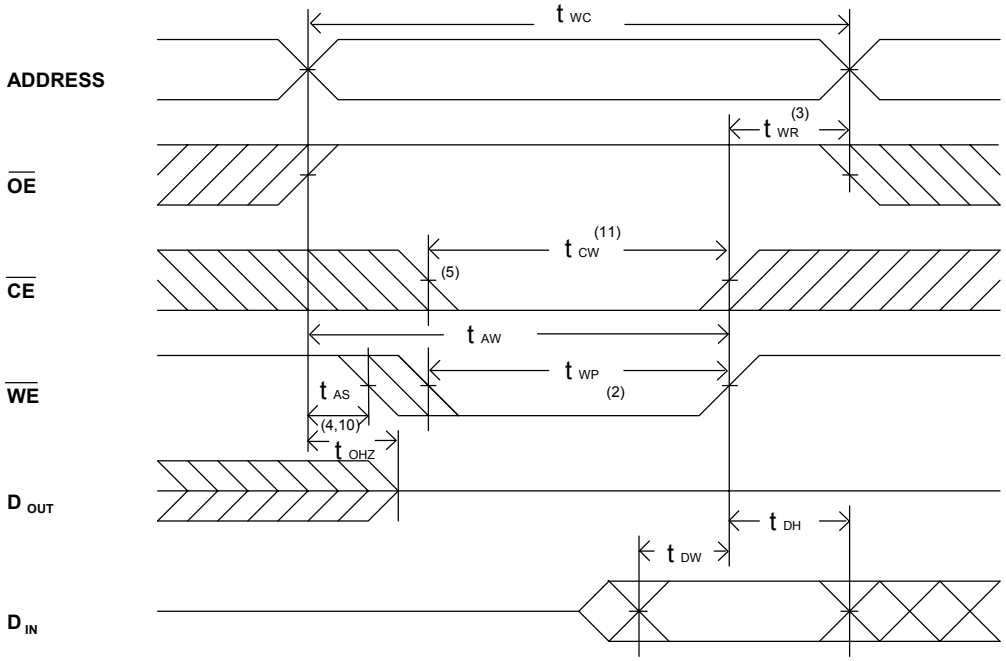
■ AC ELECTRICAL CHARACTERISTICS (TA = -40 to + 85°C)

WRITE CYCLE

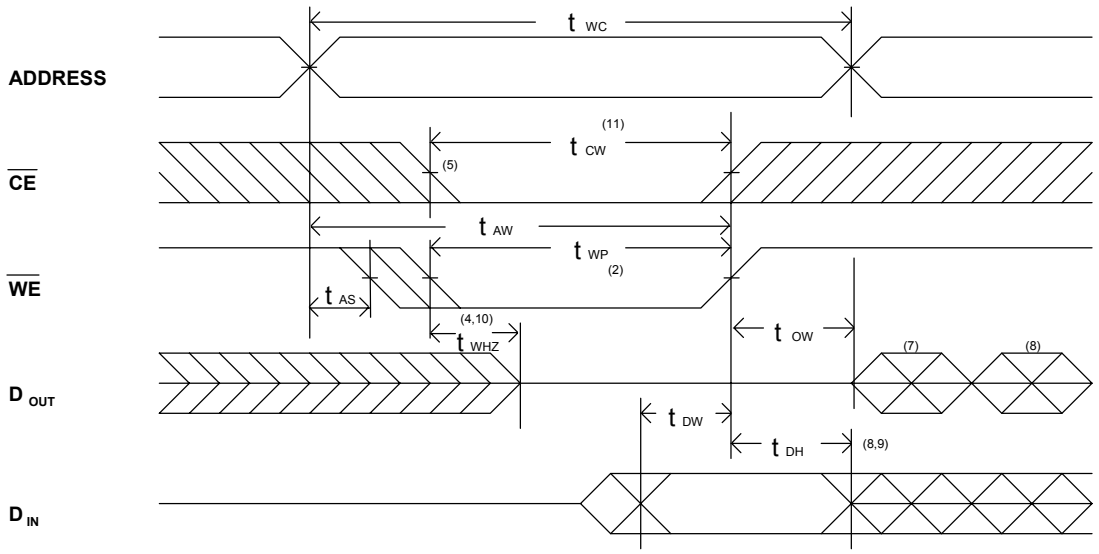
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns (Vcc = 4.5~5.5V) MIN.	TYP.	MAX.	CYCLE TIME : 70ns (Vcc = 4.5~5.5V) MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	55	--	--	70	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	55	--	--	70	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55	--	--	70	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	30	--	--	35	--	--	ns
t_{WHAX}	t_{WR}	Write Recovery Time ($\overline{CE}$, $\overline{WE}$)	0	--	--	0	--	--	ns
t_{WLOZ}	t_{WHZ}	Write to Output in High Z	--	--	25	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	--	--	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHOZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t_{WHQX}	t_{OW}	Endot Write to Output Active	5	--	--	5	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



WRITE CYCLE2 (1,6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.

■ ORDERING INFORMATION

BS62LV4007 X X Z Y Y

SPEED
55: 55ns
70: 70ns

PKG MATERIAL
-: Normal
G: Green
P: Pb free

GRADE
C: +0°C ~ +70°C
I: -40°C ~ +85°C

PACKAGE
S: SOP
E: TSOP 2
ST: Small TSOP
T: TSOP
P: PDIP

Note:
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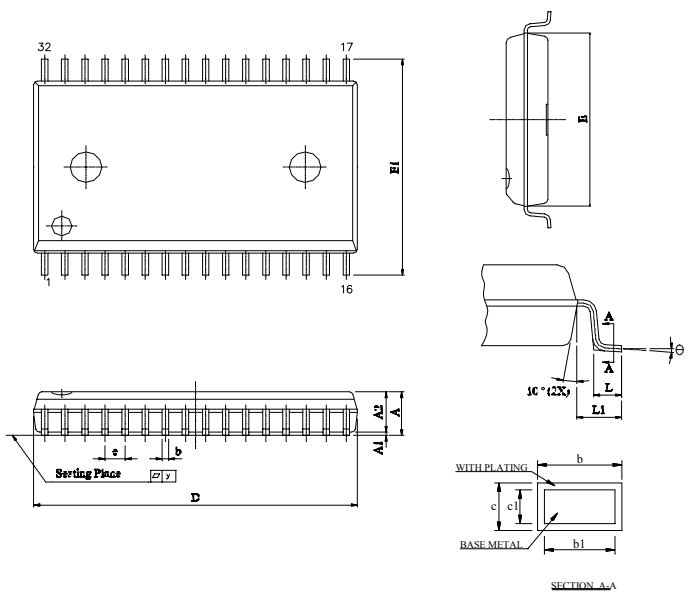
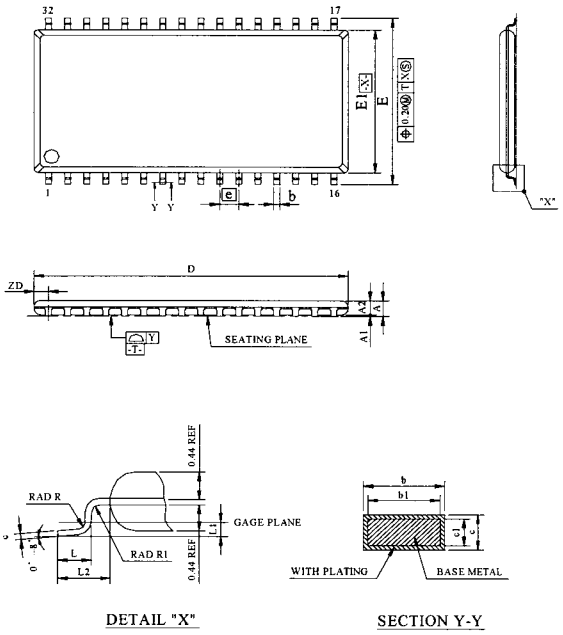
■ PACKAGE DIMENSIONS



SYMBOL \ UNIT	INCH	MM
A	0.111±0.007	2.821±0.176
A1	0.009±0.005	0.229±0.127
A2	0.1055±0.0055	2.680±0.140
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.46
c	0.006 ~ 0.012	0.15 ~ 0.32
c1	0.006 ~ 0.011	0.15 ~ 0.28
D	0.805±0.005	20.447±0.127
E	0.445±0.005	11.303±0.127
E1	0.555±0.012	14.097±0.305
e	0.050±0.006	1.270±0.152
L	0.033±0.010	0.834±0.25
L1	0.055±0.008	1.397±0.203
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

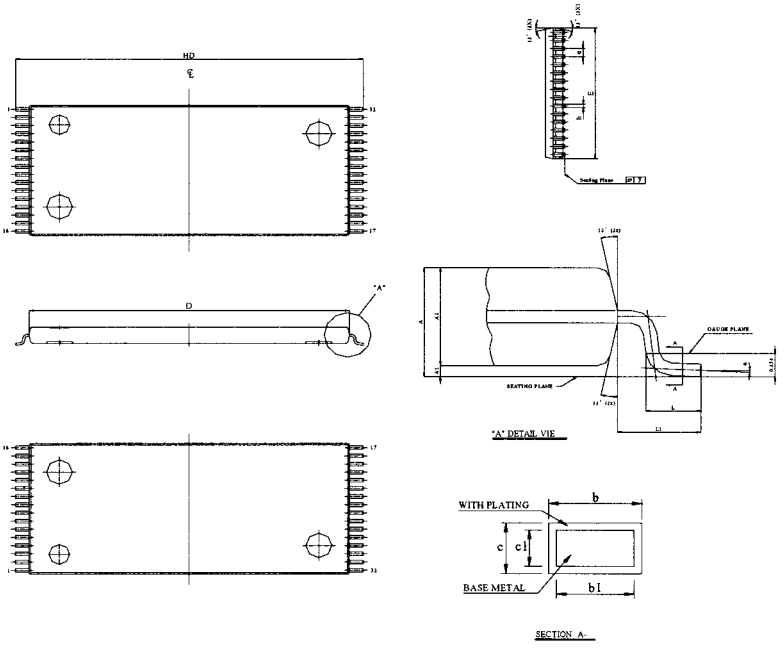
SOP -32



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
b	0.30		0.52	0.012		0.020
b1	0.30	0.40	0.45	0.012	0.016	0.018
c	0.12		0.21	0.005		0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.394	0.400	0.405
e	1.27 BASIC			0.050 BASIC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 BASIC		
L2	0.8 REF			0.031 REF		
R	0.12		0.25	0.005		0.010
R1	0.12			0.005		
ZD	0.95 REF			0.037 REF		
Y			0.10			0.004

NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS.
2. REFREENCE DOCUMENT : JEDEC MS-024
3. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.
   MOLD PROTRUSION SHALL NOT EXCEED 0.15(0.006") PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.
   INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25(0.01") PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD T
   BE WIDER THAN THE MAX bDIMENSION BY MORE THAN 0.13.
   DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER
   THAN THE MIN b DIMENSION BY MORE THAN0.07mm.

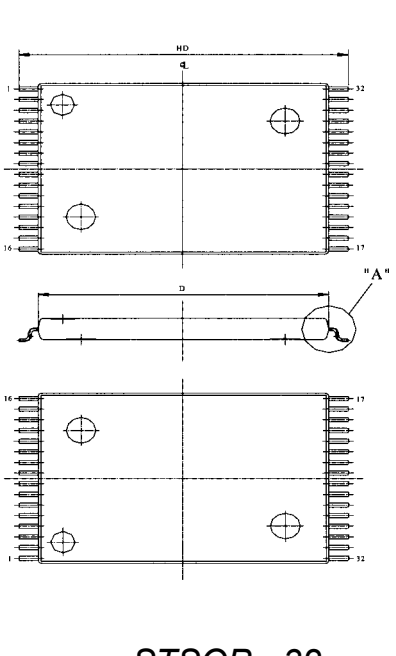
TSOP2 - 32

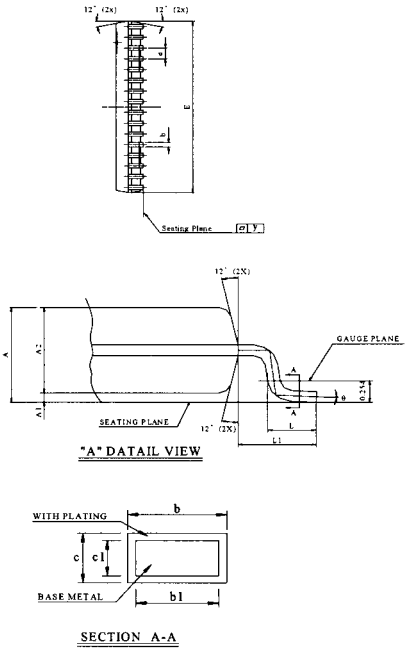


UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.724± 0.004	18.40± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.787± 0.008	20.00± 0.20
L	0.0197 +0.008 -0.004	0.50 +0.2 -0.1
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

TSOP - 32

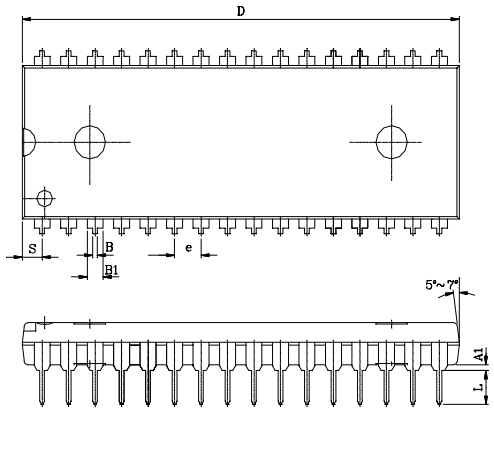
■ PACKAGE DIMENSIONS (continued)





UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.528± 0.008	13.40± 0.20
L	0.0197 $^{+0.008}_{-0.004}$	0.50 $^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

STSOP - 32



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.154±0.005	3.912±0.127
B	0.018±0.005	0.457±0.127
B1	0.050±0.005	1.270±0.127
c	0.010±0.004	0.254±0.102
D	1.650±0.005	41.910±0.127
E	0.600±0.010	15.240±0.254
E1	0.544±0.004	13.818±0.102
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508
L	0.130±0.010	3.302±0.254
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127

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