

# SN54AC86, SN74AC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCAS533A – AUGUST 1995 – REVISED MAY 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs**

## description

The 'AC86 are quadruple 2-input exclusive-OR gates. The devices perform the Boolean function  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$  in positive logic.

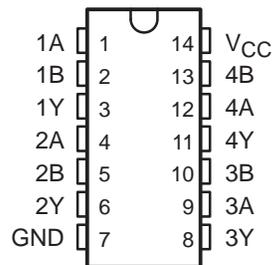
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54AC86 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AC86 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

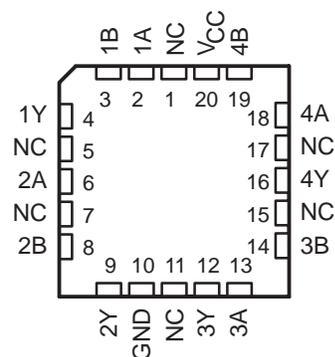
**FUNCTION TABLE**  
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

**SN54AC86 . . . J OR W PACKAGE**  
**SN74AC86 . . . D, DB, N, OR PW PACKAGE**  
(TOP VIEW)



**SN54AC86 . . . FK PACKAGE**  
(TOP VIEW)



NC – No internal connection



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**TEXAS  
INSTRUMENTS**

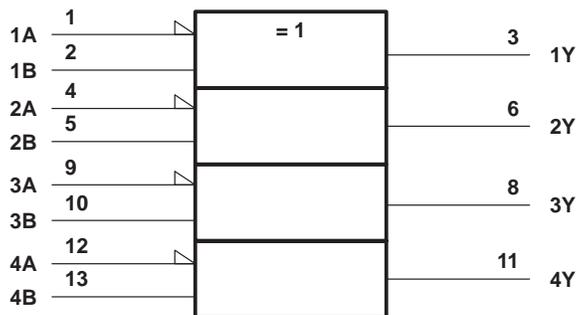
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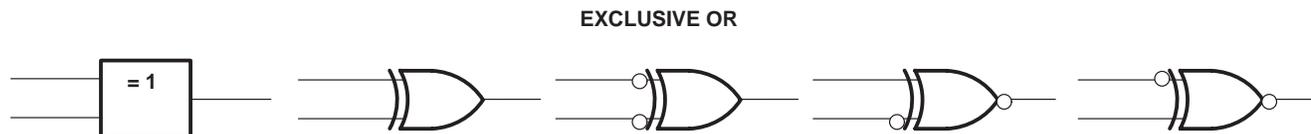
## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, PW, and W packages.

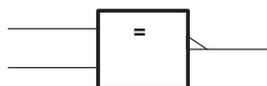
## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These five equivalent exclusive-OR symbols are valid for an 'AC86 gate in positive logic; negation may be shown at any two ports.

### LOGIC-IDENTITY ELEMENT



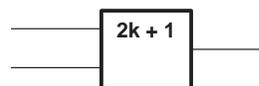
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

### EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

### ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V	
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA	
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA	
Continuous current through $V_{CC}$ or GND .....	±200 mA	
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	D package .....	1.25 W
	DB package .....	0.5 W
	N package .....	1.1 W
	PW package .....	0.5 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		SN54AC86		SN74AC86		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V		2.1	2.1	V
		$V_{CC} = 4.5$ V		3.15	3.15	
		$V_{CC} = 5.5$ V		3.85	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V		0.9	0.9	V
		$V_{CC} = 4.5$ V		1.35	1.35	
		$V_{CC} = 5.5$ V		1.65	1.65	
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3$ V		–12	–12	mA
		$V_{CC} = 4.5$ V		–24	–24	
		$V_{CC} = 5.5$ V		–24	–24	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V		12	12	mA
		$V_{CC} = 4.5$ V		24	24	
		$V_{CC} = 5.5$ V		24	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	8	0	8	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC86		SN74AC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
	I <sub>OH</sub> = -24 mA	5.5 V	4.86			4.7		4.76		
		I <sub>OH</sub> = -50 mA†	5.5 V			3.85				
I <sub>OH</sub> = -75 mA†	5.5 V						3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		5.5 V		0.001	0.1		0.1	0.1		
	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.5	0.44		
		I <sub>OL</sub> = 50 mA†	5.5 V				1.65			
I <sub>OL</sub> = 75 mA†	5.5 V						1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		40	20	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2.6				pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54AC86		SN74AC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	2	6.5	11.5	1	14	1.5	12.5	ns
t <sub>PHL</sub>			2	6	11.5	1	14	1.5	12.5	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

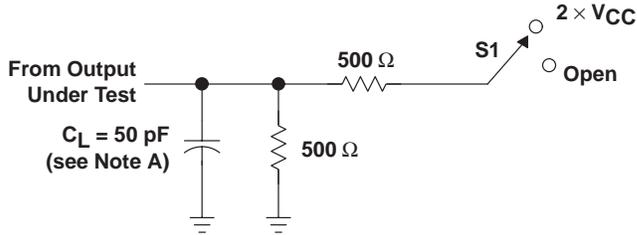
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54AC86		SN74AC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	1.5	4.5	8.5	1	10	1	9	ns
t <sub>PHL</sub>			1.5	4.5	8.5	1	10	1	9.5	

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	25	pF

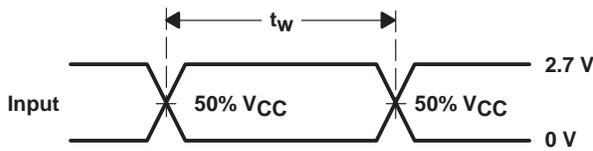


PARAMETER MEASUREMENT INFORMATION

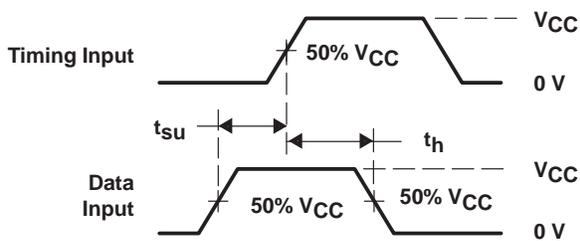


TEST	S1
$t_{PLH}/t_{PHL}$	Open

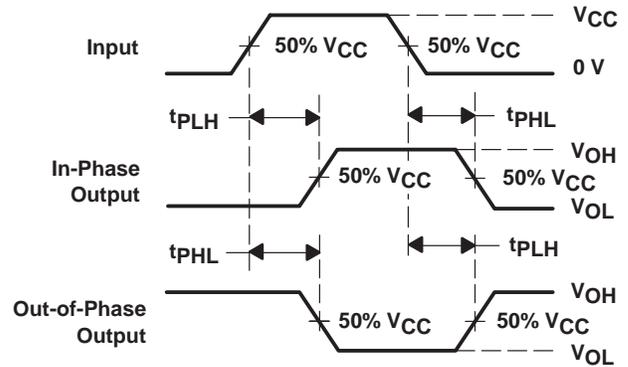
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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