

# SN54ACT534, SN74ACT534 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS556B – NOVEMBER 1995 – REVISED JANUARY 2000

- Inputs Are TTL-Voltage Compatible
- 3-State Inverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

## description

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

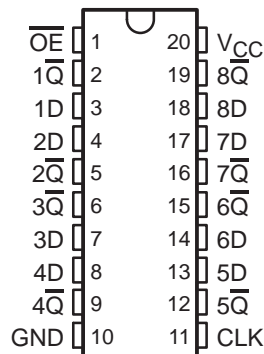
On the positive transition of the clock (CLK) input, the Q outputs are set to the complements of the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

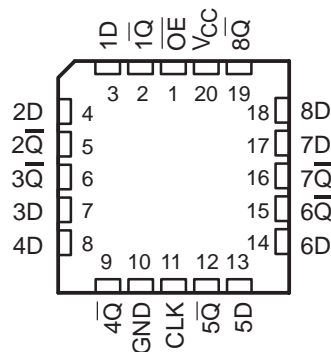
$\overline{OE}$  does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT534 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ACT534 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54ACT534 . . . J OR W PACKAGE  
SN74ACT534 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ACT534 . . . FK PACKAGE  
(TOP VIEW)



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**TEXAS  
INSTRUMENTS**

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# SN54ACT534, SN74ACT534

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

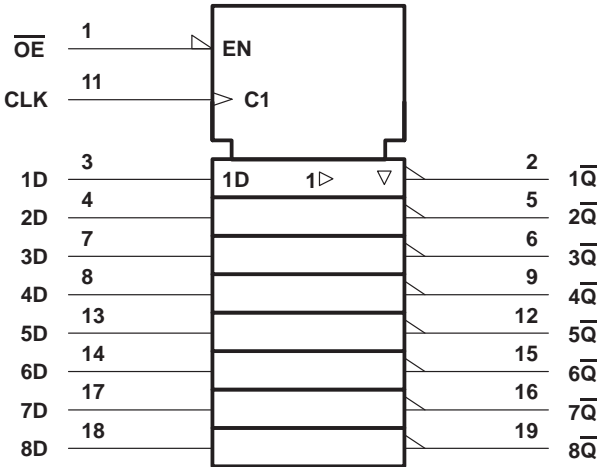
### WITH 3-STATE OUTPUTS

SCAS556B – NOVEMBER 1995 – REVISED JANUARY 2000

FUNCTION TABLE  
(each flip-flop)

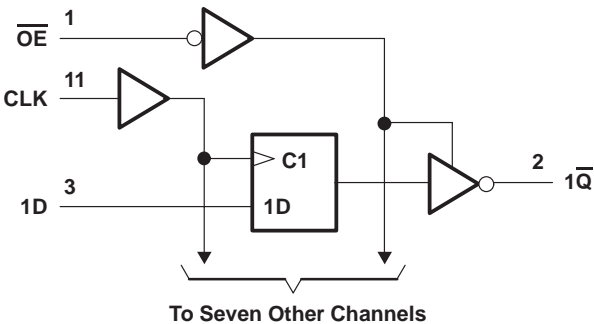
INPUTS			OUTPUT $\overline{Q}$
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	L
L	$\uparrow$	L	H
L	H or L	X	$\overline{Q_0}$
H	X	X	Z

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

# SN54ACT534, SN74ACT534 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS556B – NOVEMBER 1995 – REVISED JANUARY 2000

## recommended operating conditions (see Note 3)

		SN54ACT534		SN74ACT534		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–24		–24	mA
I <sub>OL</sub>	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	8	0	8	ns/V
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT534		SN74ACT534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I <sub>OH</sub> = –24 mA	4.5 V	3.8			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I <sub>OH</sub> = –50 mA†	5.5 V				3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 50 mA†	5.5 V				1.65				
	I <sub>OL</sub> = 75 mA†	5.5 V						1.65		
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±5		±2.5	μA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80		40	μA
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.6		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		SN54ACT534		SN74ACT534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, CLK high or low	3.5		5		3.5		ns
t <sub>su</sub>	Setup time, data before CLK↑	3.5		5		4		ns
t <sub>h</sub>	Hold time, data after CLK↑	1		3		1.5		ns

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# SN54ACT534, SN74ACT534

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### WITH 3-STATE OUTPUTS

SCAS556B – NOVEMBER 1995 – REVISED JANUARY 2000

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C		SN54ACT534		SN74ACT534		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100		85		120		MHz
t <sub>PLH</sub>	CLK	$\overline{Q}$	2.5	11.5	1.5	14	2	12.5	ns
t <sub>PHL</sub>			2	10.5	1.5	13	2	12	
t <sub>PZH</sub>	$\overline{OE}$	$\overline{Q}$	2.5	12	1.5	14	2	12.5	ns
t <sub>PZL</sub>			2	11	1.5	13	2	11.5	
t <sub>PHZ</sub>	$\overline{OE}$	$\overline{Q}$	1.5	12.5	1.5	14.5	1	13.5	ns
t <sub>PLZ</sub>			1.5	10.5	1.5	11.5	1	10.5	

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	40	pF

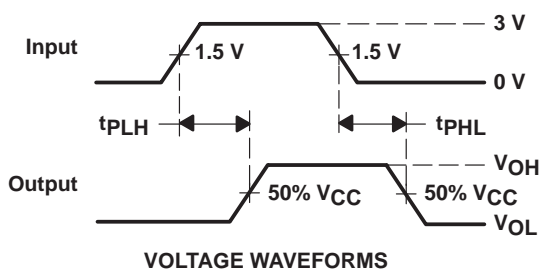
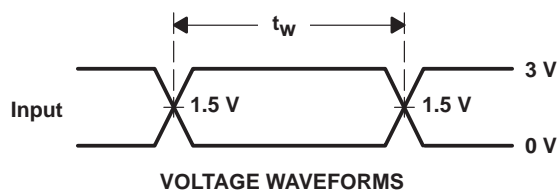
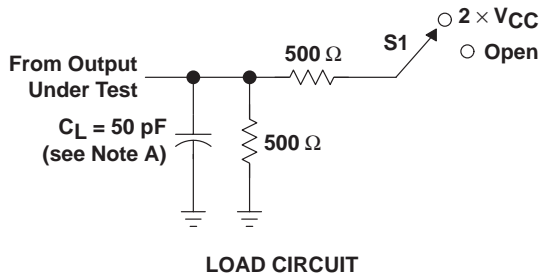
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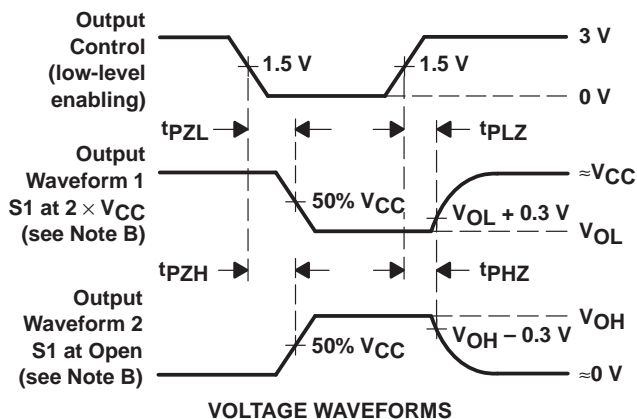
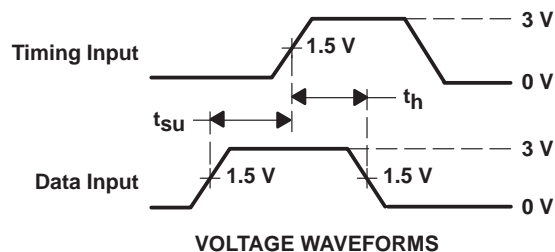
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SCAS556B – NOVEMBER 1995 – REVISED JANUARY 2000

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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