

SN74CBT16213 24-BIT FET BUS-EXCHANGE SWITCH

SCDS026F – MAY 1995 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT16213 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBT16213 is characterized for operation from –40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

S0	1	56	S1
1A1	2	55	S2
1A2	3	54	1B1
2A1	4	53	1B2
2A2	5	52	2B1
3A1	6	51	2B2
3A2	7	50	3B1
GND	8	49	GND
4A1	9	48	3B2
4A2	10	47	4B1
5A1	11	46	4B2
5A2	12	45	5B1
6A1	13	44	5B2
6A2	14	43	6B1
7A1	15	42	6B2
7A2	16	41	7B1
V _{CC}	17	40	7B2
8A1	18	39	8B1
GND	19	38	GND
8A2	20	37	8B2
9A1	21	36	9B1
9A2	22	35	9B2
10A1	23	34	10B1
10A2	24	33	10B2
11A1	25	32	11B1
11A2	26	31	11B2
12A1	27	30	12B1
12A2	28	29	12B2

FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	A2 and B2	A1 and B2	A1 port = A2 port = B2 port
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port



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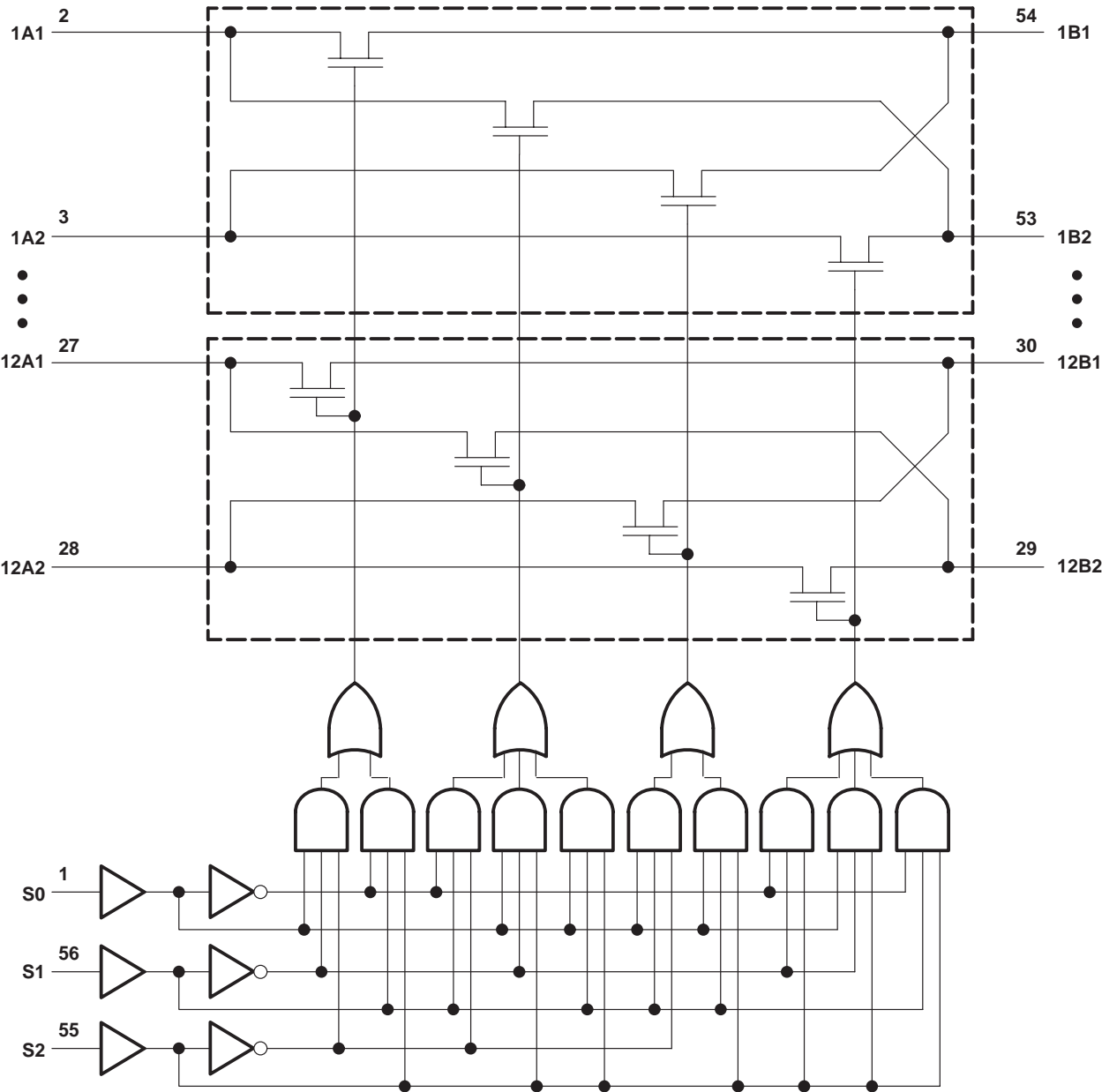
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logic diagram (positive logic)



Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51.

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
V _{IH}	High-level control input voltage	2		V
V _{IL}	Low-level control input voltage		0.8	V
T _A	Operating free-air temperature	−40	85	°C

PARAMETER		TEST CONDITIONS			MIN	TYP [‡]	MAX	UNIT		
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA					−1.2	V		
I _I		V _{CC} = 0, V _I = 5.5 V					10	μA		
		V _{CC} = 5.5 V, V _I = 5.5 V or GND					±1			
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND					3	μA		
ΔI _{CC} [§]	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND					2.5	mA		
C _i	Control inputs	V _I = 3 V or 0					4.5	pF		
C _{io} (OFF)	B port	V _O = 3 V or 0, S0, S1, or S2 = V _{CC}					8.5	pF		
	A port						8			
r _{on} [¶]	A to B or B to A	V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA				14	20	Ω	
		V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA				5		7
				I _I = 30 mA				5		7
			V _I = 2.4 V, I _I = 15 mA				8	15		
	A1 to A2	V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA				22	30		
		V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA				10		14
I _I = 30 mA						10	14			
		V _I = 2.4 V, I _I = 15 mA				16	22			

† Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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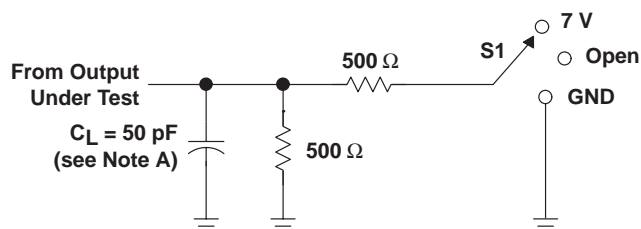
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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^\dagger	A or B	B or A	0.35		0.25		ns
	A1	A2	0.5		0.5		
t_{en}	S	A or B	12.4		3.2	11.1	ns
t_{dis}	S	A or B	12.4		2.3	11.9	ns
t_{en}	S0	A2 and B2	11.5		4	10.9	ns
t_{dis}	S0	A2 and B2	12.8		5.7	12	ns

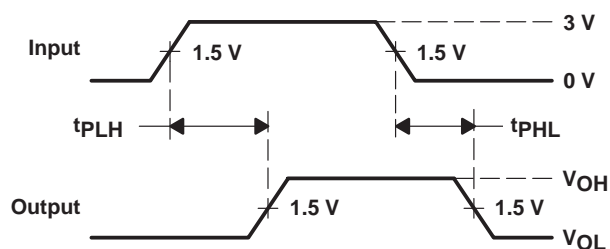
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

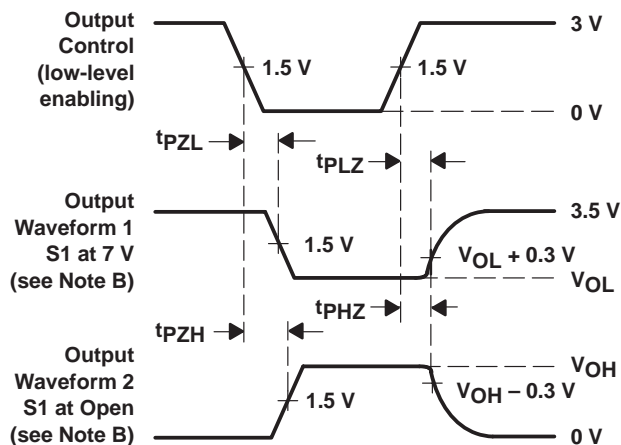


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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