

TC74HCT174AP, TC74HCT174AF, TC74HCT174AFN

HEX D - TYPE FLIP FLOP WITH CLEAR

The TC74HCT174A is a high speed CMOS D - TYPE FLIP FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. When the CLR input is held low, the Q outputs are in the low logic level independent of the other inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

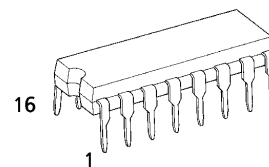
- High Speed..... $f_{MAX} = 56\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{IH} = 2.0\text{V}(\text{Min.})$
 $V_{IL} = 0.8\text{V}(\text{Max.})$
- Wide Interfacing ability..... LSTTL, NMOS, CMOS
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays.... $t_{PLH} \approx t_{PHL}$
- Pin and Function Compatible with 74LS174

TRUTH TABLE

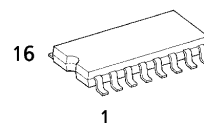
INPUTS			OUTPUT	FUNCTION
CLR	D	CK	Q	
L	X	X	L	CLEAR
H	L	$\uparrow$	L	—
H	H	$\uparrow$	H	—
H	X	$\downarrow$	Q_n	NO CHANGE

X : Don't Care

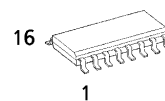
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

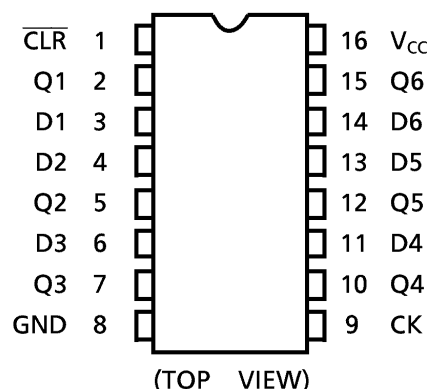


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

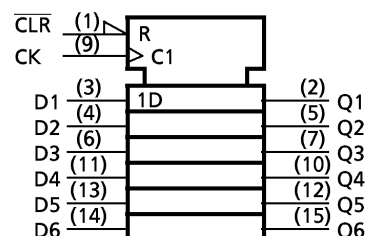


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



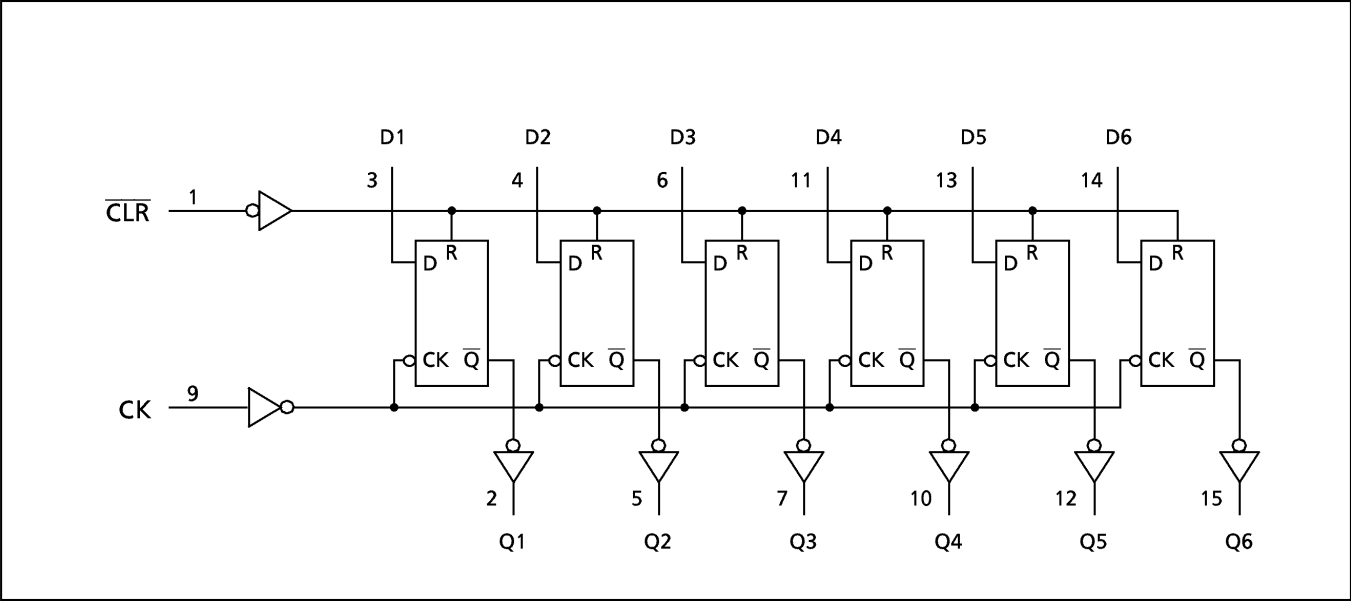
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu A$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu A$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	—	40.0	
	I_C	PER INPUT: $V_{IN} = 0.5V$ or $2.4V$ OTHER INPUT: V_{CC} or GND		5.5	—	—	2.0	—	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
					TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$			4.5	—	15	19	ns
	$t_{W(H)}$			5.5	—	14	18	
Minimum Pulse Width (CLR)	$t_{W(L)}$			4.5	—	15	19	
				5.5	—	14	18	
Minimum Set—up Time	t_s			4.5	—	20	25	
				5.5	—	18	23	
Minimum Hold Time	t_h			4.5	—	5	5	
				5.5	—	5	5	
Minimum Removal Time (CLR)	t_{rem}			4.5	—	10	10	
				5.5	—	10	10	
Clock Frequency	f			4.5	—	30	24	MHz
				5.5	—	33	26	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	12	15	ns
Propagation Delay Time (CK—Q)	t_{PLH} t_{PHL}		—	29	36	
Propagation Delay Time ($\overline{\text{CLR}}$ —Q)	t_{PHL}		—	29	36	
Maximum Clock Frequency	f_{MAX}		32	61	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C				Ta = -40~85°C		UNIT
			VCC(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	tTLH		4.5	—	8	15	—	19	ns
	tTHL		5.5	—	7	14	—	18	
Propagation Delay Time (CK—Q)	tPLH		4.5	—	20	34	—	43	
	tPHL		5.5	—	17	31	—	39	
Propagation Delay Time (CLR—Q)	tPHL		4.5	—	20	34	—	43	
			5.5	—	17	31	—	39	
Maximum Clock Frequency	fMAX		4.5	30	54	—	24	—	MHz
			5.5	33	57	—	26	—	
Input Capacitance	CIN			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	30	—	—	—	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

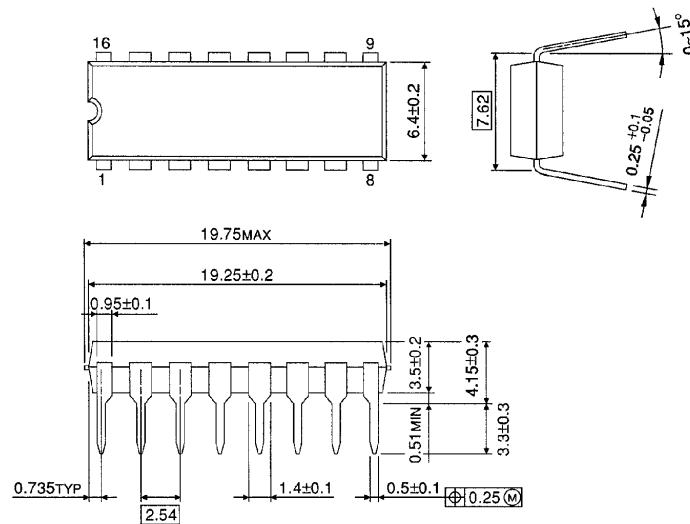
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 18 + 12 \cdot n$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

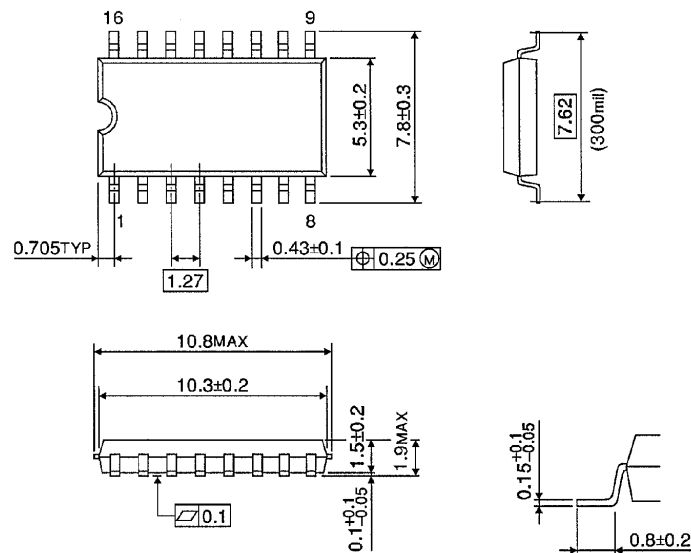
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

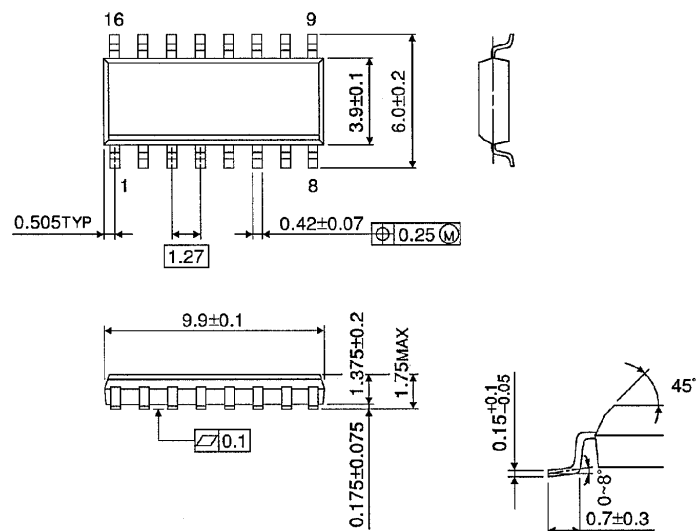


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)