DAVICOM Semiconductor, Inc.

DM9016

10/100 Mbps 3-port Ethernet Switch Controller

with General Processor Interface

DATA SHEET

Preliminary

Version: DM9016--DS-P01

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CONTENT

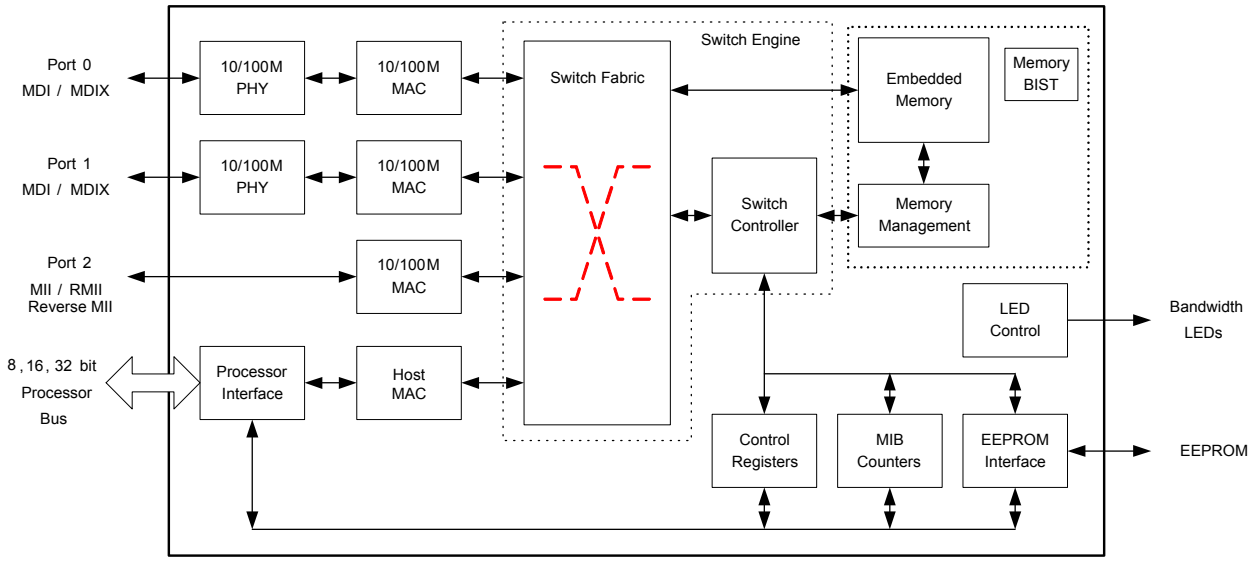
1. General Description

The DM9016 is a fully integrated and cost-effective fast Ethernet switch controller with two ports 10M/100M PHY, one port MII or RMII or Reverse MII interface, and general processor bus interface. The integrated two ports PHY are compliant with IEEE 802.3u standards and support HP Auto-MDIX capabilities for twisted-pair cable transmit/receive direction automatic switching. The MII interface provides the flexibility to connect Ethernet PHY or SoC with MII/RMII interface. The general processor bus can be configured as 8-, 16-, or 32-bit data width.

The DM9016 is a managed Switch, not only provides basic Layer-2 switch functions but offers advanced features that include 802.1Q VLAN, priority queuing management, bandwidth rate control, monitoring port traffic, multicast packet filtering, port security and hardware-based IGMP V1/V2 Snooping, etc.
The general processor bus can be configured as 8-, 16-, or 32-bit data width and interfaces to most embedded CPU. The DM9016 provides TCP/UDP/IPv4 checksum offload function to alleviate host CPU load for improved system performance. The adjustable transmit/receive buffer of processor port can facilitate CPU in processing applications such as Video and Voice streaming. For power management feature, the DM9016 support wake on LAN function via link status change or magic packet detection.

Additionally, the MIB counters, loop-back capability and the memory Build-in Self Test (BIST) are useful for system and board level diagnostic.

2. Block Diagram



3. Features

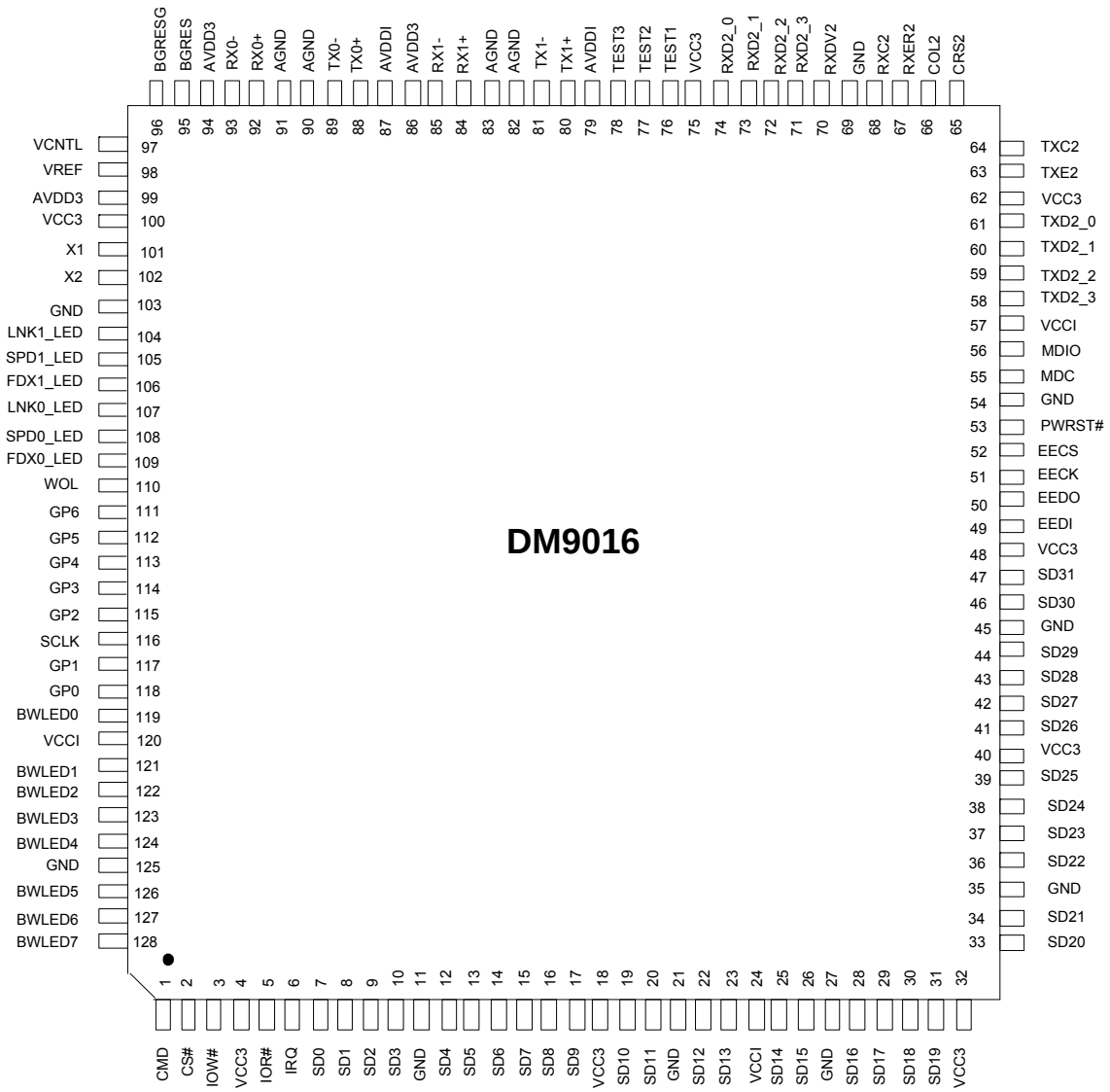
- Ethernet Switch with two 10/100Mb PHY, one MII/RMII/Reverse-MII port, and a flexible 8, 16, or 32-bit general processor bus interface
- Store and Forward switching approach
- Support HP Auto-MDIX
- Support up-to 1K Unicast MAC addresses
- Support IEEE 802.3x Flow Control in Full-duplex mode
- Support Back Pressure Flow Control in Half-duplex mode
- Per port supports ingress or egress bandwidth rate control
- Support Broadcast/Multicast Storm Suppression
- Support maximum packet length up to 1536(default)/1800/2032 bytes
- Support head of Line (HOL) blocking prevention
- Support MIB counters for diagnostic

- General processor bus is slave architecture
- General processor bus driving capability is adjustable
- General processor bus supports TCP/UDP/IPv4 checksum offload
- EEPROM interface for power up configuration
- Support EEPROM 93C46/93C56 with auto-detecting
- Driving capability of TXD/TXE of MII is adjustable

- Per port supports 4 level priority queues by Port-based, 802.1p VLAN, and IP TOS priority. The priority queue can be set at WRR(Weighted Round Robin) or Strictly(High priority queue first)
- Support 802.1Q VLAN up-to 16 VLAN group.
- Support VLAN ID tag/untag options

- MAC Address Table is accessible
- Support 256-entry multicast address table
- Support port security function
- Support 32 entry hardware-based IGMP Snooping V1, V2
- Support IPv6 Multicast Listener Discovery (MLD) Snooping V1
- Support Spanning Tree Protocol
- 128 QFP package with 0.18um technology
- 1.8V internal core, 3.3V I/O with 5V tolerant

4. Pin Configuration :



5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power, PD=internal pull-low (about 50K Ohm)
# = asserted Low

5.1 Processor Bus Interface

Pin No.	Pin Name	I/O	Description
1	CMD	I	Command Type When high, the access of this command cycle is DATA port When low, the access of this command cycle is INDEX port
2	CS#	I	Processor Chip select Command
3	IOW#	I	Processor Write Command
5	IOR#	I	Processor Read Command
6	IRQ	O	Interrupt Request
7,8,9,10,12,13,14,15, 16,17,19,20,22,23,25,26	SD0~15	I/O	Processor Data Bus bit 0~15
28,29,30,31,33,34,36,37, 38,39,41,42,43,44,46,47	SD16~31	I/O	Processor Data Bus bit 16~31 or General purpose pins when data bus is in 16-bit mode
110	WOL	O	Issue a wake up signal when wake up event occurred.

5.2 General and LED pins

Pin No.	Pin Name	I/O	Description
118,117,115,114, 113,112,111	GP0~6	I/O	General I/O Ports Registers GPCR and GPR can program these pins
119,121,122,123, 124,126,127,128	BWLED0~7	I/O	Bandwidth LED

5.3 P2 MII / RMII / Reverse MII Interfaces

5.3.1 MII Interfaces

Pin No.	Pin Name	I/O	Description
55	MDC	O,PD	MII Serial Management Data Clock
56	MDIO	I/O	MII Serial Management Data
58,59,60,61	TXD2_3~0	O,PD	Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2)
63	TXE2	O,PD	Port 2 MII Transmit Enable
64	TXC2	O,PD	Port 2 MII Transmit Clock
65	CRS2	I	Port 2 MII Carrier Sense
66	COL2	I	Port 2 MII Collision Detect
67	RXER2	I	Port 2 MII Receive Error
68	RXC2	I	Port 2 MII Receive Clock
70	RXDV2	I	Port 2 MII Receive Data Valid
71,72,73,74	RXD2_3~0	I	Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2)

5.3.2 RMII Interfaces

Pin No.	Pin Name	I/O	Description
55	MDC	O,PD	MII Serial Management Data Clock
56	MDIO	I/O	MII Serial Management Data
58,59	TXD2_3~0	O,PD	Reserved
60,61	TXD2_1~0	O,PD	RMII Transmit Data
63	TXE2	O,PD	RMII Transmit Enable
64	TXC2	O,PD	Reserved
65	CRS2	I	RMII CRS_DV
66	COL2	I	Reserved, tie to ground in application.
67	RXER2	I	Reserved, tie to ground in application.
68	RXC2	I	50MHz reference clock.
70	RXDV2	I	Reserved, tie to ground in application.
71,72	RXD2_3~2	I	Reserved, tie to ground in application.
73,74	RXD2_3~0	I	RMII Receive Data

5.3.3 Reverse MII Interfaces

Pin No.	Pin Name	I/O	Description
55	MDC	O,PD	Reserved
56	MDIO	I/O	Reserved
58,59,60,61	TXD2_3~0	O,PD	Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2)
63	TXE2	O,PD	Port 2 MII Transmit Enable
64	TXC2	O	25MHz clock output
65	CRS2	O	Port 2 carrier sense output when TXE2 orRXDV2 asserted
66	COL2	O	Port 2 collision output when TXE2 and RXDV2 asserted
67	RXER2	I	Port 2 MII Receive Error
68	RXC2	I	Port 2 MII Receive Clock
70	RXDV2	I	Port 2 MII Receive Data Valid
71,72,73,74	RXD2_3~0	I	Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2)

5.4 EEPROM Interfaces

Pin No.	Pin Name	I/O	Description
49	EEDI	I,PD	EEPROM Data In
50	EEDO	O,PD	EEPROM Data Out This pin is used serially to write op-codes, addresses and data into the EEPROM.
51	EECK	O,PD	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer.
52	EECS	O,PD	EEPROM Chip Selection.

5.5 LED Pins

Pin No.	Pin Name	I/O	Description
104	LNK1_LED	O	Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY1
105	SPD1_LED	O	Port 1 Speed LED Its low output indicates that the internal PHY1 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY1
106	FDX1_LED	O	Port 1 Full-duplex LED Its low output indicates that the internal PHY1 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY1
107	LNK0_LED	O	Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY0
108	SPD0_LED	O	Port 0 Speed LED Its low output indicates that the internal PHY0 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY0
109	FDX0_LED	O	Port 0 Full-duplex LED Its low output indicates that the internal PHY0 is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY0

5.6 Clock Interface

Pin No.	Pin Name	I/O	Description
101	X1	I	Crystal 25MHz In or Oscillator in
102	X2	O	Crystal 25MHz Out
116	SCLK	I	External system clock source

5.7 Network Interface

Pin No.	Pin Name	I/O	Description
80,81	TX1+/-	I/O	Port 1 TP TX
84,85	RX1+/-	I/O	Port 1 TP RX
88,89	TX0+/-	I/O	Port 0 TP TX
92,93	RX0+/-	I/O	Port 0 TP RX
95	BGRES	I/O	Band gap Pin
96	BGGND	P	Band gap Ground
97	VCNTL	I/O	1.8V Voltage control
98	VREF	O	Voltage Reference

5.8 Miscellaneous Pins

Pin No.	Pin Name	I/O	Description
53	PWRST#	I	Power on Reset.
76	TEST1	I,PD	Tie to ground in application
77	TEST2	I,PD	0: 3-port mode All ports are active in this mode. 1: 2-port mode Only 2 ports are active in this mode. Port 1 or port 2 can be disabled by strap TXEN2. In this mode, the disabled port's memory resource is shared by processor port and the other 2 ports.
78	TEST3	I,PD	Tie to ground in application

5.9 Power Pins

Pin No.	Pin Name	I/O	Description
4,18,32,40,48,62,75,100	VCC3	P	Digital 3.3V
24,57,120	VCCI	P	Internal 1.8V core power
11,21,27,35,45, 54,69,103,125	GND	P	Digital GND
86,94,99	AVDD3	P	Analog 3.3V power
79,87	AVDDI	P	Analog 1.8V power
82,83,90,91	AGND	P	Analog GND

5.10 Strap Pins Table

1: pull-high 1K~10K, 0: default floating.

5.10.1 Strap pin in 3-port mode

Pin No.	Pin Name	Description
50 51	EECK EEDO	Processor Data Bus Width EECK EEDO data width 0 0 16-bit (default) 0 1 32-bit 1 0 8-bit 1 1 (reserved)
52	EECS	Source of System Clock 0: system clock is internal 50MHz clock (default) 1: use SCLK pin as system clock
55	MDC	Polarity of IRQ 0: IRQ pin high active (default) 1: IRQ pin low active
58	TXD2_3	ISA pin control 0: GP6/5 as normal usage (default) 1: GP6 as IO16, GP5 as IOWAIT
59	TXD2_2	Port 2 force mode 0: Port 2 status from external PHY (N-way) 1: Port 2 in force mode
60 61	TXD2_1 TXD2_0	Port 2 mode TXD2_1, TXD2_0 0 0 Port 2 is MII mode (default) 0 1 Port 2 is Reverse-MII mode 1 0 Port 2 is RMII mode 1 1 Reserved
63	TXEN2	Output Type of IRQ 0: IRQ pin is force output (default) 1: IRQ pin is open-collect
115	GP2	Port 2 Force mode Speed is: (when TXD2_2 pulled high) 0: 100Mbps 1: 10Mbps
114	GP3	Port 2 Force mode Duplex is : (when TXD2_2 pulled high) 0: full-duplex 1: half-duplex
113	GP4	Port 2 Force mode Link is: (when TXD2_2 pulled high) 0: link 1: non-link

5.10.2 Strap pin in 2-port mode

Pin No.	Pin Name	Description
50 51	EECK EEDO	Processor Data Bus Width EECK EEDO data width 0 0 16-bit (default) 0 1 32-bit 1 0 8-bit 1 1 (reserved)
52	EECS	Source of System Clock 0: system clock is internal 50MHz clock (default) 1: use SCLK pin as system clock
55	MDC	Polarity of IRQ 0: IRQ pin high active (default) 1: IRQ pin low active
58	TXD2_3	ISA pin control 0: GP6/5 as normal usage (default) 1: GP6 as IO16, GP5 as IOWAIT
59	TXD2_2	Port 2 force mode 0: Port 2 status from external PHY (N-way) 1: Port 2 in force mode
60 61	TXD2_1 TXD2_0	Port 2 mode TXD2_1, TXD2_0 0 0 Port 2 is MII mode (default) 0 1 Port 2 is Reverse-MII mode 1 0 Port 2 is RMII mode 1 1 (reserved)
63	TXEN2	Disabled Port Selection 0: Port 2 is disabled (default) 1: Port 1 is disabled
115	GP2	Port 2 Force mode Speed is: (when TXD2_2 pulled high) 0: 100Mbps 1: 10Mbps
114	GP3	Port 2 Force mode Duplex is : (when TXD2_2 pulled high) 0: full-duplex 1: half-duplex
113	GP4	Port 2 Force mode Link is: (when TXD2_2 pulled high) 0: link 1: non-link

6. Control and Status Register Set

The DM9016 implements several control and status registers (Register is 8 bit width), which can be accessed by the host. All CSRs are set to their default values by power-on or hardware or software reset unless specified

Register	Description	Offset	Default value after reset
NCR	Network Control Register	00H	00H
NSR	Network Status Register	01H	00H
TCR	TX Control Register	02H	00H
RCR	RX Control Register	05H	00H
RSR	RX Status Register	06H	00H
ROCR	Receive Overflow Counter Register	07H	00H
FCR	Flow Control Register	0AH	00H
EPCR	EEPROM & PHY Control Register	0BH	00H
EPAR	EEPROM & PHY Address Register	0CH	40H
EPDRL	EEPROM & PHY Low Byte Data Register	0DH	XXH
EPDRH	EEPROM & PHY High Byte Data Register	0EH	XXH
WUCR	Wake Up Control Register (0FH)	0FH	00H
PAR	Processor Port Physical Address Registers	10H-15H	by EEPROM
MAR	Processor Port Multicast Address Registers	16H-1DH	XXH
GPCR	General Purpose Control Register	1EH	01H
GPR	General Purpose Register	1FH	XXH
RXPLLR	RX Packet Length Low Register	20H	00H
RXPLHR	RX Packet Length High Register	21H	00H
RASR	RX Additional Status Register	26H	00H
RACR	RX Additional Control Register	27H	00H
VID	Vendor ID	28H-29H	0A46H
PID	Product ID	2AH-2BH	9016H
CHIPR	CHIP Revision	2CH	02H
TCSCR	Transmit Check Sum Control Register	31H	00H
RCSCSR	Receive Check Sum Control Status Register	32H	00H
GPCR2	General Purpose Control Register 2	34H	00H
GPR2	General Purpose Register 2	35H	00H
GPCR3	General Purpose Control Register 3	36H	00H
GPR3	General Purpose Register 3	37H	00H
DRIVER	uP Data Bus driving capability Register	38H	21H
IRQCR	IRQ Control Register	39H	00H
P2FRV	Port 2 driving capability Register	3AH	21H
TXBSCR	TX Block Size Control Register	3FH	20H
MONIR1	Monitor Register 1	40H	XXH
MONIR2	Monitor Register 2	41H	XXH
MONIR3	Monitor Register 3	42H	XXH
SWITCHCR	SWITCH Control Register	52H	00H
VLANCR	VLAN Control Register	53H	00H
SWITCHSR	SWITCH Status Register	54H	00H
BWLED	Bandwidth LED Control Register	55H	FFH
DSP1,2	DSP Control Register I,II	58H~59H	0000H
P_INDEX	Per Port Control/Status Index Register	60H	00H

P_CTRL	Per Port Control Data Register	61H	00H
P_STUS	Per Port Status Data Register	62H	00H
P_RATE	Per Port Ingress and Egress Rate Control Register	66H	00H
P_BW	Bandwidth Control Register	67H	00H
P_UNICAST	Per Port Block Unicast ports Control Register	68H	00H
P_MULTI	Per Port Block Multicast ports Control Register	69H	00H
P_BCAST	Per Port Block Broadcast ports Control Register	6AH	00H
P_UNKNWN	Per Port Block Unknown ports Control Register	6BH	00H
P_SSTP	Per Port Security & STP Register	6CH	00H
P_PRI	Per Port Priority Queue Control Register	6DH	00H
VLAN_TAGL	Per Port VLAN Tag Low Byte Register	6EH	01H
VLAN_TAGH	Per Port VLAN Tag High Byte Register	6FH	00H
EACSR_1	Ethernet Address Control / Status Register 1	70H	00H
EAD0	MAC Address bit 07~00	71H	00H
EAD1	MAC Address bit 15~08	72H	00H
EAD2	MAC Address bit 23~16	73H	00H
EAD3	MAC Address bit 31~24	74H	00H
EAD4	MAC Address bit 39~32	75H	00H
EAD5	MAC Address bit 47~40	76H	00H
EACSR_2	Ethernet Address Control / Status Register 2 (77H)	77H	00H
SCR_1	Snooping Control Register 1 (78H)	78H	00H
SCR_2	Snooping Control Register 2 (79H)	79H	00H
SCR_3	Snooping Control Register 3 (7AH)	7AH	00H
SCR_4	Snooping Control Register 4 (7BH)	7BH	02H
SCR_5	Snooping Control Register 5 (7CH)	7CH	00H
P_MIB_IDX	Per Port MIB counter Index Register	80H	00H
MIB_DAT	MIB counter Data Register bit 0~7	81H	00H
MIB_DAT	MIB counter Data Register bit 8~15	82H	00H
MIB_DAT	MIB counter Data Register bit 16~23	83H	00H
MIB_DAT	MIB counter Data Register bit 24~31	84H	00H
P_RX_LEN	Per Port RX Packet Length Control Register	88H	00H
PVLAN	Port-based VLAN mapping table registers	B0-BFH	0FH
TOS_MAP	TOS Priority Map Register	C0-CFH	00H~FFH
VLAN_MAP	VLAN priority Map Register	D0-D1H	50H,FAH
MRCMDX	Memory Data Pre-Fetch Read Command Without Address Increment Register	F0H	XXH
MRCMD	Memory Data Read Command With Address Increment Register	F2H	XXH
MRRL	Memory Data Read address Register Low Byte	F4H	00H
MRRH	Memory Data Read address Register High Byte	F5H	00H
MWCMDX	Memory Data Write Command Without Address Increment Register	F6H	XXH
MWCMD	Memory Data Write Command With Address Increment Register	F8H	XXH
MWRL	Memory Data Write address Register Low Byte	FAH	00H
MWRH	Memory Data Write address Register High Byte	FBH	00H
TXPLL	TX Packet Length Low Byte Register	FCH	XXH
TXPLH	TX Packet Length High Byte Register	FDH	XXH
ISR	Interrupt Status Register	FEH	00H

IMR	Interrupt Mask Register	FFH	00H

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where:
<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value

P = power on reset default value
H = hardware reset command default value
S = software reset default value
E = default value from EEPROM
T = default value from strap pin
<Access Type>:
RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1=Read/Write and Cleared by write 1
WO = Write only
Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

6.1 Network Control Register (00H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	WAKEEN	PH0,WO	Wakeup Event Enable When set, it enables the wakeup function. Clearing this bit will also clear all wakeup event status This bit will not be affected after a software reset
5	CLR1	PH0,RW	0: REG. 01H auto-cleared after read 1: REG. 01H cleared by writing 1 to respected bit.
4:2	RESERVED	0,RO	Reserved
1	LBK	PH0, RW	Loopback Test Mode
0	RST	PH0,RW	Software reset and auto clear after 10us

6.2 Network Status Register (01H)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	LINK_X_ST	PH0, W/C1	Link Change Status. This bit is set after port 0 or 1 link changed. This bit is cleared by write 1
4	RESERVED	0,RO	Reserved
3	TX2END	PHS0, RW/C1	TX Packet 2 Complete Status. This bit is set after transmit completion of packet index 2 If bit 5 of NCR is set, this bit is cleared by write 1; Otherwise it can be cleared by read or write 1.
2	TX1END	PHS0, RW/C1	TX Packet 1 Complete status. This bit is set after transmit completion of packet index 1 If bit 5 of NCR is set, this bit is cleared by write 1; Otherwise it can be cleared by read or write 1.
1:0	RESERVED	0,RO	Reserved

6.3 TX Control Register (02H)

Bit	Name	Default	Description
7:4	RESERVED	0,RO	Reserved
3	CRC_DIS2	PHS0,RW	CRC Appends Disable for Packet Index 2
2	RESERVED	0,RO	Reserved
1	CRC_DIS1	PHS0,RW	CRC Appends Disable for Packet Index 1
0	TXREQ	PHS0,RW	TX Request. Auto clears after transmit completely

6.4 RX Control Register (05H)

Bit	Name	Default	Description
7	HASHALL	PHS0,RW	Filter All address in Hash Table
6	RESERVED	PHS0,RW	Reserved
5	RESERVED	PHS0,RW	Reserved
4	DIS_CRC	PHS0,RW	Discard CRC Error Packet
3	ALL	PHS0,RW	Pass All Multicast Packets
2	RESERVED	PHS0,RW	Reserved
1	PRMSC	PHS0,RW	Promiscuous Mode
0	RXEN	PHS0,RW	RX Enable

6.5 RX Status Register (06H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	MF	0,RO	Multicast Frame
5:4	PKT_TYPE	0,RO	Received Frame Type 00: Reserved 01: IGMP packet 10: MLD packet 11: BPDU packet
3:2	SRCP	0,RO	Source Port Number
1	CE	0,RO	CRC Error
0	FOE	0,RO	FIFO Overflow Error

6.6 Receive Overflow Counter Register (07H)

Bit	Name	Default	Description
7	RXFU	PHS0,R/C	Receive Overflow Counter Overflow This bit is set when the ROC has an overflow condition
6:0	ROC	PHS0,R/C	Receive Overflow Counter This is a statistic counter to indicate the received packet count upon FIFO overflow

6.7 Flow Control Register (0AH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	FLOW_EN	PHS0,RW	RX Flow Control Enable Enables the pause packet for high/low water threshold control
4:0	RESERVED	0,RO	Reserved

6.8 EEPROM & PHY Control Register (0BH)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	EETYPE	0,RO	EEPROM Type 0: 93C46 1: 93C56
5	REEP	PH0,RW	Reload EEPROM. Note: Driver needs to clear it up after the operation completes
4	WEP	PH0,RW	Write EEPROM Enable
3	EPOS	PH0,RW	EEPROM or PHY Operation Select When reset, select EEPROM; when set, select PHY
2	ERPRR	PH0,RW	EEPROM Read or PHY Register Read Command. Note:: Driver needs to clear it up after the operation completes.
1	ERPRW	PH0,RW	EEPROM Write or PHY Register Write Command. Note:: Driver needs to clear it up after the operation completes.
0	ERRE	PH0,RO	EEPROM Access Status or PHY Access Status When set, it indicates that the EEPROM or PHY access is in progress

6.9 EEPROM & PHY Address Register (0CH)

Bit	Name	Default	Description
7:6	PHY_ADR	PH01,RW	PHY Address bit 1 and 0; the PHY address bit [4:2] is force to 0.
5:0	EROA	PH0,RW	EEPROM Word Address or PHY Register Address

6.10 EPROM & PHY Data Register (0DH~0EH)

Bit	Name	Default	Description
7:0	EE_PHY_L	PH0,RW	EEPROM or PHY Low Byte Data (0DH) This data is made to write low byte of word address defined in Reg. CH to EEPROM or PHY
7:0	EE_PHY_H	PH0,RW	EEPROM or PHY High Byte Data (0EH) This data is made to write high byte of word address defined in Reg. CH to EEPROM or PHY

6.11 Wake Up Control Register (0FH)

Bit	Name	Type	Description
7:6	RESERVED	0,RO	Reserved
5	LINKEN	PHE0,RW	Link Change Event Enable When set, it enables Link Status Change Wake up Event
4	RESERVED	0,RO	Reserved
3	MAGICEN	PHE0,RW	Magic Packet Event Enable When set, it enables Magic Packet Wake up Event
2	LINKST	PH0,RO	Link Change Event Status When set, it indicates that Link Status Change Event (link of port 0 or 1) occurred This bit can be cleared by write 1 to bit 5 of NSR or write 0 to bit 6 of NCR.
1	RESERVED	0,RO	Reserved
0	MAGICST	PH0,RO	Magic Packet Event Status When set, indicates the Magic Packet is received and Magic packet Event occurred. This bit can be cleared by write 1 to bit 5 of NSR or write 0 to bit 6 of NCR.

6.12 Physical Address Register (10H~15H)

Bit	Name	Default	Description
7:0	PAB5	E,RW	Physical Address Byte 5 (15H)
7:0	PAB4	E,RW	Physical Address Byte 4 (14H)
7:0	PAB3	E,RW	Physical Address Byte 3 (13H)
7:0	PAB2	E,RW	Physical Address Byte 2 (12H)
7:0	PAB1	E,RW	Physical Address Byte 1 (11H)
7:0	PAB0	E,RW	Physical Address Byte 0 (10H)

6.13 Multicast Address Register (16H~1DH)

Bit	Name	Default	Description
7:0	MAB7	X,RW	Multicast Address Byte 7 (1DH)
7:0	MAB6	X,RW	Multicast Address Byte 6 (1CH)
7:0	MAB5	X,RW	Multicast Address Byte 5 (1BH)
7:0	MAB4	X,RW	Multicast Address Byte 4 (1AH)
7:0	MAB3	X,RW	Multicast Address Byte 3 (19H)
7:0	MAB2	X,RW	Multicast Address Byte 2 (18H)
7:0	MAB1	X,RW	Multicast Address Byte 1 (17H)
7:0	MAB0	X,RW	Multicast Address Byte 0 (16H)

6.14 General Purpose Control Register (1EH)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:0	GPC	PH,0,RW	General Purpose Control 6~0 Define the input/output direction of pins GP6~0 respectively. 1: output, 0:input

6.15 General Purpose Register (1FH)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:0	GEPIO	X,RW	General Purpose Data 6~0 These bits are reflect to pin GP6~0 respectively.

6.16 RX Packet Length Low Register (20H)

Bit	Name	Default	Description
7:0	RXPLL	PH,RO	RX Packet Length Low Byte

6.17 RX Packet Length High Register (21H)

Bit	Name	Default	Description
7:0	RXPLH	PH,RO	RX Packet Length High Byte

6.18 RX Additional Status Register (26H)

Bit	Name	Default	Description
7:4	RESERVED	0,RO	Reserved
1:0	RPTRS	PH,RO	uP Received Pointer Status Only available when RX pointer restriction is enabled (Reg27h.7=0). 00: Within buffer 01: End of buffer 1x: Exceed buffer

6.19 RX Additional Control Register (27H)

Bit	Name	Default	Description
7	RPRD	PHS0,RW	RX Pointer Restriction Disable
6:0	RESERVED	0,RO	Reserved

6.20 Vendor ID Register (28H~29H)

Bit	Name	Default	Description
7:0	VIDH	PE,0AH,RO	Vendor ID High Byte (29H)
7:0	VIDL	PE,46H.RO	Vendor ID Low Byte (28H)

6.21 Product ID Register (2AH~2BH)

Bit	Name	Default	Description
7:0	PIDH	PE,90H,RO	Product ID High Byte (2BH)
7:0	PIDL	PE,16H.RO	Product ID Low Byte (2AH)

6.22 Chip Revision Register (2CH)

Bit	Name	Default	Description
7:0	CHIPR	P02H,RO	CHIP Revision

6.23 Transmit Check Sum Control Register (31H)

Bit	Name	Default	Description
7~3	RESERVED	0,RO	Reserved
2	UDPCSE	HP0,RW	UDP Checksum Generation Enable
1	TCPCSE	HP0,RW	TCP Checksum Generation Enable
0	IPCSE	HP0,RW	IP Checksum Generation Enable

6.24 Receive Check Sum Control Status Register (32H)

Bit	Name	Default	Description
7	UDPS	HP0,RO	UDP Checksum Status 1: if UDP packet checksum fail
6	TCPS	HP0,RO	TCP Checksum Status 1: if TCP packet checksum fail
5	IPS	HP0,RO	IP Checksum Status 1: if IP packet checksum fail
4	UDPP	HP0,RO	This is a UDP Packet
3	TCPP	HP0,RO	This is a TCP Packet
2	IPP	HP0,RO	This is a IP Packet
1	RCSEN	HPS0,RW	Receive Checksum Checking Enable When set, the checksum status will store in packet first byte of status header.
0	DCSE	HPS0,RW	Discard Checksum Error Packet When set, if IP/TCP/UDP checksum field is error, this packet will be discarded.

6.25 General Purpose Control Register 2 (34H)

Bit	Name	Default	Description
7~0	GPC2	HP0,RW	General Purpose Control 2 Define the input/output direction of pins SD23~16, which are used as general purpose pins when none 32-bit mode and external MII mode, respectively.

6.26 General Purpose Register 2 (35H)

Bit	Name	Default	Description
7~0	GPD2	HP0,RW	General Purpose Register 2 Data When the correspondent bit of General Purpose Control Register 2 is set, the value of the bit is reflected to pin SD23~16 When the correspondent bit of General Purpose Control Register 2 is 0, the value of the bit to be read is reflected from correspondent pins SD23~16

6.27 General Purpose Control Register 3 (36H)

Bit	Name	Default	Description
7~0	GPC3	HP0,RW	General Purpose Control 3 Define the input/output direction of pins SD31~24, which are used as general purpose pins when none 32-bit mode and external MII mode, respectively.

6.28 General Purpose Register 3 (37H)

Bit	Name	Default	Description
7~0	GPD3	HP0,RW	General Purpose Register 3 Data When the correspondent bit of General Purpose Control Register 3 is set, the value of the bit is reflected to pin SD31~24 When the correspondent bit of General Purpose Control Register 3 is 0, the value of the bit to be read is reflected from correspondent pins SD31~24

6.29 Processor Data Bus Driving Capability Register (38H)

Bit	Name	Default	Description
7	RESERVED	0,RW	Reserved
6:5	ISA_CURR	P01,RW	SD Bus Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
4:3	Reserved	P0,RW	Reserved
2	STEP	P0,RW	Data Bus Output stepping 1: disabled 0: enabled
1	IOW_SPIKE	P0,RW	Eliminate IOW spike 0: Disable 1: Eliminate about 2ns IOW spike
0	IOR_SPIKE	P1,RW	Eliminate IOR spike 0: Disable 1: Eliminate about 2ns IOR spike

6.30 IRQ Pin Control Register (39H)

Bit	Name	Default	Description
7:5	IRQ_DELAY	PS0,RW	IRQ Delayed Output Interval This field determines the IRQ delayed output interval in multiples of 40 milliseconds(ms)
1	IRQ_TYPE	PET0,RW	IRQ Pin Output Type Control 1: IRQ open-collector output 0: IRQ direct output
0	IRQ_POL	PET0,RW	IRQ Pin Polarity Control 1: IRQ active low 0: IRQ active high

6.31 Port 2 Driving Capability Register (3AH)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:5	P2_CURR	P01,RW	Port 2 TXD/TXE Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA
4:0	RESERVED	0,RW	Reserved

6.32 RX Control Register 2 (3CH)

Bit	Name	Default	Description
7:2	Reserved	PS0,RO	Reserved
1	DIS_BCAST	PH0,RW	Abort broadcast packet if its size > 256 bytes
0	NEXT_RX	PH0,RW	Jump to Next Start of Receiving Packet Write 1 to launch and clear automatically after 10ns.

6.33 TX Block Size Control Register (3FH)

Bit	Name	Default	Description
7:6	Reserved	PS0,RO	Reserved
5:0	TX_SIZE	P20h,RW	TX Block Size in 2-Port Mode This value defines the transmit block size in 256-byte unit. TX memory size = TX_SIZE * 256 bytes And then RX memory size = 16KB – (TX_SIZE + 1)*256-Byte Note: The value of TX_SIZE should be between 14H and 30H

6.34 Monitor Register 1 (40H)

Bit	Name	Default	Description
7	BWIDTH	T0,RO	8-bit Data Strap Latch Status
6	DWIDTH	T0,RO	32-bit Data Strap Latch Status
5	IRQOC	ET0,RO	IRQ Open-Collect Pin Status
4	IRQP	ET0,RO	IRQ Polarity Pin Status
3:0	RESERVED	0,RO	Reserved

6.35 Monitor Register 2 (41H)

Bit	Name	Default	Description
7	TEST3	RO	TEST3 pin
6	TEST2	RO	TEST2 pin
5	TEST1	RO	TEST1 pin
4	MDC	T0,RO	MDC Strap Status
3	EECS	T0,RO	EECS Strap Status
2	EECK	T0,RO	EECK Strap Status
1	EEDO	T0,RO	EEDO Strap Status
0	EEDI	T0,RO	EEDI Strap Status

6.36 Monitor Register 3 (42H)

Bit	Name	Default	Description
7:4	RESERVED	0,RO	Reserved
4	TXE2	T0,RO	TXE2 Strap Status
3	TXD2_3	T0,RO	TXD2_3 Strap Status
2	TXD2_2	T0,RO	TXD2_2 Strap Status
1	TXD2_1	T0,RO	TXD2_1 Strap Status
0	TXD2_0	T0,RO	TXD2_0 Strap Status

6.37 Monitor Register 4 (43H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:0	GPIO	T0,RO	GPIO 0~6 Strap Status

6.38 Switch Control Register (52H)

Bit	Name	Default	Description
7	MEM_BIST	PH0,RO	Address Memory Test BIST Status 0: OK 1: Fail
6	RST_SW	P0,RW	Reset Switch Core Write 1 to launch and clear automatically after 10us.
5	RST_ANLG	P0,RW	Reset Analog PHY Core Write 1 to launch and clear automatically after 10us.
4:3	SNF_PORT	PHE00,RW	Sniffer Port Number
2	CRC_DIS	PHE0,RW	Switch CRC Checking Disable
1:0	RESERVED	0,RO	Reserved

6.39 VLAN Control Register (53H)

Bit	Name	Default	Description
7	TOS6	PHE0,RW	Full ToS Using Enable 0: check most significant 3-bit only of TOS 1: check most significant 6-bit of TOS
6	RESERVED	0,RO	Reserved
5	UNICAST	PHE0,RW	Unicast Packet Can Across VLAN Boundary
4	VIDFFF	PHE0,RW	Replace VID FFF
3	VID1	PHE0,RW	Replace VID 001
2	VID0	PHE0,RW	Replace VID 000
1	PRI	PHE0,RW	Replace Priority Field in The Tag
0	VLAN	PHE0,RW	VLAN Mode Enable 0: port-base VLAN 1: 802.1Q base VLAN mode enable

6.41 Bandwidth LED Control Register (55H)

Bit	Name	Default	Description
7,6	RESERVED	PH0,RW	Reserved
5	P2_TX	PH1,RW	Port 2 transmit as event of bandwidth LED source
4	P2_RX	PH0,RW	Port 2 receive as event of bandwidth LED source
3	P1_TX	PH1,RW	Port 1 transmit as event of bandwidth LED source
2	P1_RX	PH0,RW	Port 1 receive as event of bandwidth LED source
1	P0_TX	PH1,RW	Port 0 transmit as event of bandwidth LED source
0	P0_RX	PH0,RW	Port 0 receive as event of bandwidth LED source

6.42 STP Control Register (56H)

Bit	**Name**	**Default**	**Description**
7:1	RESERVED	0,RO	Reserved
0	STPEN	PS0,RW	Spanning Tree Protocol Enabled

6.43 DSP PHY Control Register (58H~59H)

58H:

Bit	Name	Default	Description
7:0	DSP_CTL1	PH0,RW	DSP Control Register 1 for testing only (register 58H)

59H:

Bit	Name	Default	Description
7:0	DSP_CTL2	PH0,RW	DSP Control Register 2 for testing only (register 59H)

6.44 Per Port Control/Status Index Register (60H)

Bit	Name	Default	Description
7:5	RESERVED	PHS0,RW	Reserved
4:2	RESERVED	0,RO	Reserved
1:0	INDEX	PHS0,RW	Port index for register 61h~84h Write the port number to this register before write/read register 61h~84h.

6.45 Per Port Control Data Register (61H)

Bit	Name	Default	Description
7	FAST_LEV	PHE0,RW	IGMP Snooping Fast Leave Enable
6	PARTI_EN	PHE0,RW	Enable Partition Detection
5	NO_DIS_RX	PHE0,RW	Don't Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control.
4	FLOW_DIS	PHE0,RW	Flow control in full duplex mode, or back pressure in half duplex mode enable 0: enable 1: disable
3	BANDWIDTH	PHE0,RW	Bandwidth Control 0: Control with Ingress and Egress separately, ref to Register 66H. 1: Control with Ingress or Egress, ref to Register 67H
2	BP_DIS	PHE0,RW	Broadcast packet filter 0: accept broadcast packets 1: reject broadcast packets
1	MP_DIS	PHE0,RW	Multicast packet filter 0: accept multicast packets 1: reject multicast packets
0	MP_STORM	PE0,RW	Broadcast Storm Control 0: only broadcast packets storm are controlled 1: multicast packets also same as broadcast storm control.

6.46 Per Port Status Data Register (62H)

Bit	Name	Default	Description
7:6	RESERVED	P0,RO	Reserved
5	LP_FCS	P0,RO	Link Partner Flow Control Enable Status
4	BIST	P0,RO	BIST status 0: SRAM BIST pass 1: SRAM BIST fail
3	RESERVED	0,RO	Reserved
2	SPEED2	P0,RO	Speed Status 0: 10Mbps, 1:100Mbps
1	FDX2	P0,RO	Duplex Status 0: half-duplex, 1: full-duplex
0	LINK2	P0,RO	Link Status 0: not Link status, 1: Link status

6.47 Per Port Forward Control Register (65H)

Bit	Name	Default	Description
7	LOOPBACK	PHE0,RW	Loop-back Mode
6	MONI_TX	PHE0,RW	TX Packet Monitored
5	MONI_RX	PHE0,RW	RX Packet Monitored
4	DIS_BMP	PHE0,RW	Broad/Multicast packet do not monitored
3	RESERVED	PH0,RW	Reserved
2	TX_DIS	PHE0,RW	Packet Transmit Disabled
1	RX_DIS	PHE0,RW	Packet Receive Disabled
0	ADR_DIS	PHE0,RW	Address Learning Disabled

6.48 Per Port Ingress/Egress Control Register (66H)

Bit	Name	Default	Description
7:4	INGRESS	PHE0,RW	Ingress Rate Control 0000: none 0001: 64K 0010: 128K 0011: 256K 0100: 512K 0101: 1M 0110: 2M 0111: 4M 1000: 8M 1001: 16M 1010: 32M 1011: 48M 1100: 64M 1101: 72M 1110: 80M 1111: 88M
3:0	EGRESS	PHE0,RW	Egress Rate Control 0000: none 0001: 64K 0010: 128K 0011: 256K 0100: 512K 0101: 1M 0110: 2M 0111: 4M 1000: 8M 1001: 16M 1010: 32M 1011: 48M 1100: 64M 1101: 72M 1110: 80M 1111: 88M

6.49 Bandwidth Control Setting Register (67H)

Bit	Name	Default	Description
7:4	BSTH	PHE0,RW	Broadcast Storm Threshold 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control
3:0	BW CTRL	PHE0,RW	Received packet length counted. Bandwidth table below. 0000: none 0001: 64K 0010: 128K 0011: 256K 0100: 512K 0101: 1M 0110: 2M 0111: 4M 1000: 8M 1001: 16M 1010: 32M 1011: 48M 1100: 64M 1101: 72M 1110: 80M 1111: 88M

6.50 Per Port Block Unicast ports Control Register (68H)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_UP	PH0,RW	Ports of unicast packet be blocked

6.51 Per Port Block Multicast ports Control Register (69H)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_MP	PH0,RW	Ports of multicast packet be blocked

6.52 Per Port Block Broadcast ports Control Register (6AH)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_BP	PH0,RW	Ports of broadcast packet be blocked

6.53 Per Port Block Unknown ports Control Register (6BH)

Bit	Name	Default	Description
7:4	RESERVED	PH0,RW	Reserved
3:0	BLK_UKP	PH0,RW	Ports of unknown packet be blocked

6.54 Per Port Security & STP Register (6CH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5:4	STPS	PH0,RW	Spanning Tree Port State There are 4 port state for supporting Spanning Tree Protocol 00: Forwarding State, The port transmits and receives packets normally & learning is enabled. 01: Disabled State, The port will not transmit and receive any packets & learning is disabled. 10: Learning State, The port will only forward the packets that are to and from uP port (span packets) & leaning is enabled. 11: Blocking/Listening State, The port will only forward the packets that are to and from uP port (span packets) & leaning is disabled.
3	RESERVED	0,RO	Reserved
2	PS_UNK	PH0,RW	Unknown source address handling when port security is enabled 0: Discard unknown source address (Default) 1: Forward unknown source address to uP Port
1:0	PS_EN	PH0,RW	Port Security Enable 00: Port Security Disable (Default) 01: First Lock 10: First Link Lock 11: Assign Lock

6.55 Per Port Priority Queue Control Register (6DH)

Bit	Name	Default	Description
7	TAG_OUT	PHE0,RW	Output Packet Tagging Enable
6	PRI_DIS	PHE0,RW	Priority Queue Disable
5	WFQUE	PHE0,RW	8:4:2:1 0: queue 3 > 2 > 1 > 0, means queue 3 always high priority 1: 8:4:2:1, means queue 3 has weighting 8, queue 2 has weighting 4, etc
4	TOS_PRI	PHE0,RW	Priority ToS over VLAN
3	TOS_OFF	PHE0,RW	ToS Priority Classification Disable
2	PRI_OFF	PHE0,RW	802.1 p Priority Classification Disable
1:0	P_PRI	PHE0,RW	Port Base priority 00= queue 0 01=queue 1 10=queue 2 11=queue 3

6.56 Per Port VLAN Tag Low Byte Register (6EH)

Bit	Name	Default	Description
7:0	VID70	PHE01,RW	VID[7:0]

6.57 Per Port VLAN Tag High Byte Register (6FH)

Bit	Name	Default	Description
7:5	PRI	PHE0,RW	Tag [15:13]
4	CFI	PHE0,RW	Tag[12]
3:0	VID118	PHE0,RW	VID[11:8]

6.58 Ethernet Address Control / Status Register 1 (70H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:5	EACS	P0,RO	Status of Ethernet Address Command 00: Command OK, Entry Non-exist a. Create an new entry when command is write b. Do nothing when command is delete c. Entry not found when command is search d. Entry is invalid when command is read 01: Command OK, Entry Exist a. Overwrite the entry when command is write b. Delete entry when command is delete c. Entry found when command is search d. Entry is valid when command is read 1X: Command Error
4:3	EAI	PHY,RW	Ethernet Address Table Index 00: Unicast Address Table 01: Multicast Address Table 10: IGMP Table (Read Only) 11: Reserved
2:1	EAC	PH0,RW	Ethernet Address Command 00: Read 01: Write 10: Delete 11: Search
0	EAS	P0,RO	Ethernet Address Table Status 0: Available 1: Busy

6.59 Ethernet Address Data Register (71H~76H)

Bit	Name	Default	Description
7:0	EAD0	PH0,RW	MAC Address bit 07~00 (71H)
7:0	EAD1	PH0,RW	MAC Address bit 15~08 (72H)
7:0	EAD2	PH0,RW	MAC Address bit 23~16 (73H)
7:0	EAD3	PH0,RW	MAC Address bit 31~24 (74H)
7:0	EAD4	PH0,RW	MAC Address bit 39~32 (75H)
7:0	EAD5	PH0,RW	MAC Address bit 47~40 (76H)

6.60 Ethernet Address Control / Status Register 2 (77H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	OVERRIDE	PH0,RW	When writing table, this bit can set the entry to override the port's setting in the receiving disable state of STP. When reading table, it indicates the entry is override one or not. This bit supports unicast and multicast address table both. 0: Entry is normal one. 1: Entry is override one.
5	IGMPE	PH0,RO	When reading multicast address table, this bit indicated the entry is IGMP entry or not. 0: Non-IGMP entry 1: IGMP entry
4	EA_STATIC	PH0,RW	When writing unicast address table, this bit can be used to set the entry as static or dynamic. When reading unicast address table, it indicates the entry is static or dynamic. 0: Entry is dynamic. 1: Entry is static, never be age-out
3:0	PORT	PH0,RW	Forwarding Port Number (0~3), when access Unicast Address Table. Forwarding Port Mapping {uP, P2, P1, P0}, when access Multicast Address Table.

6.61 Snooping Control Register 1 (78H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:5	UIPMPC	PH0,RW	Unregistered IP Multicast Packet Control The IP multicast packet with a destination address which does not match any of groups announced in earlier IGMP Membership Reports, i.e. not found in the IGMP membership table. 00: As normal multicast packets 01: Dropped. 10: Force forward to processor port. 11: Forward to all ports except incoming & uP port.
4	UD_IGR	PH0,RW	User-defined IGMP Router Port Configuration Enable 0: Disable, the router portmap is automatic manipulation via IGMP snooping. 1: Enable, the router portmap is static defined by user.
3	SIGS2UP	PH0,RW	IGMP Packet Forward to uP Port only when Software-IGS
2	HIGS2UP	PH0,RW	IGMP Packet Forward to uP Port also when Hardware-IGS 0: IGMP packet doesn't forwards to processor port when Hardware based IGMP Snooping is enabled. 1: IGMP packet also forwards to processor port when Hardware based IGMP Snooping is enabled.
1	SIGS_EN	PH0,RW	Software-based IGMP Snooping Enable 0: Hardware based IGMP Snooping, without software intervention. (default) 1: Software based IGMP Snooping
0	IGS_EN	PH0,RW	IGMP Snooping Enable 0: Disable 1: Enable

6.62 Snooping Control Register 2 (79H)

Bit	Name	Default	Description
7	SCP_PE	PH0,RW	Snooping Control Packet Priority Enable 0: Disable 1: Enable
6:5	SCP_PRI	PH0,RW	Snooping Control Packet Priority 00: Queue 0 01: Queue 1 10: Queue 2 11: Queue 3
4:3	SCP_OTC	PH0,RW	Snooping Control Packet Output Tag Control 00: Unmodified 01: Always Tagged 10: Always Untagged 11: Reserved
2:0	RPP	PH0,RW	Router Port Portmap If User-defined IGMP Router Port Configuration is enabled, this 3-bit register is used to define static router portmap, otherwise, this register is automatic manipulation by IGMP snooping and read only.

6.63 Snooping Control Register 3 (7AH)

Bit	Name	Default	Description
7:0	QI	PH0,RW	Query Interval Define Query Interval when Hardware-IGS is enabled

6.64 Snooping Control Register 4 (7BH)

Bit	Name	Default	Description
7:2	RESERVED	0,RO	Reserved
1:0	RV	PH10,RW	Robustness Variable Define Robustness Variable when Hardware-IGS is enabled. 00 = Reserved 01 = 1 times 10 = 2 times (Default) 11 = 3 times

6.65 Snooping Control Register 5 (7CH)

Bit	Name	Default	Description
7:3	RESERVED	0,RO	Reserved
2	MLDS_OPT	PH0,RW	MLD Snooping Option Enable 0: Disable 1: Enable
1	MLD2UP	PH0,RW	MLD Packet Forward to uP Port only.
0	MLDS_EN	PH0,RW	MLD Snooping Enable 0: Disable 1: Enable

6.66 MIB counter Port Index Register (80H)

Bit	Name	Default	Description
7	READY	P0,RO	MIB counter data is ready
6	MIB_DIS	PHS0,RW	MIB Counter Disabled This bit has the opposite meaning in write and read: When write: 1: MIB counter disabled When read: 1: MIB counter is enabled
5	RESERVED	0,RO	Reserved
4:0	INDEX	PHS0,RW	MIB counter index 0~9, each counter is 32-bit in Register 81h~84h. Write the MIB counter index to this register before read them.

6.67 MIB counter Data Register (81H~84H)

Bit	Name	Default	Description
81H	Counter0	X,RO	Counter's data bit 7~0
82H	Counter1	X,RO	Counter's data bit 15~8
83H	Counter2	X,RO	Counter's data bit 23~16
84H	Counter3	X,RO	Counter's data bit 31~24

MIB counter: RX Byte Counter Registers (00H)

MIB counter: RX Uni-cast Packet Counter Registers (01H)

MIB counter: RX Multi-cast Packet Counter Registers (02H)

MIB counter: RX Discard Packet Counter Registers (03H)

MIB counter: RX Error Packet Counter Registers (04H)

MIB counter: TX Byte Counter Registers (05H)

MIB counter: TX Uni-cast Packet Counter Registers (06H)

MIB counter: TX Multi-cast Packet Counter Registers (07H)

MIB counter: TX Discard Packet Counter Registers (08H)

MIB counter: TX Error Packet Counter Registers (09H)

6.68 Per Port RX Packet Length Control Register (88H)

Bit	Name	Default	Description
7:2	RESERVED	PE0,RO	Reserved
1:0	PKT_LEN	PE0,RW	Accept Packet Length 0X: 1536-byte 10: 1800-byte 11: 2032-byte

6.69 Port-based VLAN mapping table Registers (B0H~BFH)

Define the port member in VLAN group
There are 16 VLAN group that defined in Reg. B0H~BFH.
Group 0 defined in Reg. B0H, and group 1 defined in Reg. B1H … and so on.

Bit	Name	Default	Description
7:4	RESERVED	PHE0,RO	Reserved
2	PORT_P2	PHE1,RW	Mapping to port 2
1	PORT_P1	PHE1,RW	Mapping to port 1
0	PORT_P0	PHE1,RW	Mapping to port 0

6.70 TOS Priority Map Registers (C0H~CFH)

Define the 6-bit or 3-bit of ToS field mapping to 2-bit priority queue number.
In 6-bit type, the Reg. 53H bit 7 is "1", Reg. C0H bit [1:0] define the mapping for ToS value 0, Reg. 60H bit [3:2] define the mapping for ToS value 1, … and so on, till Reg. CFH bit [7:6] define ToS value 63.
In 3-bit type, Reg. C0H bit [1:0] defines the mapping for ToS value 0, Reg. 60H bit [3:2] defines the mapping for ToS value 1 … and so on, and till Reg. C1H bit [7:6] define ToS value 7.

C0H:

Bit	Name	Default	Description
7:6	TOS3	PHE0/1,RW	If bit 53H.7 =1 :TOS[7:2]=03H, otherwise TOS]7:5]=03H
5:4	TOS2	PHE0,/1RW	If bit 53H.7 =1 :TOS[7:2]=02H, otherwise TOS]7:5]=02H
3:2	TOS1	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=01H, otherwise TOS]7:5]=01H
1:0	TOS0	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=00H, otherwise TOS]7:5]=00H

C1H:

Bit	Name	Default	Description
7:6	TOS7	PHE0/3,RW	If bit 53H.7 =1 :TOS[7:2]=07H, otherwise TOS]7:5]=07H
5:4	TOS6	PHE0/3,RW	If bit 53H.7 =1 :TOS[7:2]=06H, otherwise TOS]7:5]=06H
3:2	TOS5	PHE0/2,RW	If bit 53H.7 =1 :TOS[7:2]=05H, otherwise TOS]7:5]=05H
1:0	TOS4	PHE0/2,RW	If bit 53H.7 =1 :TOS[7:2]=04H, otherwise TOS]7:5]=04H

C2H:

Bit	Name	Default	Description
7:6	TOSB	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=0BH
5:4	TOSA	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=0AH
3:2	TOS9	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=09H
1:0	TOS8	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=08H

C3H:

Bit	Name	Default	Description
7:6	TOSF	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=0FH
5:4	TOSE	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=0EH
3:2	TOSD	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=0DH
1:0	TOSC	PHE0,RW	If bit 53H.7 =1 :TOS[7:2]=0CH

C4H:

Bit	Name	Default	Description
7:6	TOS13	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=13H
5:4	TOS12	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=12H
3:2	TOS11	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=11H
1:0	TOS10	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=10H

C5H:

Bit	Name	Default	Description
7:6	TOS17	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=17H
5:4	TOS16	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=16H
3:2	TOS15	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=15H
1:0	TOS14	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=14H

C6H:

Bit	Name	Default	Description
7:6	TOS1B	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=1BH
5:4	TOS1A	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=1AH
3:2	TOS19	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=19H
1:0	TOS18	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=18H

C7H:

Bit	Name	Default	Description
7:6	TOS1F	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=1FH
5:4	TOS1E	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=1EH
3:2	TOS1D	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=1DH
1:0	TOS1C	PHE1,RW	If bit 53H.7 =1 :TOS[7:2]=1CH

C8H:

Bit	Name	Default	Description
7:6	TOS23	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=23H
5:4	TOS22	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=22H
3:2	TOS21	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=21H
1:0	TOS20	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=20H

C9H:

Bit	Name	Default	Description
7:6	TOS27	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=27H
5:4	TOS26	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=26H
3:2	TOS25	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=25H
1:0	TOS24	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=24H

CAH:

Bit	Name	Default	Description
7:6	TOS2B	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=2BH
5:4	TOS2A	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=2AH
3:2	TOS29	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=29H
1:0	TOS28	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=28H

CBH:

Bit	Name	Default	Description
7:6	TOS2F	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=2FH
5:4	TOS2E	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=2EH
3:2	TOS2D	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=2DH
1:0	TOS2C	PHE2,RW	If bit 53H.7 =1 :TOS[7:2]=2CH

CCH:

Bit	Name	Default	Description
7:6	TOS33	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=33H
5:4	TOS32	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=32H
3:2	TOS31	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=31H
1:0	TOS30	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=30H

CDH:

Bit	Name	Default	Description
7:6	TOS37	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=37H
5:4	TOS36	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=36H
3:2	TOS35	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=35H
1:0	TOS34	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=34H

CEH:

Bit	Name	Default	Description
7:6	TOS3B	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=3BH
5:4	TOS3A	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=3AH
3:2	TOS39	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=39H
1:0	TOS38	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=38H

CFH:

Bit	Name	Default	Description
7:6	TOS3F	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=3FH
5:4	TOS3E	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=3EH
3:2	TOS3D	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=3DH
1:0	TOS3C	PHE3,RW	If bit 53H.7 =1 :TOS[7:2]=3CH

6.71 VLAN Priority Map Registers (D0H~D1H)

Define the 3-bit of priority field VALN mapping to 2-bit priority queue number

D0H:

Bit	Name	Default	Description
7:6	TAG3	PHE1,RW	VLAN priority tag value = 03H
5:4	TAG2	PHE1,RW	VLAN priority tag value = 02H
3:2	TAG1	PHE0,RW	VLAN priority tag value = 01H
1:0	TAG0	PHE0,RW	VLAN priority tag value = 00H

D1H:

Bit	Name	Default	Description
7:6	TAG7	PHE3,RW	VLAN priority tag value = 07H
5:4	TAG6	PHE3,RW	VLAN priority tag value = 06H
3:2	TAG5	PHE2,RW	VLAN priority tag value = 05H
1:0	TAG4	PHE2,RW	VLAN priority tag value = 04H

6.72 Memory Data Pre-Fetch Read Command without Address Increment Register (F0H)

Bit	Name	Default	Description
7:0	MRCMDX	X,RO	Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. And the DM9016 starts to pre-fetch the SRAM data to internal data buffers.

6.73 Memory Data Read Command with Address Increment Register (F2H)

When register FFH bit 7 is “0”, register F5H value will be returned to 0000H, if 16K-byte boundary is reached.
When register FFH bit 7 is “1”, register F5H value will be returned to 0000H, if processor port receive memory byte boundary address RX memory size, defined in register 3FH with default 1F00H, is reached.

Bit	Name	Default	Description
7:0	MRCMD	X,RO	Read data from RX SRAM. After the read of this command, the read pointer is increased by 1,2, or 4, depends on the operator mode (8-bit,16-bit and 32-bit respectively)

6.74 Memory Data Read address Register (F4H)

When register FFH bit 7 is “0”, register F5H and F4H can be used as memory byte address to read internal 64K-byte memory.
When register FFH bit 7 is “1”, register F5H and F4H can be used as processor port receive memory byte address with memory space range from 0 to (RX memory size - 1), defined in register 3FH with default 1EFFH.

Bit	Name	Default	Description
7:0	MDRAL	PHS0,RW	Memory Data Read_ address Low Byte

6.75 Memory Data Read address Register (F5H)

Bit	Name	Default	Description
7-6	RESERVED	P0,RO	Reserved
5:4	MDRAH65	PHS0,RW	Port number
3:0	MDRAH40	PHS0,RW	Memory Data Read_ address [11:8]

6.76 Memory Data Write Command without Address Increment Register (F6H)

Bit	Name	Default	Description
7:0	MWCMDX	X,WO	Write data to TX SRAM. After the write of this command, the write pointer is unchanged

6.77 Memory Data Write Command with Address Increment Register (F8H)

Bit	Name	Default	Description
7:0	MWCMD	X,WO	Write Data to TX SRAM After the write of this command, the write pointer is increased by 1, 2, or 4, depends on the operator mode. (8-bit, 16-bit,32-bit respectively)

6.78 Memory Data Write address Register (FAH)

Bit	Name	Default	Description
7:0	MDRAL	PHS0,RW	Memory Data Write_ address Low Byte

6.79 Memory Data Write address Register (FBH)

Bit	Name	Default	Description
7,6	RESERVED	P0,RO	Reserved
5:4	MDRAH65	PHS0,RW	Port number
3:0	MDRAH40	PHS0,RW	Memory Data Write_ address [11:8]

6.80 TX Packet Length Register (FCH~FDH)

Bit	Name	Default	Description
7:0	TXPLH	PHS0,RW	TX Packet Length High byte
7:0	TXPLL	PHS0,RW	TX Packet Length Low byte

6.81 Interrupt Status Register (FEH)

Bit	Name	Default	Description
7:6	M_WIDTH	T0, RO	Memory Bus Width Bit 7 Bit 6 0 0 16-bit mode 0 1 32-bit mode 1 0 8-bit mode 1 1 Reserved
5	LNKCHG	PHS0,RW/C1	Link Status Change of port 0 or 1
4	CNT_ERR	PHS0,RW/C1	BLK Table Counter error
3	ROO	PHS0,RW/C1	Receive Overflow Counter Overflow
2	ROS	PHS0,RW/C1	Receive Overflow
1	PT	PHS0,RW/C1	Packet Transmitted
0	PR	PHS0,RW/C1	Packet Received

6.82 Interrupt Mask Register (FFH)

Bit	Name	Default	Description
7	TXRX_EN	PHS0,RW	Enable the SRAM read/write pointer used as transmit /receive address.
6	RESERVED	0,RO	Reserved
5	LNKCHGI	PHS0,RW	Enable Link Status Change of port 0 or 1Interrupt
4	CNT_ERR	PHS0,RW/C1	Enable BLK Table Counter error interrupt
3	ROOI	PHS0,RW	Enable Receive Overflow Counter Overflow Interrupt
2	ROI	PHS0,RW	Enable Receive Overflow Interrupt
1	PTI	PHS0,RW	Enable Packet Transmitted Interrupt
0	PRI	PHS0,RW	Enable Packet Received Interrupt

7. EEPROM Format

Name	Word	Description
MAC address	0~2	6 Byte Ethernet Address
Auto Load Control	3	Bit[1:0] = 01: Accept Setting of WORD4 and WORD5 Bit[3:2] = 01: Accept setting of WORD6 [4:0] Bit[5:4] = Reserved, set to 00 in application Bit[7:6] = 01: Accept setting of WORD7 [3:0] Bit[9:8] = 01: Accept setting of WORD8 [4:0] Bit[11:10] = 01: Accept setting of WORD7[13:8] Bit[13:12] = Reserved, set to 00 in application Bit[15:14] = 01: Accept setting of WORD7 [15:14]
Vendor ID	4	2 byte vendor ID (Default: 0A46H)
Product ID	5	2 byte product ID (Default: 9016H)
Pin control	6	When word 3 bit [3:2] =01, these bits can control the CS#, IOR#, IOW# and IRQ pins polarity. Bit[0] 0: CS# pin is active low (default) 1: CS# pin is active high Bit[1] 0: IOR# pin is active low (default) 1: IOR# pin is active high Bit[2] 0: IOW# pin is active low (default) 1: IOW# pin is active high Bit[3] 0: IRQ pin is active high (default) 1: IRQ pin is active low Bit[4] 0: IRQ pin is force output (default) 1: IRQ pin is open-collected Bit [15:5] = Reserved, set to 0 in application
PHY control	7	Bit[0] 0: The WOL pin is active high (default) 1: The WOL pin is active low Bit[1] 0: The WOL pin is in level mode (default) 1: The WOL pin is in pulse mode Bit[2] 0: magic wakeup event is disable (default) 1: magic wakeup event is enabled Bit[3] 0: link change wakeup event is disable (default) 1: link change wakeup event is enabled Bit[7:4] = Reserved, set to 00 in application Bit[8] = LED mode 0: LED in normal mode (default, description see chapter 5.5) 1: LED be changed to following mode LNK0_LED/LNK1_LED active low indicates traffic active FDX0_LED/FDX1_LED active low indicates 100Mbps mode

		SPD0_LED/SPD1_LED active low indicates 10Mbps mode Bit[13:9] = set to 00000 for reserved Bit[14] = Port 1 AUTO-MDIX control 1: ON, 0: OFF(default ON) Bit[15] = Port 0 AUTO-MDIX control 1: ON, 0: OFF(default ON)
RESERVED	8~15	Reserved
Control	16	Bit[1:0] = 01: Accept setting of WORD 17,18 Bit[3:2] = 01: Accept setting of WORD 19~26 Bit[5:4] = 01: Accept setting of WORD 27~30 Bit[7:6] = 01: Accept setting of WORD 31 Bit[9:8] = 01: Accept setting of WORD 32~39 Bit[11:10] = 01: Accept setting of WORD 40~47 Bit[13:12] = 01: Accept setting of WORD 49~52 Bit[15:14] = Reserved, set to 0000 in application
Switch Control 1	17	When word 16 bit [1:0] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. 52H bit [7:0] This word bit [15:8] will be loaded to Reg. 53H bit [7:0]
RESERVED	18	This word must be cleared to 0000, if word 16 bit [1:0]=01
Port 0 Control 1	19	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 0 Reg. 61H bit [7:0] This word bit [15:8] will be loaded to port 0 Reg. 66H bit [7:0]
Port 0 Control 2	20	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 0 Reg. 67H bit [7:0] This word bit [15:8] will be loaded to port 0 Reg. 6DH bit [7:0]
Port 1 Control 1	21	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 1 Reg. 61H bit [7:0] This word bit [15:8] will be loaded to port 1 Reg. 66H bit [7:0]
Port 1 Control 2	22	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 1 Reg. 67H bit [7:0] This word bit [15:8] will be loaded to port 1 Reg. 6DH bit [7:0]
Port 2 Control 1	23	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 2 Reg. 61H bit [7:0] This word bit [15:8] will be loaded to port 2 Reg. 66H bit [7:0]
Port 2 Control 2	24	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 2 Reg. 67H bit [7:0] This word bit [15:8] will be loaded to port 2 Reg. 6DH bit [7:0]
uP Port Control 1	25	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 3 Reg. 61H bit [7:0] This word bit [15:8] will be loaded to port 3 Reg. 66H bit [7:0]
uP Port Control 2	26	When word 16 bit [3:2] is “01”, after power on reset: This word bit [7:0] will be loaded to port 3 Reg. 67H bit [7:0] This word bit [15:8] will be loaded to port 3 Reg. 6DH bit [7:0]
Port 0 VLAN Tag	27	When word 16 bit [5:4] is “01”, after power on reset: This word bit [7:0] will be loaded to port 0 Reg. 6EH bit [7:0] This word bit [15:8] will be loaded to port 0 Reg. 6FH bit [7:0]
Port 1 VLAN Tag	28	When word 16 bit [5:4[is “01”, after power on reset: This word bit [7:0] will be loaded to port 1 Reg. 6EH bit [7:0] This word bit [15:8] will be loaded to port 1 Reg. 6FH bit [7:0]
Port 2 VLAN Tag	29	When word 16 bit [5:4] is “01”, after power on reset: This word bit [7:0] will be loaded to port 2 Reg. 6EH bit [7:0] This word bit [15:8] will be loaded to port 2 Reg. 6FH bit [7:0]

uP Port VLAN Tag	30	When word 16 bit [5:4] is “01”, after power on reset: This word bit [7:0] will be loaded to port 3 Reg. 6EH bit [7:0] This word bit [15:8] will be loaded to port 3 Reg. 6FH bit [7:0]
VLAN Priority Map	31	When word 16 bit [7:6] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. D0H bit [7:0] This word bit [15:8] will be loaded to Reg. D1H bit [7:0]
Port VLAN Group 0,1	32	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. B0H bit [7:0] This word bit [15:8] will be loaded to Reg. B1H bit [7:0]
Port VLAN Group 2,3	33	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. B2H bit [7:0] This word bit [15:8] will be loaded to Reg. B3H bit [7:0]
Port VLAN Group 4,5	34	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. B4H bit [7:0] This word bit [15:8] will be loaded to Reg. B5H bit [7:0]
Port VLAN Group 6,7	35	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. B6H bit [7:0] This word bit [15:8] will be loaded to Reg. B7H bit [7:0]
Port VLAN Group 8,9	36	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. B8H bit [7:0] This word bit [15:8] will be loaded to Reg. B9H bit [7:0]
Port VLAN Group 10,11	37	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. BAH bit [7:0] This word bit [15:8] will be loaded to Reg. BBH bit [7:0]
Port VLAN Group 12,13	38	When word 16 bit [9:8] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. BCH bit [7:0] This word bit [15:8] will be loaded to Reg. BDH bit [7:0]
Port VLAN Group 14,15	39	When word 16 bit 9:8 is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. BEH bit [7:0] This word bit [15:8] will be loaded to Reg. BFH bit [7:0]
ToS Priority Map 0	40	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. C0H bit [7:0] This word bit [15:8] will be loaded to Reg. C1H bit [7:0]
ToS Priority Map 1	41	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. C2H bit [7:0] This word bit [15:8] will be loaded to Reg. C3H bit [7:0]
ToS Priority Map 2	42	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. C4H bit [7:0] This word bit [15:8] will be loaded to Reg. C5H bit [7:0]
ToS Priority Map 3	43	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. C6H bit [7:0] This word bit [15:8] will be loaded to Reg. C7H bit [7:0]
ToS Priority Map 4	44	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. C8H bit 7~0 This word bit [15:8] will be loaded to Reg. C9H bit 7~0
ToS Priority Map 5	45	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. CAH bit [7:0] This word bit [15:8] will be loaded to Reg. CBH bit [7:0]
ToS Priority Map 6	46	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0] will be loaded to Reg. CCH bit [7:0]

		This word bit [15:8] will be loaded to Reg. CDH bit [7:0]
ToS Priority Map 7	47	When word 16 bit [11:10] is “01”, after power on reset: This word bit [7:0]0 will be loaded to Reg. CEH bit [7:0] This word bit [15:8] will be loaded to Reg. CFH bit [7:0]
RESERVED	48	Reserved
Port Security Control	49	When word 16 bit [13:12] is “01”, after power on reset: This word bit [3:0] will be loaded to port 0 register 6CH bit [2:0] This word bit [7:4] will be loaded to port 1 register 6CH bit [2:0] This word bit [11:8] will be loaded to port 2 register 6CH bit [2:0]
Snooping Control 1	50	When word 16 bit [13:12] is “01”, after power on reset: This word bit [7:0] will be loaded to register 78H This word bit [15:8] will be loaded to register 79H
Snooping Control 2	51	When word 16 bit [13:12] is “01”, after power on reset: This word bit [7:0] will be loaded to register 7AH This word bit [15:8] will be loaded to register 7BH
Snooping Control 3	52	When word 16 bit [13:12] is “01”, after power on reset: This word bit [1:0] will be loaded to register 7CH bit [1:0]

8. PHY Registers

MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01H	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02H	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03H	PHYID2	1	0	1	1	1	0	Model No.						Version No.			
								01011						0000			
04H	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05H	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06H	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
10H	Specified Config.	BP 4B5B	BP SCR	BP ALIGN	BP_ADP OK	Reserved	TX	Reserved	Reserved	Force 100LNK	Reserved	Reserved	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
11H	Specified Conf/Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserved	Reversed	Reversed	PHY ADDR [4:0]					Auto-N. Monitor Bit [3:0]			
12H	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Reserved	Reserved									Polarity Reverse
13H	PWDOR	Reserved							PD10DRV	PD100I	PDchip	PDcrm	PDaeq	PDdrv	PDedi	PDeclo	PD10
14H	Specified config	TSTSE1	TSTSE2	FORCE_TXSD	FORCE_FEF	PREAMBLEX	TX10M_PWR	NWAY_PWR	Reserved	MDIX_CNTL	AutoNeg_dlpbk	Mdix_fix Value	Mdix_down	MonSel1	MonSel0	Reserved	PD_value
16H	RCVER	Receiver Error Counter															
17H	DIS_connect	Reversed									Disconnect_counter						
1DH	PSCR	Reversed				PREAMBLEX	AMPLITUDE	TX_PWR	Reversed								
1EH	DATA	indirect data															
1FH	ADDR													indirect address			

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>
Where:
<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

<Access Type>:
RO = Read only, RW = Read/Write
<Attribute (s)>:
SC = Self clearing, P = Value permanently set

8.1 Basic Mode Control Register (BMCR) – 00H

Bit	Bit Name	Default	Description
15	Reset	0, RW/SC	Reset 0=Normal operation 1=Software reset This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
14	Loopback	0, RW	Loopback Loop-back control register 0 = Normal operation 1 = Loop-back enabled When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs
13	Speed selection	1, RW	Speed Select 0 = 10Mbps 1 = 100Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type
12	Auto-negotiation enable	1, RW	Auto-negotiation Enable 0= Auto-negotiation is disabled 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status
11	Power down	0, RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 0=Normal operation 1=Power down
10	Isolate	0,RW	Isolate Force to 0 in application.
9	Restart Auto-negotiation	0,RW/SC	Restart Auto-negotiation 0 = Normal operation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM9016. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit
8	Duplex mode	1,RW	Duplex Mode 0 = Normal operation 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability

			selected by auto-negotiation
7	Collision test	0,RW	Collision Test 0 = Normal operation 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN in internal MII interface.
6-0	Reserved	0,RO	Reserved Read as 0, ignore on write

8.2 Basic Mode Status Register (BMSR) – 01H

Bit	Bit Name	Default	Description
15	100BASE-T4	0,RO/P	100BASE-T4 Capable 0 = not able to perform in 100BASE-T4 mode 1 = able to perform in 100BASE-T4 mode
14	100BASE-TX full-duplex	1,RO/P	100BASE-TX Full Duplex Capable 0 = not able to perform 100BASE-TX in full duplex mode 1 = able to perform 100BASE-TX in full duplex mode
13	100BASE-TX half-duplex	1,RO/P	100BASE-TX Half Duplex Capable 0 = not able to perform 100BASE-TX in half duplex mode 1 = able to perform 100BASE-TX in half duplex mode
12	10BASE-T full-duplex	1,RO/P	10BASE-T Full Duplex Capable 0 = not able to perform 10BASE-TX in full duplex mode 1 = able to perform 10BASE-T in full duplex mode
11	10BASE-T half-duplex	1,RO/P	10BASE-T Half Duplex Capable 0 = not able to perform 10BASE-T in half duplex mode 1 = able to perform 10BASE-T in half duplex mode
10-7	Reserved	0,RO	Reserved Read as 0, ignore on write
6	MF preamble suppression	1,RO	MII Frame Preamble Suppression 0 = not accept management frames with preamble suppressed 1 = accept management frames with preamble suppressed
5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete 0 = Auto-negotiation process not completed 1 = Auto-negotiation process completed
4	Remote fault	0, RO	Remote Fault 0 = No remote fault condition detected 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9016 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set
3	Auto-negotiation ability	1,RO/P	Auto Configuration Ability 0 = not able to perform auto-negotiation

			1 = able to perform auto-negotiation
2	Link status	0,RO	Link Status 0 = Link is not established 1 = Valid link is established (for either 10Mbps or 100Mbps operation) The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1	Jabber detect	0, RO	Jabber Detect 0 = No jabber 1 = Jabber condition detected This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9016 reset. This bit works only in 10Mbps mode
0	Extended capability	1,RO/P	Extended Capability 0 = Basic register capable only 1 = Extended register capable

8.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9016. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
15-0	OUI_MSB	<0181h>	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

8.4 PHY ID Identifier Register #2 (PHYID2) – 03H

Bit	Bit Name	Default	Description
15-10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9-4	VNDR_MDL	<001011>, RO/P	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3-0	MDL_REV	<0000>, RO/P	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

8.5 Auto-negotiation Advertisement Register (ANAR) – 04H

This register contains the advertised abilities of this DM9016 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	0,RO/P	Next page Indication 0 = No next page available 1 = Next page available The DM9016 has no next page, so this bit is permanently set to 0
14	ACK	0,RO	Acknowledge 0 = Not acknowledged 1 = Link partner ability data reception acknowledged The DM9016's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit.
13	RF	0, RW	Remote Fault 0 = No fault detected 1 = Local device senses a fault condition
12-11	Reserved	X, RW	Reserved Write as 0, ignore on read
10	FCS	1, RW	Flow Control Support 0 = Controller chip doesn't support flow control ability 1 = Controller chip supports flow control ability
9	T4	0, RO/P	100BASE-T4 Support 0 = 100BASE-T4 is not supported 1 = 100BASE-T4 is supported by the local device The DM9016 does not support 100BASE-T4 so this bit is permanently set to 0
8	TX_FDX	1, RW	100BASE-TX Full Duplex Support 0 = 100BASE-TX full duplex is not supported 1 = 100BASE-TX full duplex is supported by the local device
7	TX_HDX	1, RW	100BASE-TX Support 0 = 100BASE-TX half duplex is not supported 1 = 100BASE-TX half duplex is supported by the local device
6	10_FDX	1, RW	10BASE-T Full Duplex Support 0 = 10BASE-T full duplex is not supported 1 = 10BASE-T full duplex is supported by the local device
5	10_HDX	1, RW	10BASE-T Support 0 = 10BASE-T half duplex is not supported 1 = 10BASE-T half duplex is supported by the local device
4-0	Selector	<00001>, RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05H

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
15	NP	0, RO	Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available
14	ACK	0, RO	Acknowledge 0 = Not acknowledged 1 = Link partner ability data reception acknowledged The DM9016's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit
13	RF	0, RO	Remote Fault 0 = No remote fault indicated by link partner 1 = Remote fault indicated by link partner
12-11	Reserved	0, RO	Reserved Read as 0, ignore on write
10	FCS	0, RO	Flow Control Support 0 = Controller chip doesn't support flow control ability by link partner 1 = Controller chip supports flow control ability by link partner
9	T4	0, RO	100BASE-T4 Support 0 = 100BASE-T4 is not supported by the link partner 1 = 100BASE-T4 is supported by the link partner
8	TX_FDX	0, RO	100BASE-TX Full Duplex Support 0 = 100BASE-TX full duplex is not supported by the link partner 1 = 100BASE-TX full duplex is supported by the link partner
7	TX_HDX	0, RO	100BASE-TX Support 0 = 100BASE-TX half duplex is not supported by the link partner 1 = 100BASE-TX half duplex is supported by the link partner
6	10_FDX	0, RO	10BASE-T Full Duplex Support 0 = 10BASE-T full duplex is not supported by the link partner 1 = 10BASE-T full duplex is supported by the link partner
5	10_HDX	0, RO	10BASE-T Support 0 = 10BASE-T half duplex is not supported by the link partner 1 = 10BASE-T half duplex is supported by the link partner
4-0	Selector	<00000>, RO	Protocol Selection Bits Link partner's binary encoded protocol selector

8.7 Auto-negotiation Expansion Register (ANER) - 06H

Bit	Bit Name	Default	Description
15-5	Reserved	0, RO	Reserved Read as 0, ignore on write
4	PDF	0, RO/LH	Local Device Parallel Detection Fault PDF = 1: A fault detected via parallel detection function. PDF = 0: No fault detected via parallel detection function
3	LP_NP_ABLE	0, RO	Link Partner Next Page Able LP_NP_ABLE = 1: Link partner, next page available LP_NP_ABLE = 0: Link partner, no next page
2	NP_ABLE	0,RO/P	Local Device Next Page Able NP_ABLE = 1: DM9016, next page available NP_ABLE = 0: DM9016, no next page DM9016 does not support this function, so this bit is always 0
1	PAGE_RX	0, RO	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able A “1” in this bit indicates that the link partner supports Auto-negotiation

8.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Bit Name	Default	Description
15	BP_4B5B	0,RW	Bypass 4B5B Encoding and 5B4B Decoding 0 = Normal 4B5B and 5B4B operation 1 = 4B5B encoder and 5B4B decoder function bypassed
14	BP_SCR	0, RW	Bypass Scrambler/Descrambler Function 0 = Normal scrambler and descrambler operation 1 = Scrambler and descrambler function bypassed
13	BP_ALIGN	0, RW	Bypass Symbol Alignment Function 0 = Normal operation 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed
12	BP_ADPOK	0, RW	BYPASS ADPOK Force signal detector (SD) active. This register is for debug only, not release to customer 0=Normal operation 1=Forced SD is OK,
11	Reserved	RW	Reserved Force to 0 in application
10	TX	1, RW	100BASE-TX Mode Control 0 = 100BASE-FX operation 1 = 100BASE-TX operation
9	Reserved	0, RO	Reserved

8	Reserved	0, RW	Reserved
7	F_LINK_100	0, RW	Force Good Link in 100Mbps 0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes
6	Reserved	0, RW	Reserved Force to 0 in application.
5	COL_LED	0, RW	COL LED Control (valid in PHY test mode)
4	RPDCTR-EN	1, RW	Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 0 = Disable automatic reduced power down 1 = Enable automatic reduced power down
3	SMRST	0, RW	Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed
2	MFPSC	1, RW	MF Preamble Suppression Control MII frame preamble suppression control bit 0 = MF preamble suppression bit off 1 = MF preamble suppression bit on
1	SLEEP	0, RW	Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
0	RLOUT	0, RW	Remote Loop out Control When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

Bit	Bit Name	Default	Description
15	100FDX	1, RO	100M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
14	100HDX	1, RO	100M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
13	10FDX	1, RO	10M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
12	10HDX	1, RO	10M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
11	Reserved	0, RO	Reserved Read as 0, ignore on write
10-9	Reserved	0,RW	Reserved
8-4	PHYADR[4:0]	1, RW	PHY Address Bit 4:0 The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY
3-0	ANMB[3:0]	0, RO	Auto-negotiation Monitor Bits These bits are for debug only. The auto-negotiation status will be written to these bits.

B3	B2	B1	B0	
0	0	0	0	In IDLE state
0	0	0	1	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detects signal link ready
0	1	1	1	Parallel detects signal link ready fail
1	0	0	0	Auto-negotiation completed successfully

8.10 10BASE-T Configuration/Status (10BTCSR) – 12H

Bit	Bit Name	Default	Description
15	Reserved	0, RO	Reserved Read as 0, ignore on write
14	LP_EN	1, RW	Link Pulse Enable 0 = Link pulses disabled, good link condition forced 1 = Transmission of link pulses enabled This bit is valid only in 10Mbps operation
13	HBE	1,RW	Heartbeat Enable 0 = Heartbeat function disabled 1 = Heartbeat function enabled When the DM9016 is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode)
12	SQUELCH	1, RW	Squelch Enable 0 = Low squelch 1 = Normal squelch
11	JABEN	1, RW	Jabber Enable Enables or disables the Jabber function when the DM9016 is in 10BASE-T full duplex or 10BASE-T transceiver Loopback mode 0 = Jabber function disabled 1 = Jabber function enabled
10	SERIAL	0, RW	10M Serial Mode (valid in PHY test mode) Force to 0, in application.
9-1	Reserved	0, RO	Reserved Read as 0, ignore on write
0	POLR	0, RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module

8.11 Power Down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
15-9	Reserved	0, RO	Reserved Read as 0, ignore on write
8	PD10DRV	0, RW	Vendor power down control test
7	PD100DL	0, RW	Vendor power down control test
6	PDchip	0, RW	Vendor power down control test
5	PDcrm	0, RW	Vendor power down control test
4	PDaeq	0, RW	Vendor power down control test
3	PDdrv	0, RW	Vendor power down control test
2	PDedi	0, RW	Vendor power down control test
1	PDedo	0, RW	Vendor power down control test
0	PD10	0, RW	Vendor power down control test

***** When selected, the power down value is control by Register 0x14H

8.12 (Specified config) Register – 14H

Bit	Bit Name	Default	Description
15	TSTSE1	0,RW	Vendor test select control
14	TSTSE2	0,RW	Vendor test select control
13	FORCE_TXSD	0,RW	Force Signal Detect 0: normal SD signal. 1: force SD signal OK in 100M
12	FORCE_FEF	0,RW	Vendor test select control
11	PREAMBLEX	0,RW	Preamble Saving Control 0: when bit 10 is set, the 10M TX preamble count is reduced. When bit 11 of register 29 is set, 12-bit preamble bit is reduced; otherwise 22-bit preamble bits is reduced. 1: 10M TX preamble bit count is normal.
10	TX10M_PWR	1,RW	10M TX Power Saving Control 1: enable 10M TX power saving 0: disable 10M TX power saving
9	NWAY_PWR	0,RW	N-Way Power Saving Control 1: disable N-Way power saving 0: enable N-Way power saving
8	Reserved	0, RO	Reserved Read as 0, ignore on write
7	MDIX_CNTL	MDI/MDIX,RO	The polarity of MDI/MDIX value 0: MDI mode 1: MDIX mode
6	AutoNeg_dpbk	0,RW	Auto-negotiation Loopback 0: normal. 1: test internal digital auto-negotiation Loopback
5	Mdix_fix Value	0, RW	MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value.
4	Mdix_down	0,RW	MDIX Down Manual force MDI/MDIX. 0: Enable HP Auto-MDIX 1: Disable HP Auto-MDIX , MDIX_CNTL value depend on 20.5
3	MonSel1	0,RW	Vendor monitor select
2	MonSel0	0,RW	Vendor monitor select
1	Reserved	0,RW	Reserved Force to 0, in application.
0	PD_value	0,RW	Power down control value Decision the value of each field Register 19. 0: normal 1: power down

8.13 DAVICOM Specified Receive Error Counter Register (RECR) – 16H

Bit	Bit Name	Default	Description
15-0	Rcv_ Err_ Cnt	0, RO	Receive Error Counter Receive error counter that increments upon detection of RXER. Clean by read this register.

8.14 DAVICOM Specified Disconnect Counter Register (DISCR) – 17H

Bit	Bit Name	Default	Description
15-8	Reserved	0, RO	Reserved
7-0	Disconnect Counter	0, RO	Disconnect Counter that increment upon detection of disconnection. Clean by read this register.

8.15 Power Saving Control Register (PSCR) – 1DH

Bit	Bit Name	Default	Description
15-12	RESERVED	0,RO	RESERVED
11	PREAMBLEX	0,RW	Preamble Saving Control when both bit 10and 11 of register 0x14H are set, the 10M TX preamble count is reduced. 1: 12-bit preamble bit is reduced. 0: 22-bit preamble bits is reduced.
10	AMPLITUDE	0,RW	10M TX Amplitude Control Disabled 1: when cable is unconnected with link partner, the TX amplitude is reduced for power saving. 0: disable TX amplitude reduce function
9	TX_PWR	0.RW	TX Power Saving Control Disabled 1: when cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 0: disable TX driving power saving function
8-0	RESERVED	0,RO	RESERVED

8.16 DAVICOM indirect DATA Register (DATA) – 1EH

Bit	Bit Name	Default	Description
15-0	DATA	0, RW	In-direct DATA register When write, data to register that addressing by ADDR When read, data from register that addressing by ADDR

8.17 DAVICOM indirect ADDR Register (ADDR) – 1FH

Bit	Bit Name	Default	Description
15-8	Reserved	0, RO	Reserved
3-0	ADDR	0, RW	In-direct ADDR register 1: addressing to power saving control register (same as REG 1DH) 2: reserved 3: reserved 4: addressing to TX amplitude control register

8.18 DAVICOM indirect TX Amplitude Control Register (TX_OUT_CNTL) – indirect-04H

Bit	Bit Name	Default	Description
15-6	Reserved	0, RO	Reserved
5-0	TX AMPLITUDE	0, RW	TX amplitude control To tune the amplitude of TX +/-.

9. Functional Description

9.1 Processor bus and memory management function:

9.1.1 Processor Interface

In the general processor mode, the chip selection is just coming from pin 2 (CS#). There are only two addressing ports through the access of the host interface.

One port is the INDEX port and the other is the DATA port. The INDEX port is decoded by the CMD pin=0 and the DATA by the CMD pin=1. The contents of the INDEX port are the register address of the DATA port. Before the access of any register, the address of the register must be saved in the INDEX port before.

9.1.2 Direct Memory Access Control

The DM9016 provides DMA capability to simplify the access of the internal memory. After the setting of the starting address of the internal memory and then issuing a dummy read/write command to load the current data to internal data buffer, the desired location of the internal memory can be accessed by the read/write command registers. The memory's address will be increased with the size equal to the current operation mode (i.e. the byte, word or double-word mode) and the data of the next location will be loaded to internal data buffer automatically. It is noted that the data of the first access (the dummy read/write command) in a sequential burst should be ignored because that the data was the contents of the last read/write command.

There are two configured types of internal memory which are controlled by bit 7 of IMR. When the bit 7 of IMR is set, the internal memory is used for transmit and receive buffers. The transmit buffer occupies 7.5K bytes in 3-port mode and 8K bytes in 2-port mode. And the receive buffer occupies 7.5K bytes in 3-port mode and 7.75K bytes in 2-port mode. Both the transmit and receive buffer address need not to be programmed instead that they are managed by the DM9016 automatically. In transmit function, after power on reset or each time after the transmit command is issued (bit 0 of TCR is set), the next starting transmit buffer address is loaded. In receive function, the 7.5K-byte (or 7.75K-byte) receive buffer can be treated as a continued logic memory space. The memory address will wrap to address 0 if the end of address is reached.

When the bit 7 of IMR is cleared, there is a 64K-byte memory space in the DM9016 can be accessed. This configured type of internal memory is used for testing only. The memory write address (register FAh/FBh) and the memory read address (register F4h/F5h) represent the physical memory address of the DM9016 internal memory. It is noted that after the memory had been written by memory write command, the switch reset command (bit 6 of register 52h) should be set before normal switch function operation, since the controlled data in internal memory may be corrupted.

9.1.3 Packet Transmission

There are two packets, sequentially named as index I and index II, can be stored in the TX SRAM at the same time. The index register 02h controls the insertion of CRC.

The start address of transmission is 00h and the current packet is index I after software or hardware reset. Firstly write data to the TX SRAM using the DMA port and then write the byte count to byte count register at index register 0fch and 0fdh. Set the bit 1 of control register. The DM9016 starts to transmit the index I packet. Before the transmission of the index I packet ends, the data of the next (index II) packet can be moved to TX SRAM. After the index I packet ends the transmission, write the byte count data of the index II to BYTE_COUNT register and then set the bit 1 of control register to transmit the index II packet. The following packets, named index I, II, I, II… use the same way to be transmitted.

9.1.4 Packet Reception

The RX SRAM is a ring data structure. Each packet has a 4-byte header followed with the data of the reception packet which CRC field is included. The format of the 4-byte header is 01h, status, BYTE_COUNT low, and BYTE_COUNT high. It is noted that the start address of each packet is in the proper address boundary which depends on the operation mode (byte, word, or double-word mode).

9.2 Switch function:

9.2.1 Address Learning

The DM9016 stores MAC addresses, port number and time stamp information in the Hash-based Address Table. The table can learn up to 1K unicast address entries. The DM9016 provides two methods to learn address in the table, self-learning and manual learning.

Self-learning

The self-learning mechanism means the DM9016 learn the MAC addresses of incoming packets in real time without CPU's assistance.

The switch engine creates a new entry if incoming packet's Source Address (SA) does not exist and the packet is valid (error-free). If SA was found and incoming port mismatch with port number in table, update the entry with SA and incoming port number. Those entries will be created, updated or aged dynamically.

Besides, the DM9016 has an option to disable address learning for individual port. This feature can be set by bit 0 of register 65h.

Manual Learning

The DM9016 also provides manual learning mechanism with CPU's assistance. The CPU can create, update or delete entry for flexible management. In addition to above, the entry can be set as static one that will not be aged-out forever.

9.2.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time.

The period can be programmed or disabled through bit 0 & 1 of register 52h.

9.2.3 Packet Forwarding

The DM9016 forwards the incoming packet according to following decision:

(1). If DA is Multicast/Broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.

(2). Switch engine would look up address table based on DA when incoming packets is UNICAST. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.

(3). Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM9016 will filter incoming packets under following conditions:

(1). Error packets, including CRC errors, alignment errors, illegal size errors.

(2). PAUSE packets.

(3). If incoming packet is UNICAST and its destination port number is equal to source port number.

9.2.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

9.2.5 Back-off Algorithm

The DM9016 implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

9.2.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

9.2.7 Full Duplex Flow Control

The DM9016 supports IEEE standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, The DM9016 will defer transmitting next normal frames, if it receives a pause frame from link partner.

On the transmit side, The DM9016 issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once

resources are available, The DM9016 sends out a pause frame with zero pause time allows traffic to resume immediately.

9.2.8 Half Duplex Flow Control

The DM9016 supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM9016 sends jam pattern, thus forcing a collision.

The flow control ability can be set in bit 4 of register 61h.

9.2.9 Partition Mode

The DM9016 provides a partition mode for each port, see bit 6 of register 61h. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

(1). Entering Partition State

A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

(2). While in Partition state:

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

(3). Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

9.2.10 Broadcast Storm Filtering

The DM9016 has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two type of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through bit 1 of register 61h.

The broadcast storm threshold can be programmed by EEPROM or register 67h, the default setting is no broadcast storm protecting.

9.2.11 Bandwidth Control

The DM9016 supports two type of bandwidth control for each port. One is the ingress and egress bandwidth rate can be control separately, the other is combined together, this function can be set through bit 3 of register 61h. The bandwidth control is disabled by default.

For separated bandwidth control mode, the threshold rate is defined in register 66h. For combined mode, it is defined in register 67h.

The behavior of bandwidth control as below:

(1).For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.

(2).For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.

(3).In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

9.2.12 Port Monitoring Support

The DM9016 supports “Port Monitoring” function on per port base, detail as below:

(1). Sniffer Port and Monitor Port

There is only one port can be selected as “sniffer port” by register 52h, multiple ports can be set as “receive monitor port” or “transmit monitor port” in per-port register 65h.

(2).Receive monitor

All packets received on the “receive monitor port” are send a copy to “sniffer port”. For example, port 0 is set as “receive monitor port” and port 3 is selected

as “sniffer port”. If a packet is received form port 0 and predestined to port 1 after forwarding decision, the DM9016 will forward it to port 1 and port 3 in the end.

(3).Transmit monitor

All packets transmitted on the “transmit monitor port” are send a copy to “sniffer port”. For example, port 1 is set as “transmit monitor port” and port 3 is selected as “sniffer port”. If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM9016 will forward it to port 1 and port 3 in the end.

(4).Exception

The DM9016 has an optional setting that broadcast/multicast packets are not monitored (see bit 4 of register 65h). It’s useful to avoid unnecessary bandwidth.

9.2.13 VLAN Support

9.2.13.1 Port-Based VLAN

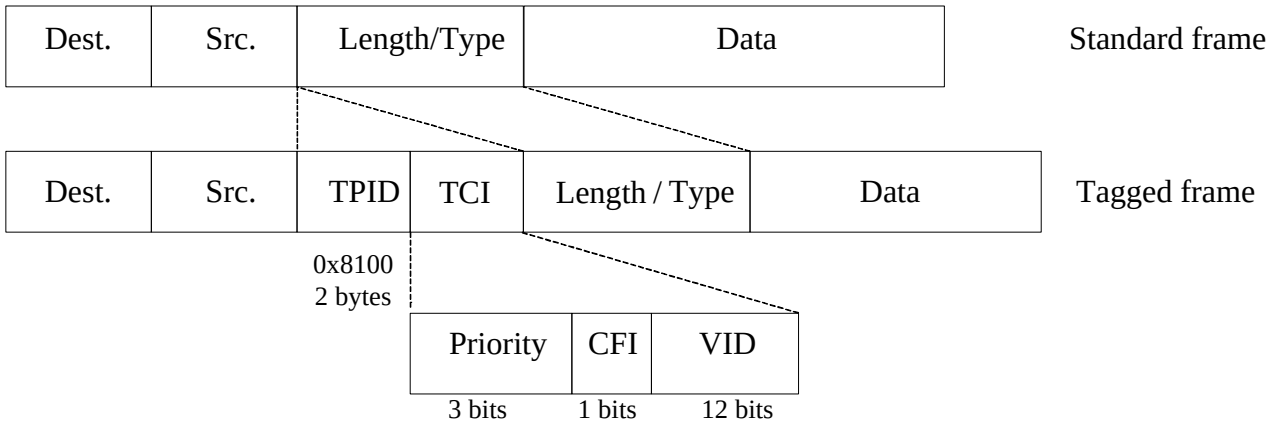
The DM9016 supports port-based VLAN as default, up to 16 groups. Each port has a default VID called PVID (Port VID, see register 6Fh). The DM9016 used LSB 4-bytes of PVID as index and mapped to register B0h~BFh, to define the VLAN groups.

For instance, we intend to partition DM9016’s ports into three groups. Port 0 and port 1 in group A, port 1 and port 2 in group B, finally, port 2 and port 3 in group C. In this case, the setting as below:

(1). Set PVID of Port 0 to 0x01h.
(2). Set PVID of Port 1 to 0x02h.
(3). Set PVID of Port 2 to 0x03h.
(4). Set PVID of Port 3 to 0x04h.
(5). Set register B1h to 0x02h.
(6). Set register B2h to 0x05h.
(7). Set register B3h to 0x0Ah.
(8). Set register B4h to 0x04h.

9.2.13.2 802.1Q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).



The DM9016 also supports 16 802.1Q-based VLAN groups, as specified in bit 1 of register 53h. It’s obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM9016 used LSB 4-bytes VID of received packet with VLAN tag and VLAN Group Mapping Register (B0h~BFh) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.

9.2.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by bit 7 of register 6Dh in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

(1). Receive untagged packet and forward to Un-tag port.

Received packet will forward to destination port without modification.

(2). Receive tagged packet and forward to Un-tag port.

The DM9016 will remove the tag from the packet and recalculate CRC before sending it out.

(3). Receive untagged packet and forward to Tag port.

The DM9016 will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

(4). Receive tagged packet and forward to Tag port.

Received packet will forward to destination port without modification.

9.2.14 Priority Support

The DM9016 supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM9016 provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM9016 offers four level queues for transmit on per-port based.

The DM9016 provides two packet scheduling algorithms: Weighted Round Robin Queuing (WRR) and Strict Priority Queuing (SPQ). Weighted Round Robin Queuing (WRR) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The Packet on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in bit 5 of register 6Dh.

9.2.14.1 Port-Based Priority

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in bit 0 and 1 of register 6Dh.

9.2.14.2 802.1p-Based Priority

802.1p priority can be disabled by bit 2 of register 6Dh, it is enabled by default.

The DM9016 extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers (D0h~D1h) to determine which transmit queue is designated. The VLAN Priority Map is programmable.

9.2.14.3 DiffServ-Based Priority

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (C0h~CFh) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see bit 7 of register 53h.

9.2.15 Address Table Accessing

Type of Address Table

There are three types of address table in the DM9016. The description is represented below:

(1). Unicast Address Table

This table is used for destination MAC address lookup and source MAC address learning. The table can have up to 1024 entries. If the table is full, the latest one will kick out the eldest one. The programming method can refer to next section.

(2). Multicast Address Table

This table stores multicast addresses up to 256 entries and can be maintained by host CPU for custom filtering and forwarding multicast packets. If the table is full, the latest one will kick out the eldest one. All of entries in multicast address table are static one. In addition to host CPU, multicast address table can be manipulated by internal switch engine, if hardware-based IGMP Snooping function is enabled.

(3). IGMP Membership Table

This table is used to establish IPv4 multicast forwarding rule under IGMP protocol if hardware-based IGMP Snooping function is enabled. It is automatic maintained by internal engine according to snooping IGMP control packets, and can only support to read out by the host CPU. The maximum of entries of table is 16. If the table is full, never join anymore.

9.2.16 Access Rules of Address Table

The DM9016 The procedure and flow chart of Entry Write is described as following:

Entry Write

(1). Check the busy bit of Ethernet Address Control/Status Register 1 (Reg70H.0) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the MAC address to the Ethernet Address Data Registers (Reg71H~76H).

(3). Write the Port Number (if target is unicast address table) or Port Map (if target is multicast address table) to Ethernet Address Data Register (Reg77H.[3:0]).

(4). If need, write the entry's attributes that includes both static and overriding to Ethernet Address Control/Status Register 1 (Reg77H).

(5). Write the "WRITE" command and assign the target table to Ethernet Address Control/Status Register 1 (Reg70H.[4:1]) to start the operation.

(6). Check the busy bit again, wait for available.

(7). Read the command status from Ethernet Address Control/Status Register 1 (Reg70H.[6:5]).

Entry Delete

(1). Check the busy bit of Ethernet Address Control/Status Register 1 (Reg70H.0) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the MAC address to the Ethernet Address Data Register (Reg71H~76H).

(3). Write the "DELETE" command and assign the target table to Ethernet Address Control/Status Register 1 (Reg70H.[4:1]) to start the operation.

(4). Check the busy bit again, wait for available.

(5). Read the command status from Ethernet Address Control/Status Register 1 (Reg70H.[6:5]).

Entry Search

(1). Check the busy bit of Ethernet Address Control/Status Register 1 (Reg70H.0) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the MAC address to the Ethernet Address Data Register (Reg71H~76H).

(3). Write the "SEARCH" command and assign the target table to Ethernet Address Control/Status Register 1 (Reg70H.[4:1]) to start the operation.

(4). Check the busy bit again, wait for available.

(5). Read the command status from Ethernet Address Control/Status Register 1 (Reg70H.[6:5]).

(6). Read the Port Number or Port Map from Ethernet Address Control/Status Register 2 (Reg77H.[3:0])

(7). If need, read the entry sequence (the sequence number of entry in address table) from Ethernet Address Data Register (Reg71H~72H).

(8). If need, read the entry's attributes that include static (unicast address table only), IGMP signature (multicast address table only) and overriding from Ethernet Address Control/Status Register 2 (77H.[6:4]).

Entry Read

(1). Check the busy bit of Ethernet Address Control/Status Register 1 (Reg70H.0) to seek the availability of access engine. Waiting until engine is available and to keep on following.

(2). Write the entry sequence to the Ethernet Address Data Register (Reg71H~76H).

(3). Write the "READ" command and assign the target table to Ethernet Address Control/Status Register 1 (Reg70H.[4:1]) to start the operation.

(4). Check the busy bit again, wait for available.

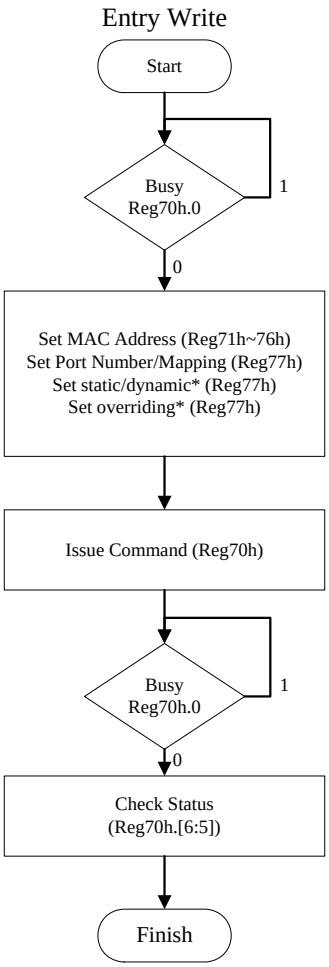
(5). Read the command status from Ethernet Address Control/Status Register 1 (70H.[6:5]).

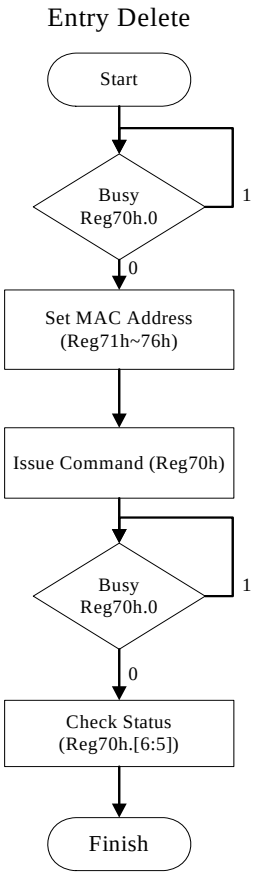
(6). Read the Port Number or Port Map from Ethernet Address Control/Status Register 2 (Reg77H.[3:0])

(7). If target is unicast or multicast address table, read the entry's MAC address from Ethernet Address Data Register (Reg71H~76H). If target is IGMP membership table, read the entry

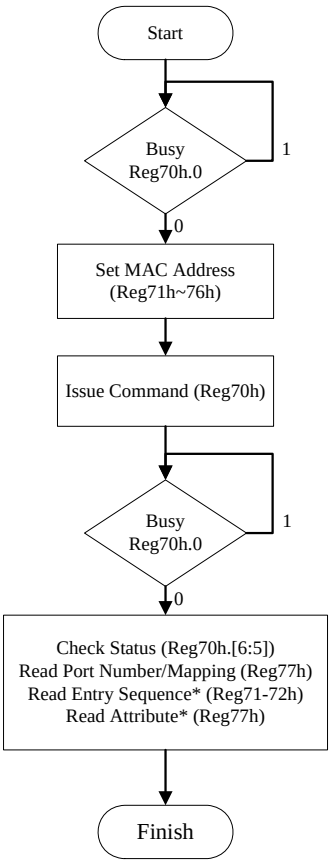
sequence (the sequence number of entry in address table) from Ethernet Address Data Register (Reg71H~72H).

(8). If need, read the entry's attributes that include static, IGMP signature and overriding from Ethernet Address Control/Status Register 2 (Reg77H.[6:4]).

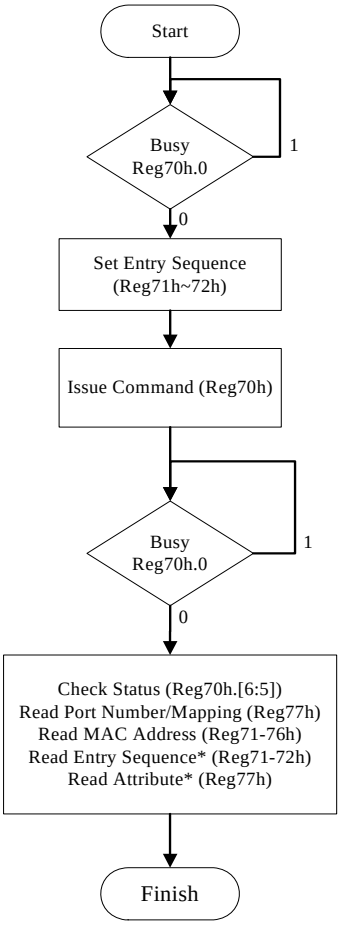




Entry Search



Entry Read



9.2.17 IGMP Snooping

The Internet Group Management Protocol (IGMP) is a communications protocol used to manage the membership of Internet Protocol multicast groups. IGMP is used by IP hosts and adjacent multicast routers to establish multicast group memberships.
There are three versions of IGMP, as defined by "Request for Comments" (RFC) documents of the Internet Engineering Task Force (IETF). IGMP v1 is defined by RFC 1112, IGMP v2 is defined by RFC 2236 and IGMP v3 is defined by RFC 3376.

IGMP snooping is a feature that allows the switch to "listen in" on the IGMP protocol conversation between hosts and routers.

The IGMP snooping switch hears an IGMP report from a host with a given multicast group address. It adds the host's port number to the multicast list for that group, and when the switch hears an IGMP Leave, it removes the host's port from the table entry.

Finally, switch will only forward multicast traffic to the hosts interested in that traffic. Therefore, this function can effectively reduce multicast traffic.

Hardware-based IGMP Snooping

The DM9016 supports IGMP v1/v2 snooping and the maximal group is 16 without any software effort.

The DM9016 automatically manipulates and updates IGMP membership table and Multicast table according to IGMP control packets, such as membership report and leave.

If IGMP membership table is full, the later incoming IGMP Membership Report (Join) packet will be ignored and the group address won't be registered into multicast address table. After that, the unregistered IP multicast packets (the destination MAC address can not be found in the multicast address table) will be treated as normal multicast packets by default. The additional forwarding control method can see the register Reg78H.[6:5].

The DM9016 supports router ports auto-detect and auto-aging mechanism. The port which receives IGMP Query packets will be treated as router port by default. The router port also can be define as static one by user (see Reg78H.4) and the port map of the router port can be programmed at Reg79H.[2:0]. Keep in mind that the uP port (port 3) is never treated as router port. The DM9016 leaves the router port if the time (Router Present Timeout, 400sec by default) is expired that the port never receives IGMP Query during this period.

If receiving V1REPORT or V2REPORT (group join), DM9016 creates new or updates the entry. If receiving LEAVE, DM9016 deletes the entry directly when Fast Leave is enabled, or waiting until timeout.

DM9016 removes the entry that was never updated after the timer of host timeout (Group Membership Interval) is expired. This timer is programmable in DM9016 and defined by RFC 2236 as ((the Robustness Variable) times (the Query Interval)) plus (one Query Response Interval). The setting of the Robustness Variable and the Query Interval can see Reg7AH and Reg7BH.

9.2.18 Port Security

DM9016 supports three types of port security function on each port, see the Port Security & STP Register (Reg6CH.[1:0]).

(1). First Lock:

The DM9016 locks the source MAC address of first received packet on the port and the disables the learning function in this mode.

After that, on detecting incoming packet, the DM916 compares source MAC address of incoming with the locked one. The DM9016 forwards the packet if match, or drops by default.

If port's link status is changed, the first received packet would be locked again after link on. It's noticeable that the previous one was kept in address table until aging out or removed by user.

(2). First Link Lock:
The lock scheme is same as first lock except that don't lock again when link status is changed.

(3). Assign Lock:

The DM9016 allows user to assign the locked entries by programming instead of dynamic learning. The port's learning function is disabled in this mode.

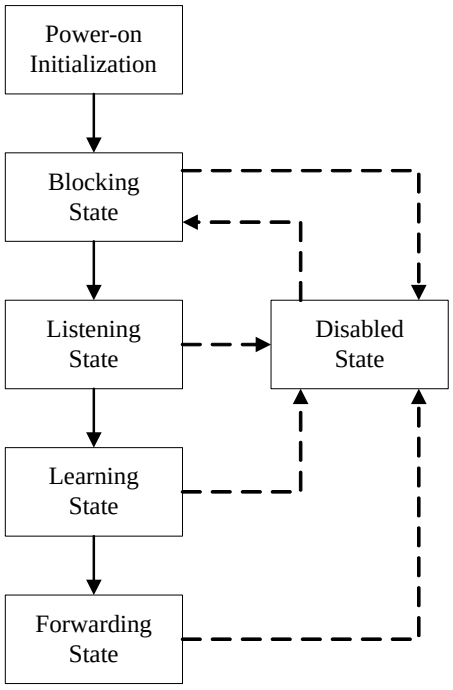
9.2.19 IPv6 MLD Snooping

The DM9016 forwards the IPv6 Multicast Listener Discovery (MLD) packets to the processor port when MLD Snooping is enabled and the MLD packets meet following scenario:

- IPv6 Multicast packets.
- The Hop Limit in IPv6 header is 1.
- The Next Header in IPv6 header is 0x3A (ICMPv6) or 0x00 (and next header of hop-by-hop option header is 0x3A).
- The Type in ICMP header is 0x82 (Multicast Listener Query), 0x83 (Multicast Listener Report) or 0x84 (Multicast Listener Done).

9.2.20 Spanning Tree Protocol Support

The DM9016 supports Spanning Tree Protocol and provides four types of port state, Forwarding, Disable, Learning and Blocking/Listening, see the Port Security & STP Register (Reg6CH.[1:0]). This function needs the cooperation n with external CPU. The following figure is the port state diagram of Spanning Tree Protocol.



(1). Disable State:

- **Setting:** Reg6CH[5:4] = 2'b01
- **Description:** The port will neither receive nor transmit any packets. Learning is disabled.
- **Software Action:** None.

(2). Blocking State:

- **Setting:** Reg6CH[5:4] = 2'b11
- **Description:** Only the BPDUs or overriding packet will be received and transmitted. Leaning is disabled.
- **Software Action:** In order to establish spanning tree, the receiving BPDUs will be forward to processor port but the processor should not send BPDUs to the port in this state.

(3). Listening State:

- **Setting:** Reg6CH[5:4] = 2'b11
- **Description:** Only the BPDUs and overriding packet will be received and transmitted. Leaning is disabled.
- **Software Action:** The receiving BPDUs will be forward to processor port and the processor can send BPDUs to the port in this state.

(4). Learning State:

- **Setting:** Reg6CH[5:4] = 2'b10
- **Description:** Only the BPDUs and overriding packet will be received and transmitted. Leaning is enabled.
- **Software Action:** The receiving BPDUs will be forward to processor port and the processor can send BPDUs to the port in this state.

(5). Forwarding State:

- **Setting:** Reg6CH[5:4] = 2'b00
- **Description:** The port participates in frame relay, learning, and STA calculation.
- **Software Action:** The receiving BPDUs will be forward to processor port and the processor can send BPDUs to the port in this state.

9.3 MII Interface

9.3.1 MII data interface

The DM9016 port 2 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the DM9016 port 2 and external device (a PHY or a MAC in reverse MII).

- TXD2 (transmit data) is a nibble (4 bits) of data that are driven by the DM9016 synchronously with respect to TXC2. For each TXC2 period, which TXE2 is asserted, TXD2 (3:0) are accepted for transmission by the external device.
- TXC2 (transmit clock) from the external device is a continuous clock that provides the timing reference for the transfer of the TXE2, TXD2. The DM9016 can drive 25MHz clock if it is configured to reversed MII mode.
- TXE2 (transmit enable) from the DM9016 port 2 MAC indicates that nibbles are being presented on the MII for transmission to the external device.

- RXD2 (receive data) is a nibble (4 bits) of data that are sampled by the DM9016 port 2 MAC synchronously with respect to RXC2. For each RXC2 period which RXDV2 is asserted, RXD2 (3:0) are transferred from the external device to the DM9016 port 2 MAC reconciliation sub layer.
- RXC2 (receive clock) from external device to the DM9016 port 2 MAC reconciliation sub layer is a continuous clock that provides the timing reference for the transfer of the RXDV2, RXD2, and RXER2 signals.
- RXDV2 (receive data valid) input from the external device to indicates that the external device is presenting recovered and decoded nibbles to the DM9016 port 2 MAC reconciliation sub layer. To interpret a receive frame correctly by the reconciliation sub layer, RXDV2 must encompass the frame, starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RXER2 (receive error) input from the external device is synchronously with respect to RXC2. RXER2 will be asserted for 1 or more clock periods to indicate to the reconciliation sub layer that an error was detected somewhere in the frame being transmitted from the external device to the DM9016 port 2 MAC.
- CRS2 (carrier sense) is asserted by the external device when either the transmit or receive medium is non-idle, and de-asserted by the external device when the transmit and receive medium are idle. The CRS2 can also in output mode when the DM9016 port 2 is configured to reversed MII mode.
- COL2 (collision detection) is asserted by the external device, when both the transmit and receive medium is non-idle, and de-asserted by the external device when the either transmit or receive medium are idle. The COL2 can also in output mode when the DM9016 port 2 is configured to reversed MII mode.

9.3.2 MII Serial Management

The MII serial management interface consists of a data interface, basic register set in DM9016 port 0 and 1, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, include internal two ports, get status and error information, and determine the type and capabilities of the attached PHY device(s). The DM9016 default is polling 3 ports basic registers 0, 1, 4, and 5 to get the link, duplex, and speed status automatically. Alternatively, the DM9016 can be programmed to read or write any registers of 3 ports by section 6.8~11 CSR B, C, D, and E.

The DM9016 management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, 18, 21, 22, 23 and 24~27.

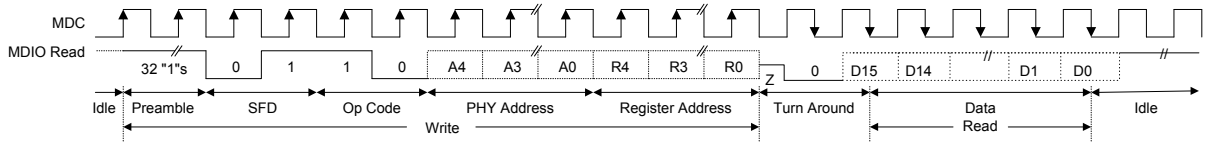
In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP) :< 10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

9.3.3 Serial Management Interface

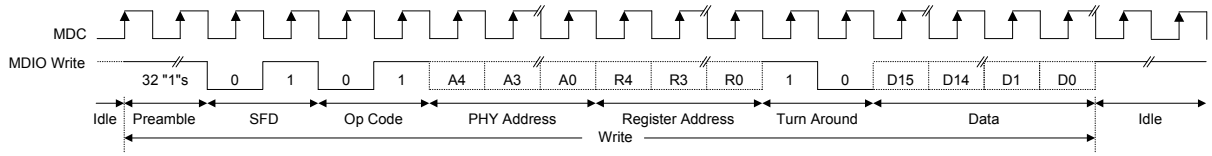
The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals.

The MDIO pin is bi-directional and may be shared by up to 32 devices.

9.3.4 Management Interface - Read Frame Structure



9.3.5 Management Interface - Write Frame Structure



9.4 Internal PHY functions

9.4.1 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.4.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

9.4.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.4.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

9.4.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base -TX transmission over Category-5 unshielded twisted pair cable.

9.4.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic one event.

9.4.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.4.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

9.4.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.4.2.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.4.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.4.2.3 MLT-3 to NRZI Decoder

The DM9016 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.4.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.4.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.4.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.4.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.4.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected and subsequent data is aligned on a fixed boundary.

9.4.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.4.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9016 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.4.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.4.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during receive operations.

9.4.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

10. DC and AC Electrical Characteristics

10.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC3	3.3V Supply Voltage	3.135	3.6	V	
VCCI	1.8V core power supply	1.71	1.95	V	
AVDD3	Analog power supply 3.3V	3.135	3.6	V	
AVDDI	Analog power supply 1.8V	1.71	1.95	V	
V_{IN}	DC Input Voltage (VIN)	3.135	3.6	V	
T_{STG}	Storage Temperature range	-65	+150	°C	
T_A	Ambient Temperature	0	+70	°C	
L_T	Lead Temperature (TL, soldering, 10 sec.).	-	+260	°C	Lead-free Device

10.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VCC3	3.3V Supply Voltage	3.135	3.30	3.465	V	
VCCI	1.8V core power supply	1.71	1.80	1.89	V	
AVDD3	Analog power supply 3.3V	3.135	3.30	3.465	V	
AVDDI	Analog power supply 1.8V	1.71	1.80	1.89	V	
P_D (Power Dissipation)	100BASE-TX	-	230	-	mA	1.8V only
		-	70	-	mA	3.3V only
	10BASE-TX		140		mA	TX idle, 1.8V only
			250		mA	50% utilization, 1.8V only
			360		mA	100% utilization, 1.8V only
			30		mA	3.3V only
	Auto-negotiation or cable off		170		mA	1.8V only
			40		mA	3.3V only

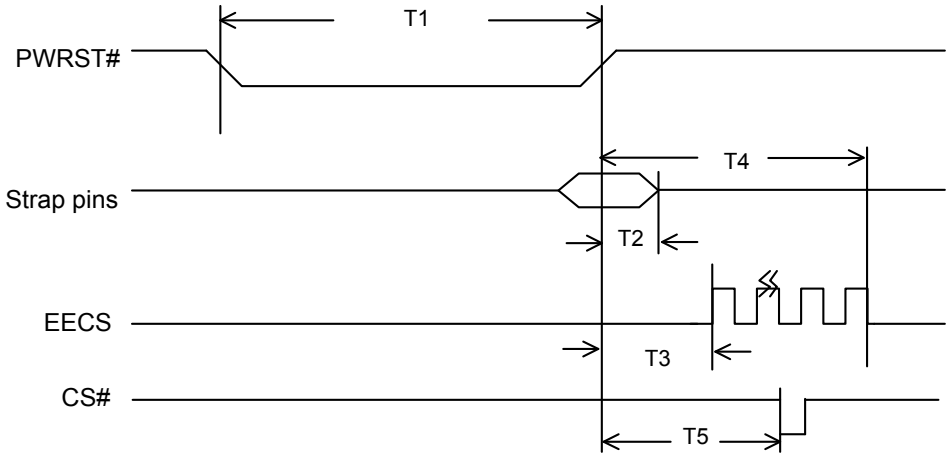
10.3 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
VIL	Input Low Voltage	-	-	0.8	V	Vcond1
VIH	Input High Voltage	2.0	-	-	V	Vcond1
IIL	Input Low Leakage Current	-1	-	-	uA	VIN = 0.0V, Vcond1
IIH	Input High Leakage Current	-	-	1	uA	VIN = 3.3V, Vcond1
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA
Receiver						
VICM	RX+/RX- Common Mode Input Voltage	-	1.8	-	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	Absolute Value

Note: Vcond1 = VCC3 = 3.3V, VCCI = 1.8V, AVDD3 = 3.3V, AVDDI = 1.8V.

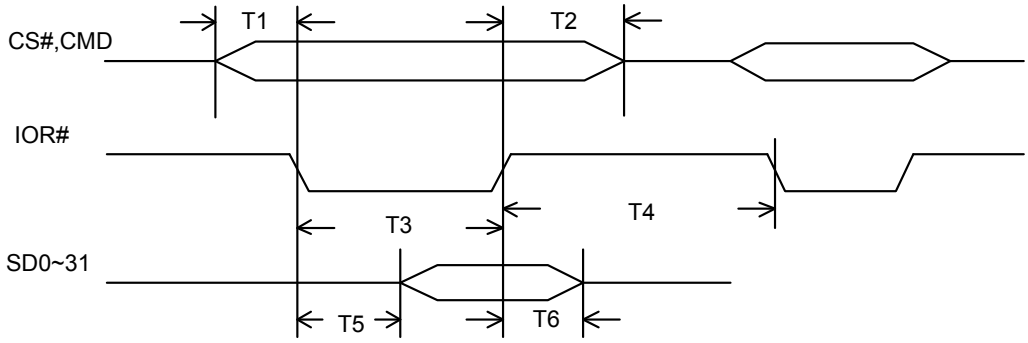
10.4 AC characteristics

10.4.1 Power On Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	PWRST# Low Period	1	-	-	ms	-
T2	Strap pin hold time with PWRST#	40	-	-	ns	-
T3	PWRST# high to EECS high	-	5	-	us	-
T4	PWRST# high to EECS burst end	-	--	4	ms	-
T5	PWRST# high to CS# available	--	400	--	us	-

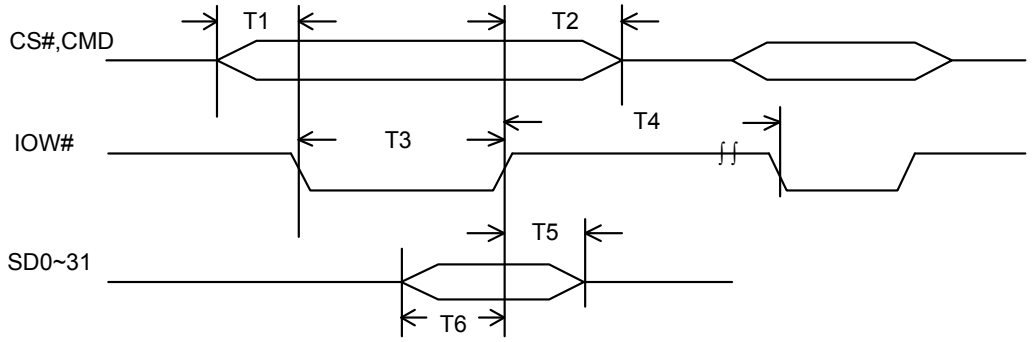
10.4.2 Processor I/O Read Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CS#,CMD valid to IOR# valid	5			ns
T2	IOR# invalid to CS#,CMD invalid	5			ns
T3	IOR# width	20			ns
T4	IOR# invalid to next IOR#/IOW# valid When read DM9016 register	2			clk*
T4	IOR# invalid to next IOR#/IOW# valid When read DM9016 memory with F0h register	4			clk*
T3+T4	IOR# invalid to next IOR#/IOW# valid When read DM9016 memory with F2h register	1			clk*
T5	System Data(SD) Delay time			25	ns
T6	IOR# invalid to System Data(SD) invalid			10	ns

Note: the Unit: clk is under the internal system clock 50MHz..

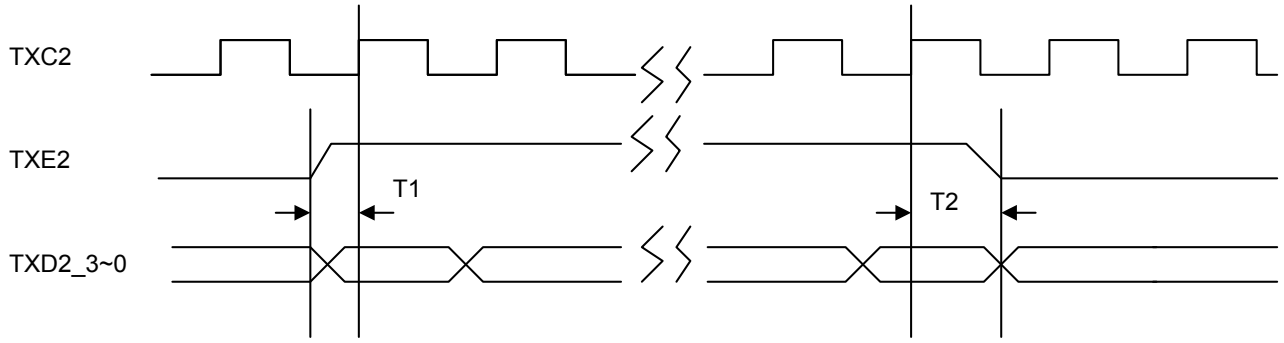
10.4.3 Processor I/O Write Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CS#,CMD valid to IOW# valid	5			ns
T2	IOW# Invalid to CS#,CMD Invalid	0			ns
T3	IOW# Width	20			ns
T4	IOW# Invalid to next IOW#/IOR# valid When write DM9016 INDEX port	1			clk*
T4	IOW# Invalid to next IOW#/IOR# valid When write DM9016 DATA port	2			clk*
T5	System Data(SD) Hold Time	3			ns
T6	System Data(SD) Setup Time	5			ns
T3+T4	IOW# Invalid to next IOW#/IOR# valid When write DM9016 memory	1			clk*

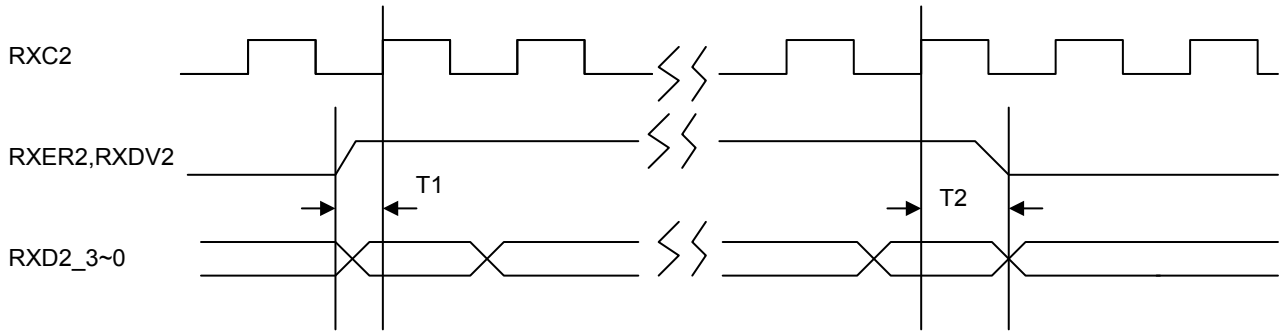
Note: the Unit: clk is under the internal system clock 50MHz.

10.4.4 Port 2 MII Interface Transmit Timing



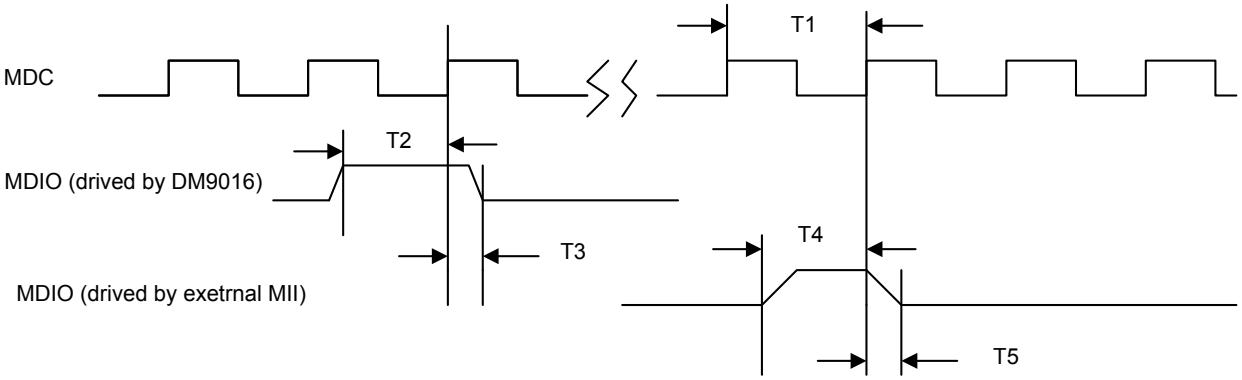
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	TXE2,TXD2_3~0 Setup Time		32		ns
T_2	TXE2,TXD2_3~0 Hold Time		8		ns

10.4.5 Port 2 MII Interface Receive Timing



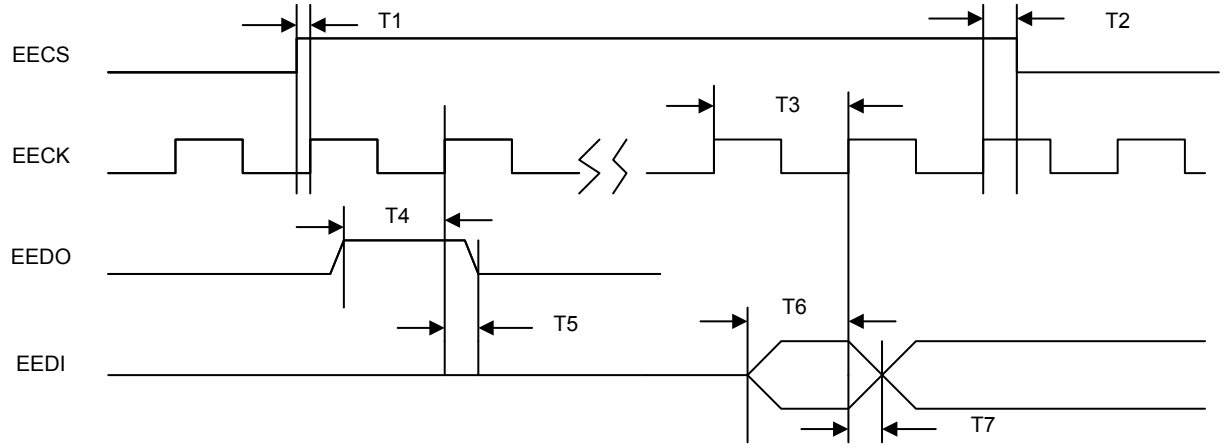
Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RXER2, RXDV2,RXD2_3~0 Setup Time	5			ns
T2	RXER2, RXDV2,RXD2_3~0 Hold Time	5			ns

10.4.6 MII Management Interface Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	MDC Frequency		0.52		MHz
T2	MDIO by DM9016 Setup Time		955		ns
T3	MDIO by DM9016 Hold Time		960		ns
T4	MDIO by External MII Setup Time	40			ns
T5	MDIO by External MII Hold Time	40			ns

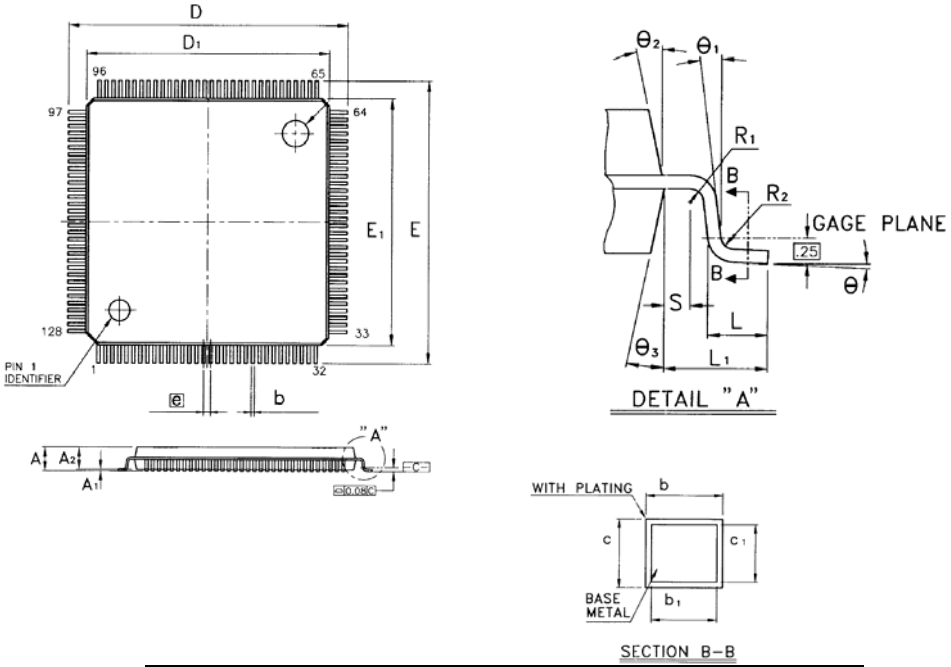
10.4.7 EEPROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EECS Setup Time		480		ns
T2	EECS Hold Time		2080		ns
T3	EECK Frequency		0.38		MHz
T4	EEDO Setup Time		460		ns
T5	EEDO Hold Time		2100		ns
T6	EEDI Setup Time	8			ns
T7	EEDI Hold Time	8			ns

11. Package Information

128 Pins LQFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	-	-	1.60		-	-	0.063
A_1	0.05	-	-		0.002	-	-
A_2	1.35	1.40	1.45		0.053	0.055	0.057
b	0.13	0.18	0.23		0.005	0.007	0.009
b_1	0.13	0.16	0.19		0.005	0.006	0.007
c	0.09	-	0.20		0.004	-	0.008
c_1	0.09	-	0.16		0.004	-	0.006
D	15.85	16.00	16.15		0.624	0.630	0.636
D_1	13.90	14.00	14.10		0.547	0.551	0.555
E	15.85	16.00	16.15		0.624	0.630	0.636
E_1	13.90	14.00	14.10		0.547	0.551	0.555
e	0.40 BSC				0.016 BSC		
L	0.45	0.60	0.75		0.018	0.024	0.030
L_1	1.00 REF				0.039 REF		
R_1	0.08	-	-		0.003	-	-
R_2	0.08	-	0.20		0.003	-	0.008
S	0.20	-	-		0.008	-	-
Θ	0°	3.5°	7°		0°	3.5°	7°
$Θ_1$	0°	-	-		0°	-	-
$Θ_2$	12° TYP				12° TYP		
$θ_3$	12° TYP				12° TYP		

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

12. Ordering Information

Part Number	Pin Count	Package
DM9016EP	128	LQFP (Pb-free)

*Support Lead-Free and Halogen-Free

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.