

# SN54ALS251, SN74ALS251 1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDAS215A – APRIL 1982 – REVISED DECEMBER 1994

- 3-State Version of the 'ALS151
- 3-State Outputs Interface Directly With System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

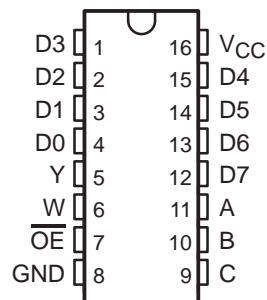
## description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature controlled complementary 3-state outputs.

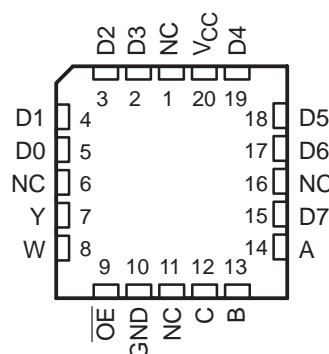
The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at the high-impedance state), the low impedance of the signal-enabled output drives the bus line to a high or low logic level. Both outputs are controlled by the output-enable ( $\overline{OE}$ ) input. The outputs are disabled when  $\overline{OE}$  is high.

The SN54ALS251 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS251 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS251 . . . J PACKAGE  
SN74ALS251 . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS251 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			$\overline{OE}$		
C	B	A		Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1, . . . D7 = the level of the respective D input

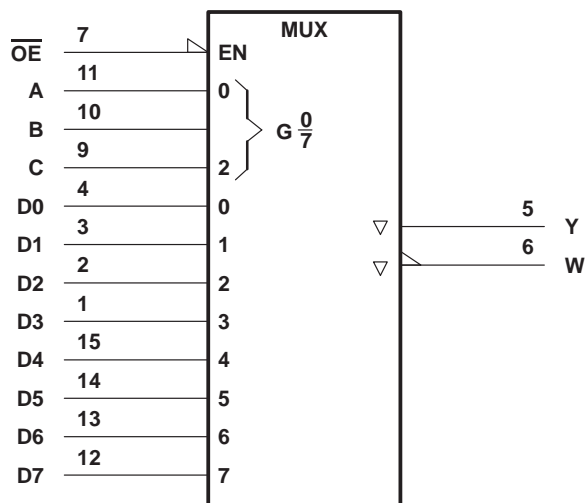
# SN54ALS251, SN74ALS251

## 1-OF-8 DATA SELECTORS/MULTIPLEXERS

### WITH 3-STATE OUTPUTS

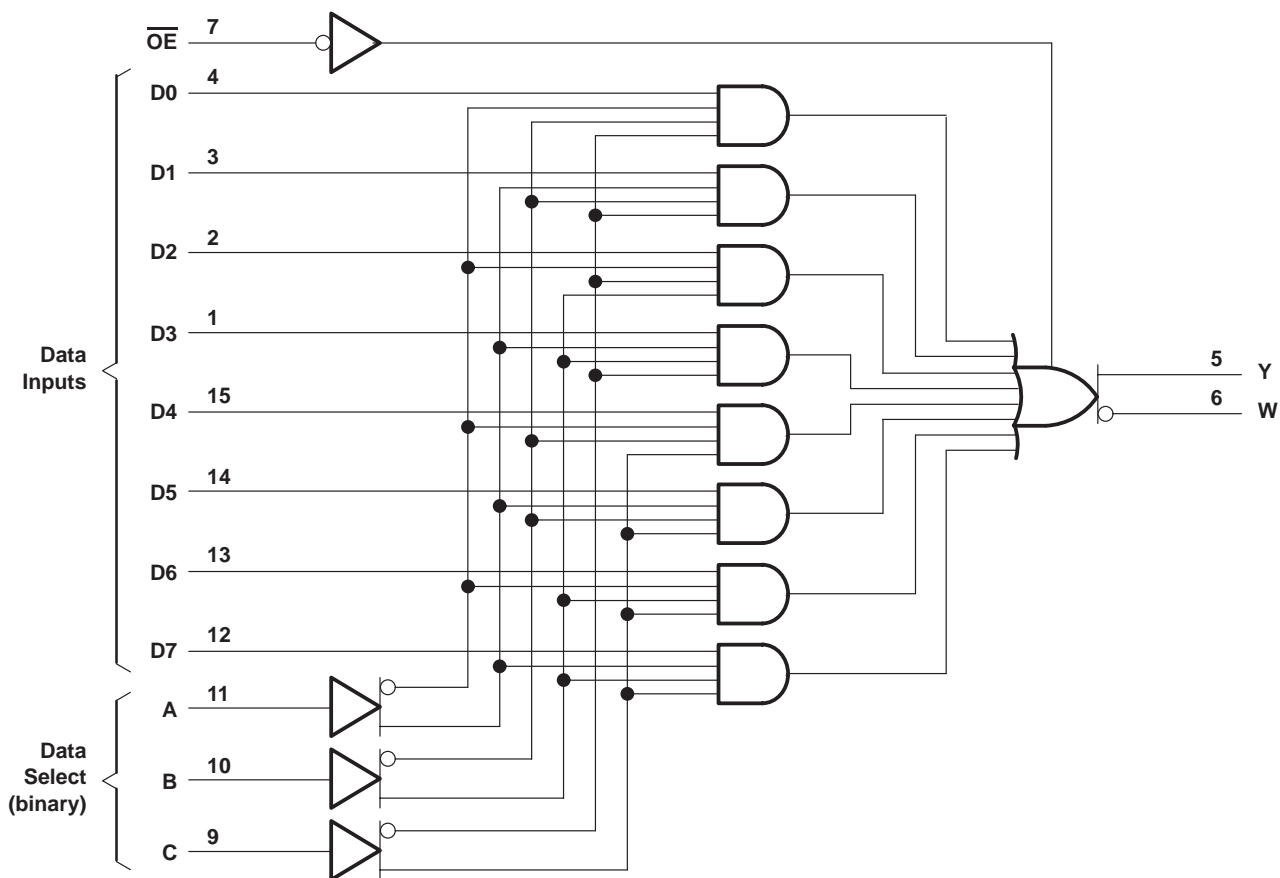
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

#### logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

# SN54ALS251, SN74ALS251

## 1-OF-8 DATA SELECTORS/MULTIPLEXERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS251	–55°C to 125°C
SN74ALS251	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN54ALS251			SN74ALS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS251			SN74ALS251			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA	−1.5			−1.5			V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −0.4 mA	V <sub>CC</sub> − 2			V <sub>CC</sub> − 2			V
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −1 mA	2.4	3.3					
			I <sub>OH</sub> = −2.6 mA				2.4	3.2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25			0.4	0.25	0.4	V
			I <sub>OL</sub> = 24 mA				0.35	0.5		
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	20			20			μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V	−20			−20			μA
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.1			0.1			mA
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	20			20			μA
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−0.1			−0.1			mA
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 4.5 V	−20	−112		−30	−112		mA
I <sub>CC</sub>	Enabled	V <sub>CC</sub> = 5.5 V	Inputs at GND	7		10	7		10	mA
	Disabled		Inputs at 4.5 V		9.4		14			

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



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### WITH 3-STATE OUTPUTS

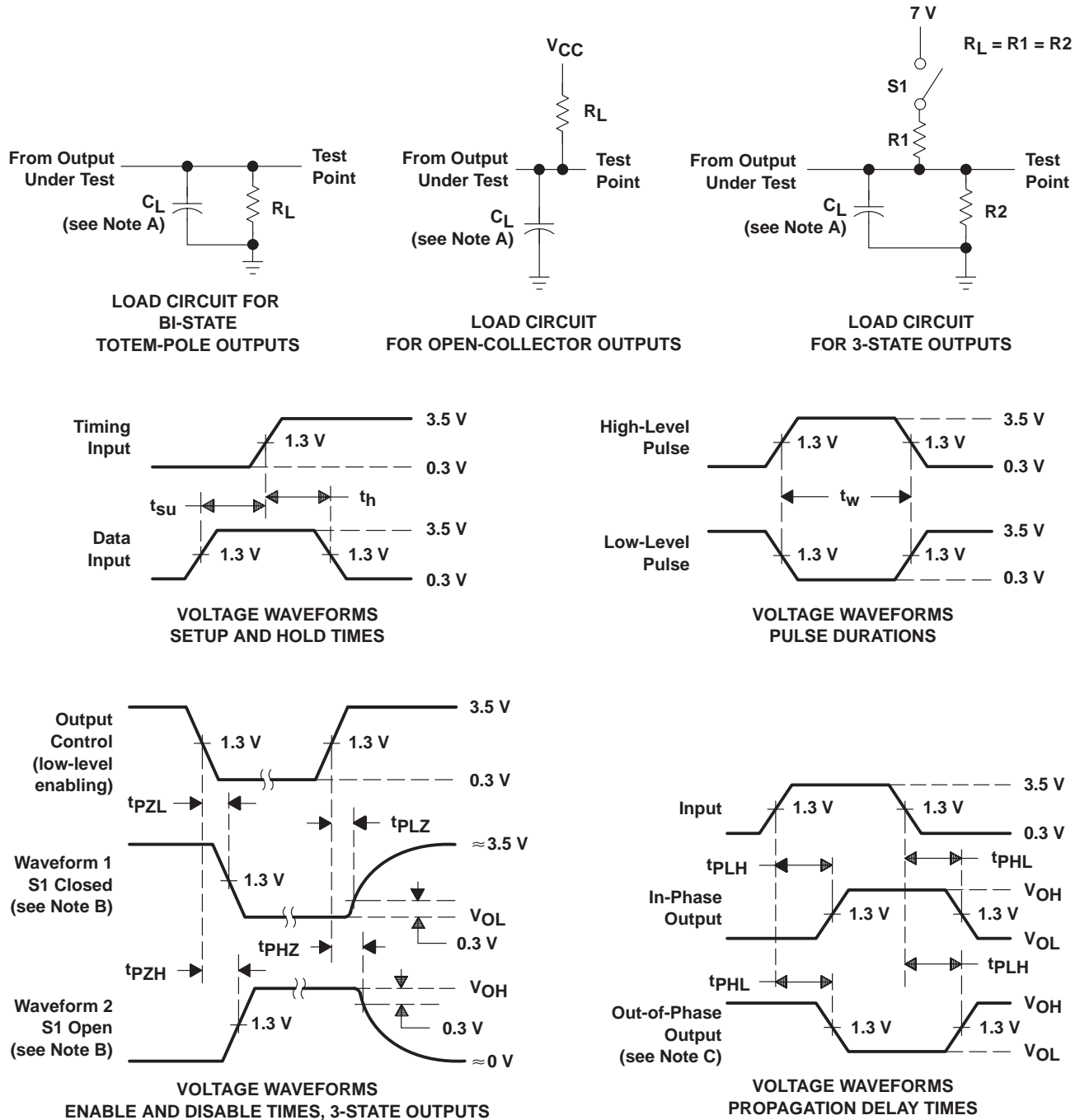
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#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS251		SN74ALS251		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A, B, or C	Y	1	21	5	18	ns
t <sub>PHL</sub>			7	34	8	24	
t <sub>PLH</sub>	A, B, or C	W	5	38	8	24	ns
t <sub>PHL</sub>			7	26	7	23	
t <sub>PLH</sub>	Any D	Y	2	15	2	10	ns
t <sub>PHL</sub>			3	23	3	15	
t <sub>PLH</sub>	Any D	W	3	25	3	15	ns
t <sub>PHL</sub>			3	20	3	15	
t <sub>PZH</sub>	$\overline{OE}$	Y	3	21	3	15	ns
t <sub>PZL</sub>			3	19	3	15	
t <sub>PZH</sub>	$\overline{OE}$	W	3	21	3	15	ns
t <sub>PZL</sub>			3	19	3	15	
t <sub>PZH</sub>	$\overline{OE}$	Y	2	12	2	10	ns
t <sub>PZL</sub>			1	18	1	10	
t <sub>PZH</sub>	$\overline{OE}$	W	2	12	2	10	ns
t <sub>PZL</sub>			1	18	1	10	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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