- **Members of the Texas Instruments _Widebus_™ Family**

- **State-of-the-Art _EPIC_-II_B_™ BiCMOS Design Significantly Reduces Power Dissipation**

- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**

- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16241A . . . WD PACKAGE
SN74ABT16241A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

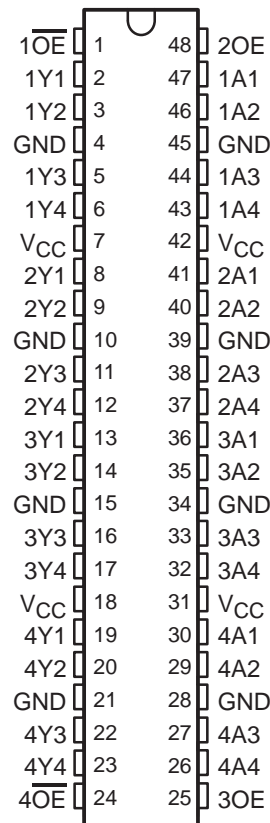| | | | | |
|---|---|---|---|---|
| 1$\overline{OE}$ | 1 | | 48 | 2OE |
| 1Y1 | 2 | | 47 | 1A1 |
| 1Y2 | 3 | | 46 | 1A2 |
| GND | 4 | | 45 | GND |
| 1Y3 | 5 | | 44 | 1A3 |
| 1Y4 | 6 | | 43 | 1A4 |
| $V_{CC}$ | 7 | | 42 | $V_{CC}$ |
| 2Y1 | 8 | | 41 | 2A1 |
| 2Y2 | 9 | | 40 | 2A2 |
| GND | 10 | | 39 | GND |
| 2Y3 | 11 | | 38 | 2A3 |
| 2Y4 | 12 | | 37 | 2A4 |
| 3Y1 | 13 | | 36 | 3A1 |
| 3Y2 | 14 | | 35 | 3A2 |
| GND | 15 | | 34 | GND |
| 3Y3 | 16 | | 33 | 3A3 |
| 3Y4 | 17 | | 32 | 3A4 |
| $V_{CC}$ | 18 | | 31 | $V_{CC}$ |
| 4Y1 | 19 | | 30 | 4A1 |
| 4Y2 | 20 | | 29 | 4A2 |
| GND | 21 | | 28 | GND |
| 4Y3 | 22 | | 27 | 4A3 |
| 4Y4 | 23 | | 26 | 4A4 |
| 4$\overline{OE}$ | 24 | | 25 | 3OE |

### description

The 'ABT16241A devices are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT16241A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16241A is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**TEXAS INSTRUMENTS**

**FUNCTION TABLES**

| INPUTS | | OUTPUTS |
|---|---|---|
| 1OE, 4OE | 1A, 4A | 1Y, 4Y |
| L | H | H |
| L | L | L |
| H | X | Z |

| INPUTS | | OUTPUTS |
|---|---|---|
| 2OE, 3OE | 2A, 3A | 2Y, 3Y |
| H | H | H |
| H | L | L |
| L | X | Z |

## logic symbol†
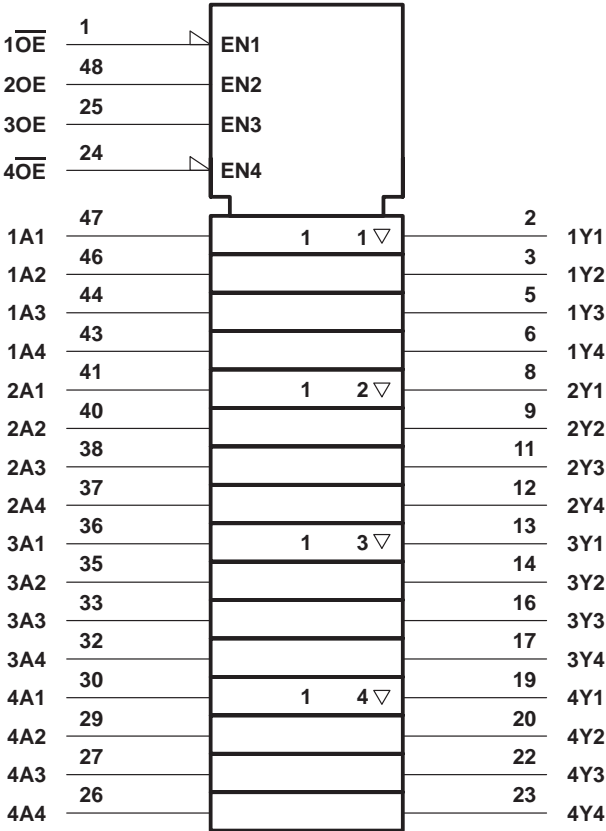


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)
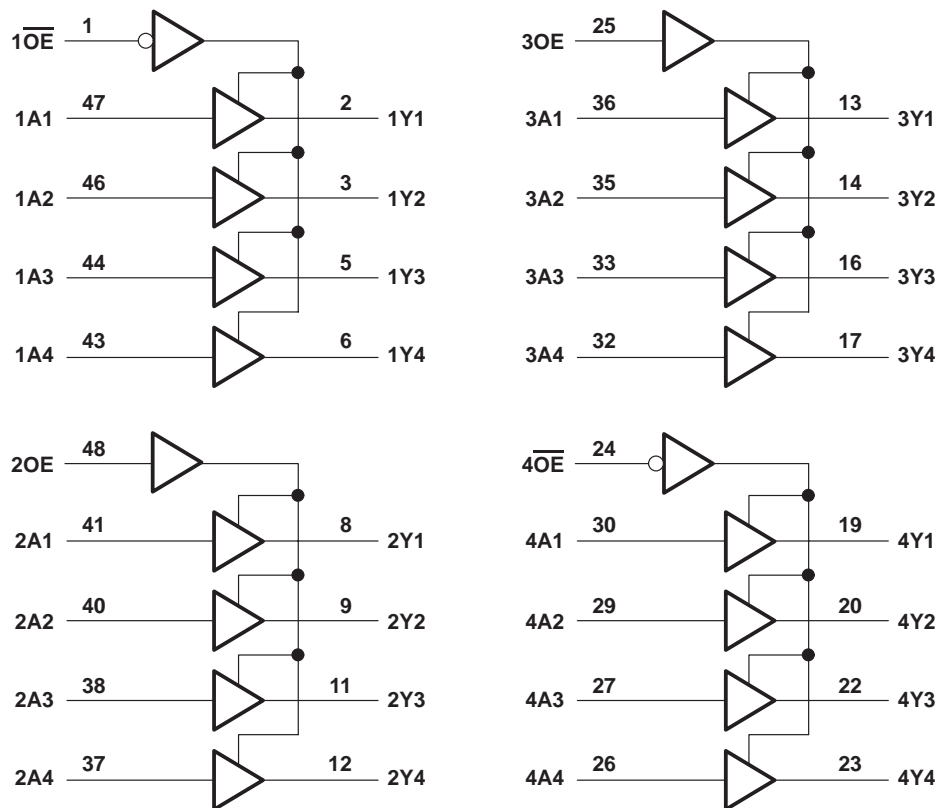


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ............................................................. –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ................................................... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ ................... –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT16241A ................................. 96 mA
SN74ABT16241A ................................. 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ..................................................... –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) .................................................. –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package ............................. 89°C/W
DGV package ................................. 93°C/W
DL package ................................. 94°C/W
Storage temperature range, $T_{stg}$ ........................................................ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

| | | | SN54ABT16241A | | SN74ABT16241A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABT16241A | | SN74ABT16241A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC} = 4.5$ V, | $I_I = -18$ mA | | | −1.2 | | −1.2 | | −1.2 | V |
| $V_{OH}$ | | $V_{CC} = 4.5$ V, | $I_{OH} = -3$ mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC} = 5$ V, | $I_{OH} = -3$ mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC} = 4.5$ V | $I_{OH} = -24$ mA | 2 | | | 2 | | | | |
| | | | $I_{OH} = -32$ mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL} = 64$ mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | | $V_{CC} = 5.5$ V, | $V_I = V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | μA |
| $I_{OZH}$ | | $V_{CC} = 5.5$ V, | $V_O = 2.7$ V | | | 10 | | 10 | | 10 | μA |
| $I_{OZL}$ | | $V_{CC} = 5.5$ V, | $V_O = 0.5$ V | | | −10 | | −10 | | −10 | μA |
| $I_{off}$ | | $V_{CC} = 0$, | $V_I$ or $V_O ≤ 4.5$ V | | | ±100 | | | | ±100 | μA |
| $I_{CEX}$ | | $V_{CC} = 5.5$ V, $V_O = 5.5$ V | Outputs high | | | 50 | | 50 | | 50 | μA |
| $I_O$‡ | | $V_{CC} = 5.5$ V, | $V_O = 2.5$ V | −50 | −100 | −180 | −50 | −180 | −50 | −180 | mA |
| $I_{CC}$ | | $V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | | 3 | | 3 | | 3 | mA |
| | | | Outputs low | | | 34 | | 34 | | 34 | |
| | | | Outputs disabled | | | 3 | | 3 | | 3 | |
| $\Delta I_{CC}$§ | Data inputs | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | Outputs enabled | | | 1 | | 1.5 | | 1 | mA |
| | | | Outputs disabled | | | 0.05 | | 1 | | 0.05 | |
| | Control inputs | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | |
| $C_i$ | | $V_I = 2.5$ V or 0.5 V | | | 3.5 | | | | | | pF |
| $C_o$ | | $V_O = 2.5$ V or 0.5 V | | | 7.5 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

![Texas Instruments logo]

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT16241A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | 0.9 | 2.7 | 3.4 | 0.9 | 3.8 | ns |
| $t_{PHL}$ | | | 0.9 | 2.7 | 3.9 | 0.9 | 4.6 | |
| $t_{PZH}$ | OE or $\overline{OE}$ | Y | 1.2 | 3.3 | 4.2 | 1.2 | 5.1 | ns |
| $t_{PZL}$ | | | 1.3 | 3.4 | 5.9 | 1.3 | 7 | |
| $t_{PHZ}$ | OE or $\overline{OE}$ | Y | 1.5 | 4.1 | 5.5 | 1.5 | 7 | ns |
| $t_{PLZ}$ | | | 1.7 | 3.6 | 5.1 | 1.7 | 5.7 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT16241A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A | Y | 1 | 2.7 | 3.4 | 1 | 3.7 | ns |
| $t_{PHL}$ | | | 1 | 2.7 | 3.9 | 1 | 4.5 | |
| $t_{PZH}$ | OE or $\overline{OE}$ | Y | 1.2 | 3.3 | 4.2 | 1.2 | 5 | ns |
| $t_{PZL}$ | | | 1.3 | 3.4 | 5.9 | 1.3 | 6.9 | |
| $t_{PHZ}$ | OE or $\overline{OE}$ | Y | 1.5 | 4.1 | 5.2 | 1.5 | 6.2 | ns |
| $t_{PLZ}$ | | | 1.7 | 3.6 | 5.1 | 1.7 | 5.6 | |

TEXAS
INSTRUMENTS

## PARAMETER MEASUREMENT INFORMATION
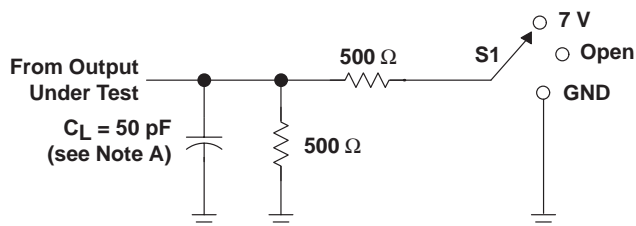
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |



**LOAD CIRCUIT**
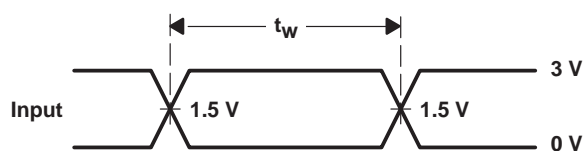
**VOLTAGE WAVEFORMS**
**PULSE DURATION**
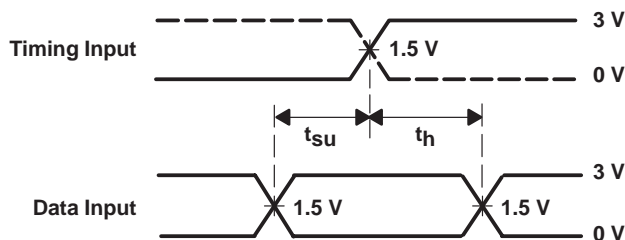
**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
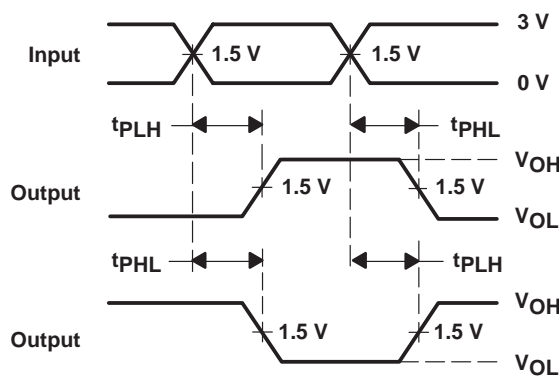
**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**
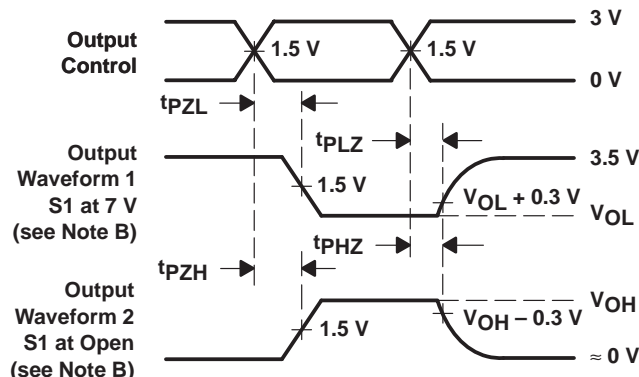
**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**