

# SN54ABT16500B, SN74ABT16500B 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS057G – DECEMBER 1990 – REVISED MAY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

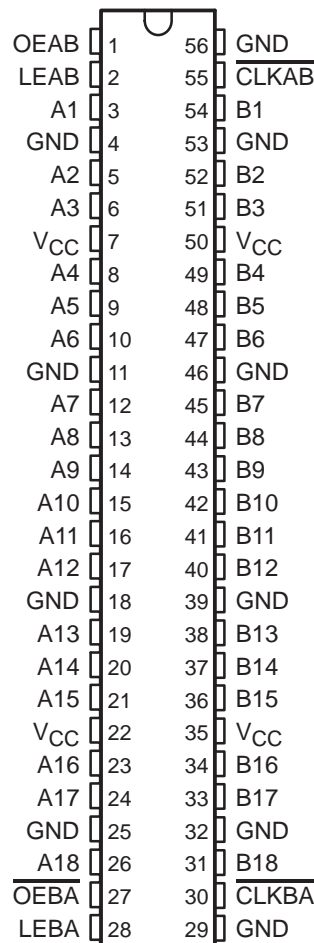
## description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

SN54ABT16500B . . . WD PACKAGE  
SN74ABT16500B . . . DGG OR DL PACKAGE  
(TOP VIEW)



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**TEXAS  
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# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### description (continued)

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT16500B is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT16500B is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	$B_0^{\ddagger}$
H	L	L	X	$B_0^{\S}$

† A-to-B data flow is shown: B-to-A flow is similar but uses  $\overline{OEBA}$ ,  $\overline{LEBA}$ , and  $\overline{CLKBA}$ .

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

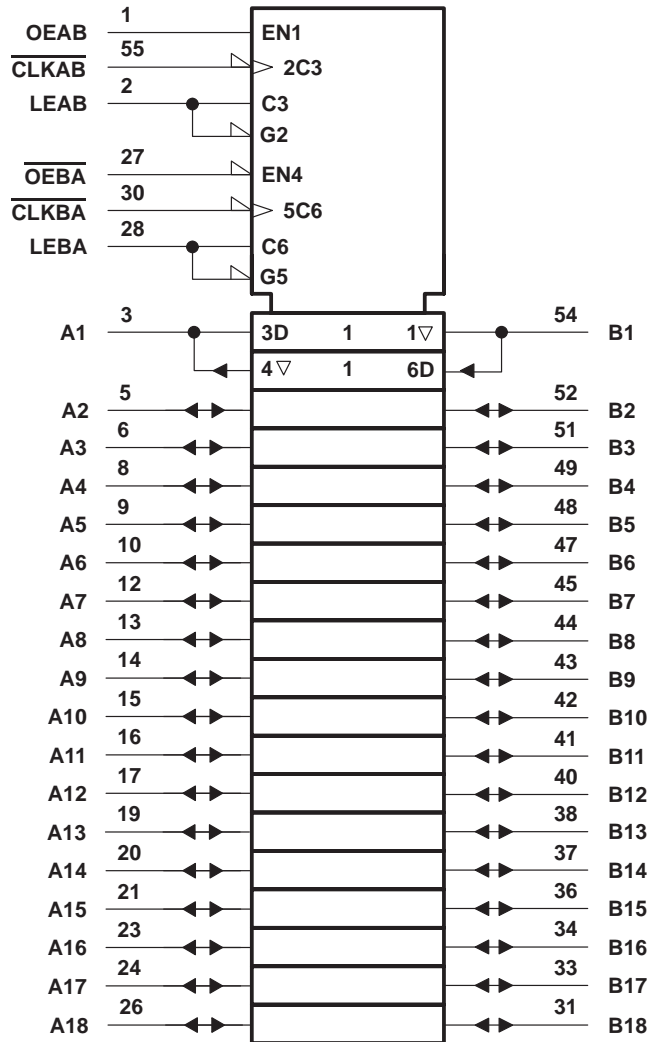
# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

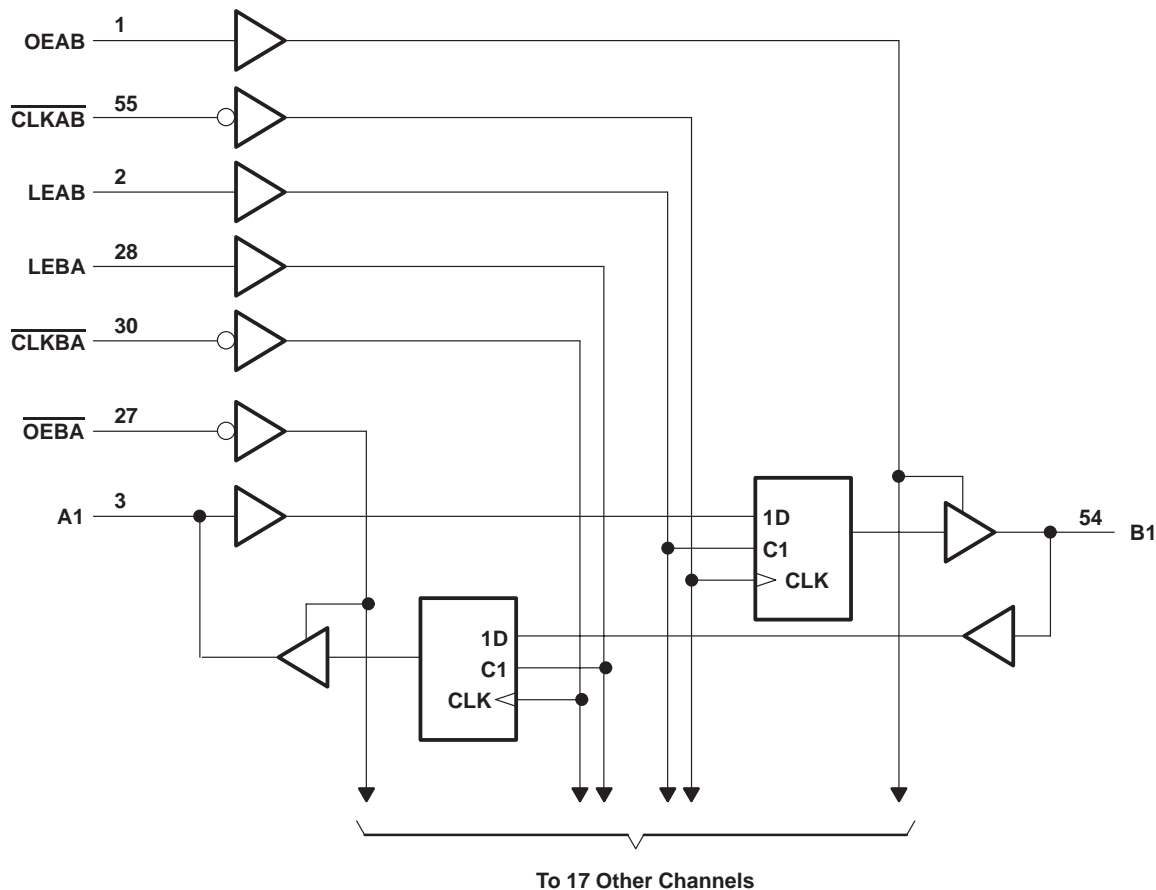
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## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16500B	96 mA
SN74ABT16500B	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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## recommended operating conditions (see Note 3)

			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current			–24		–32	mA
$I_{OL}$	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		$\mu$ s/V
$T_A$	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

# SN54ABT16500B, SN74ABT16500B

## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2				
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA	2*					2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA			0.55		0.55			V
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA			0.55*				0.55	
V <sub>hys</sub>				100						mV
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V, Outputs high			50		50		50	μA
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±20		±20		±20	
I <sub>O†</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>OZPU</sub> §		V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE}$ or OE = X			±50		±50		±50	μA
I <sub>OZPD</sub> §		V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE}$ or OE = X			±50		±50		±50	μA
I <sub>OZH</sub> ¶		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE}$ ≥ 2 V, OE ≤ 0.8 V#			10		10		10	μA
I <sub>OZL</sub> ¶		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE}$ ≥ 2 V, OE ≤ 0.8 V#			-10		-10		-10	μA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, Outputs high			3		3		3	mA
		I <sub>O</sub> = 0, Outputs low			36		36		36	
		V <sub>I</sub> = V <sub>CC</sub> or GND, Outputs disabled			3		3		3	
ΔI <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50		50		50	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			9					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This parameter is characterized, but not production tested.

¶ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

# For V<sub>CC</sub> between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

|| This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT16500B		SN74ABT16500B		UNIT
				MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
t <sub>w</sub> <sup>†</sup>	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t <sub>su</sub>	Setup time	A before CLKAB↓		3		3		ns
		B before CLKBA↓		3		3		
		A before LEAB↓ or B before LEBA↓	CLK high	1		1		
			CLK low	2.5		2.5		
t <sub>h</sub>	Hold time	A after CLKAB↓ or B after CLKBA↓		0		0		ns
		A after LEAB↓ or B after LEBA↓		2		2		

$^\dagger$  This parameter is characterized, but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16500B		SN74ABT16500B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150	200		150		150		MHz
$t_{\text{PLH}}$	A or B	B or A	1	2.5	3.6	1	4.2	1	4	ns
$t_{\text{PHL}}$			1	3.2	4.5	1	5.1	1	4.9	
$t_{\text{PLH}}$	LEAB or LEBA	B or A	1	3.2	4.5	1	5.6	1	5	ns
$t_{\text{PHL}}$			1	3.4	4.5	1	5.4	1	5	
$t_{\text{PLH}}$	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$	B or A	1	3.5	4.7	1	5.4	1	5.3	ns
$t_{\text{PHL}}$			1	3.5	4.7	1	5.4	1	5.3	
$t_{\text{PZH}}$	OEAB or $\overline{\text{OEBA}}$	B or A	1	3.4	4.6	1	5.3	1	5.1	ns
$t_{\text{PZL}}$			1.5	3.8	4.7	1.5	5.6	1.5	5.4	
$t_{\text{PHZ}}$	OEAB or $\overline{\text{OEBA}}$	B or A	1.5	4.5	5.7	1.5	6.9	1.5	6.5	ns
$t_{\text{PLZ}}$			1.4	3.4	4.7	1.4	5.8	1.4	5.4	

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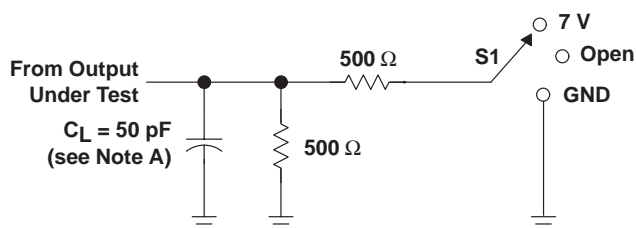
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## 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

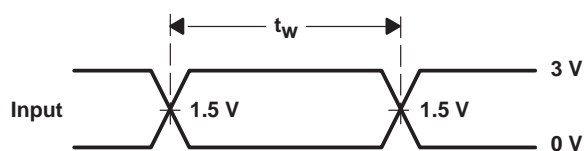
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#### PARAMETER MEASUREMENT INFORMATION

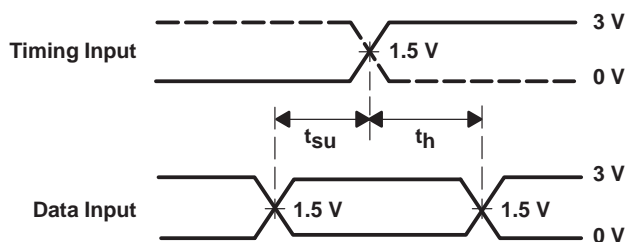


LOAD CIRCUIT

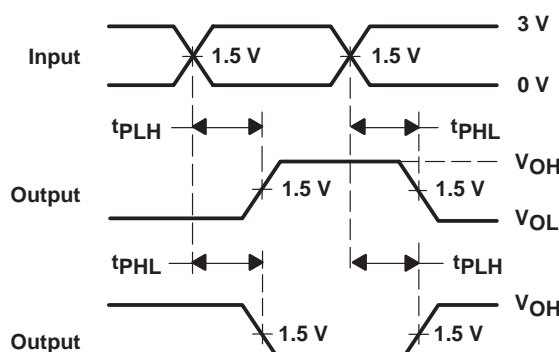
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



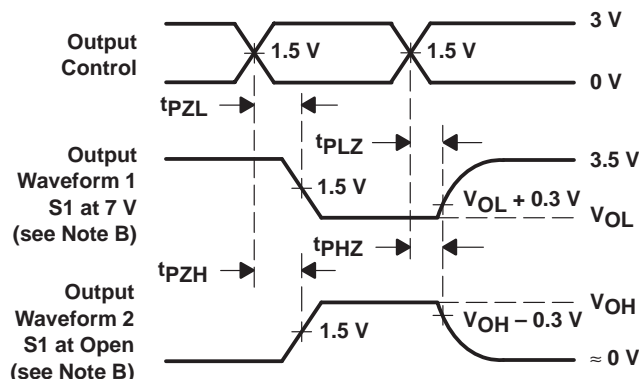
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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