

SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-II*[™] BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

description

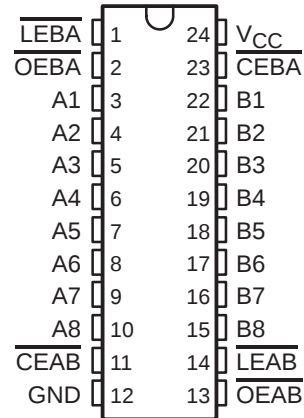
The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

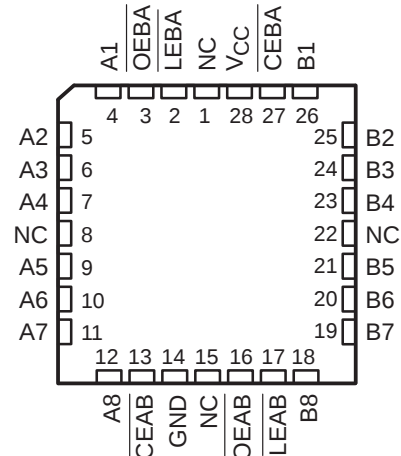
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT543A is characterized for operation from -40°C to 85°C .

SN54ABT543A . . . JT OR W PACKAGE
SN74ABT543A . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT543A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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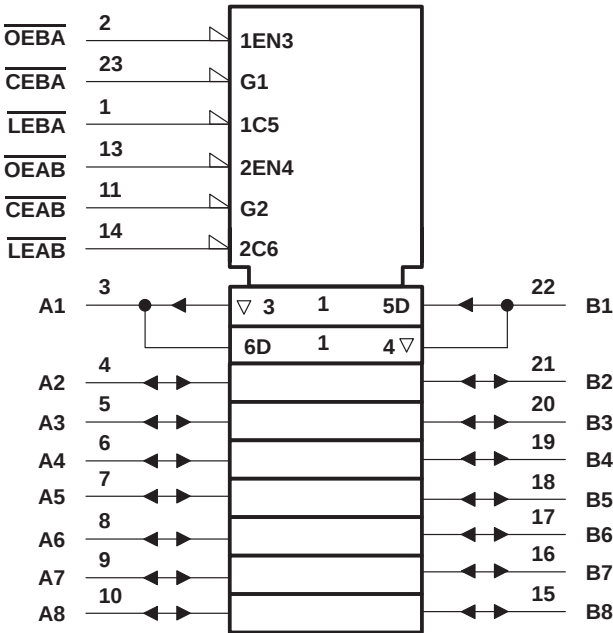
SN54ABT543A, SN74ABT543A
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

FUNCTION TABLE†				
INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.
‡ Output level before the indicated steady-state input conditions were established

logic symbols§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

SCBS157F – JANUARY 1991 – REVISED MAY 1997

The diagram illustrates the logic for the A1 channel. It features four 2-input AND gates at the top, each with one input from a channel select line (OEBA, CEBA, LEBA, OEAB, CEAB, LEAB) and another from a common bus. The outputs of these AND gates are connected to a central logic block. This block contains two comparators (C1, 1D) and two inverters. The central logic block has two inputs from the common bus and two outputs, A1 and B1. The outputs A1 and B1 are connected to the common bus. The central logic block is connected to the other six channels via a bus labeled "To Seven Other Channels".

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)		-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O		-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT543A		96 mA
SN74ABT543A		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		-18 mA
Output clamp current, I_{OK} ($V_O < 0$)		-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package		104°C/W
DW package		81°C/W
NT package		67°C/W
PW package		120°C/W
Storage temperature range, T_{Stg}		-65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT543A, SN74ABT543A

OCTAL REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

recommended operating conditions (see Note 3)

			SN54ABT543A		SN74ABT543A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT543A		SN74ABT543A		UNIT
			MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			–1.2		–1.2		–1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2				
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55		0.55			V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$			0.55*				0.55	
V_{hys}				100						mV
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND			± 1		± 1		± 1	μA
	A or B ports				± 100		± 100		± 100	
$I_{OZH}^{\ddagger}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			$10^{\S}$		$10^{\S}$		$10^{\S}$	μA
$I_{OZL}^{\ddagger}$		$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$			$-10^{\S}$		$-10^{\S}$		$-10^{\S}$	μA
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$			± 100				± 100	μA
I_{CEX}		$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$, Outputs high			50		50		50	μA
$I_O^{\P}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	–50*	–100	–180*	–50	–200	–50	–180	mA
I_{CC}	A or B ports	$V_{CC} = 5.5\text{ V}$, Outputs high		1	250*		350		250	μA
		$I_O = 0$, Outputs low		24	30*		34		30	mA
		$V_I = V_{CC}$ or GND, Outputs disabled		0.5	250*		350		250	μA
$\Delta I_{CC}^{\#}$		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	mA
C_i	Control inputs	$V_I = 2.5\text{ V}$ or 0.5 V			4					pF
C_{io}	A or B ports	$V_O = 2.5\text{ V}$ or 0.5 V			7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at $V_{CC} = 5\text{ V}$.

[‡] The parameters I_{OZH} and I_{OZL} include the input leakage current.

[§] This data sheet limit may vary among suppliers.

[¶] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[#] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT543A, SN74ABT543A
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SCBS157F – JANUARY 1991 – REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT543A		UNIT		
				$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$			MIN	MAX
				MIN	MAX			
t_W	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.5	3.5	ns		
t_{SU}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	High	2.5	2.5	ns		
			Low	3	3			
		Data before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	High	2.5	2.5			
			Low	3	3			
t_H	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	1	1	ns			
		Data after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	1	1				

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN74ABT543A		UNIT		
				$V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$			MIN	MAX
				MIN	MAX			
t_W	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.5	3.5	ns		
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	High	3.5	3.5	ns		
			Low	3	3			
		Data before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	High	3.5	3.5			
			Low	3	3			
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	0.5	0.5	ns			
		Data after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	0.5	0.5				

SN54ABT543A, SN74ABT543A

OCTAL REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT543A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.6 [†]	4.4	4.4	1.6 [†]	5.5	ns
t _{PHL}			1.6	4.4	5.1	1.6	6.2	
t _{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.6 [†]	4.1	5.1	1.6 [†]	6.6	ns
t _{PHL}			1.6	4.6	5.4	1.6	6.4	
t _{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	4.1	1.4	5.1	ns
t _{PZL}			2	5	4.9	2	5.8	
t _{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5 [†]	5.9	5.8	2.5 [†]	6.9	ns
t _{PLZ}			2.5 [†]	5.5	6.1	2.5 [†]	7.6	
t _{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	4.7	1.4	5.6	ns
t _{PZL}			2	5	5.7	2	6.2	
t _{PHZ}	CEBA or CEAB	A or B	3.2 [†]	5.9	6.5	3.2 [†]	7.3	ns
t _{PLZ}			2.5 [†]	5.5	6.7	2.5 [†]	7.8	

[†] This data sheet limit may vary among suppliers.

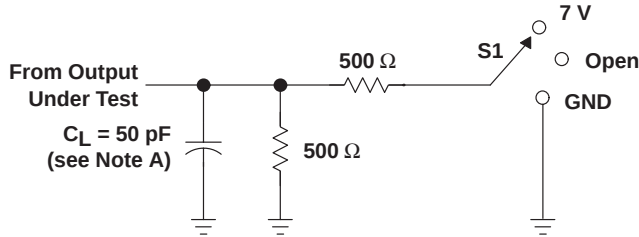
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT543A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.8 [†]	4.4	5.9	1.8 [†]	6.9	ns
t _{PHL}			1.9	4.4	5.9	1.9	6.9	
t _{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.5 [†]	4.1	5.6	1.5 [†]	6.6	ns
t _{PHL}			2.1	4.6	6.1	2.1	7.1	
t _{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
t _{PZL}			2.5	5	6.5	2.5	7.5	
t _{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5 [†]	5.9	7.4	2.5 [†]	8.4	ns
t _{PLZ}			2.5 [†]	5.5	7	2.5 [†]	8	
t _{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.9	5.4	1.4	6.4	ns
t _{PZL}			2.5	5	6.5	2.5	7.5	
t _{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2.9 [†]	5.9	7.4	2.9 [†]	8.4	ns
t _{PLZ}			2.4 [†]	5.5	7	2.4 [†]	8	

[†] This data sheet limit may vary among suppliers.

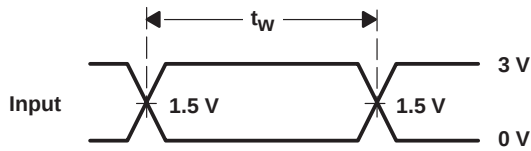


PARAMETER MEASUREMENT INFORMATION

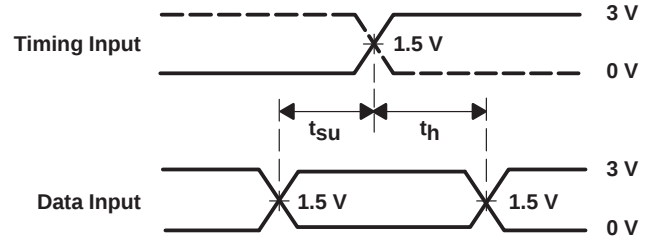


LOAD CIRCUIT

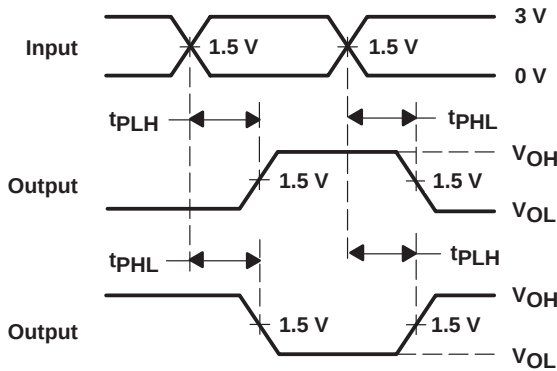
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



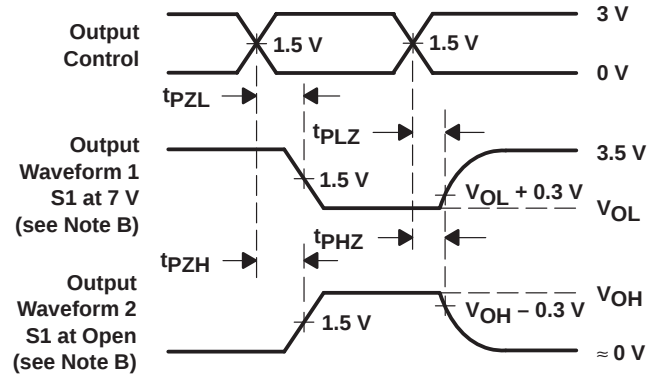
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9231402Q3A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-9231402QKA	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC
5962-9231402QLA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN74ABT543ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT543ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT543ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT543ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ABT543ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ABT543APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74ABT543APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT543APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT543AFK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ABT543AJT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ABT543AW	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

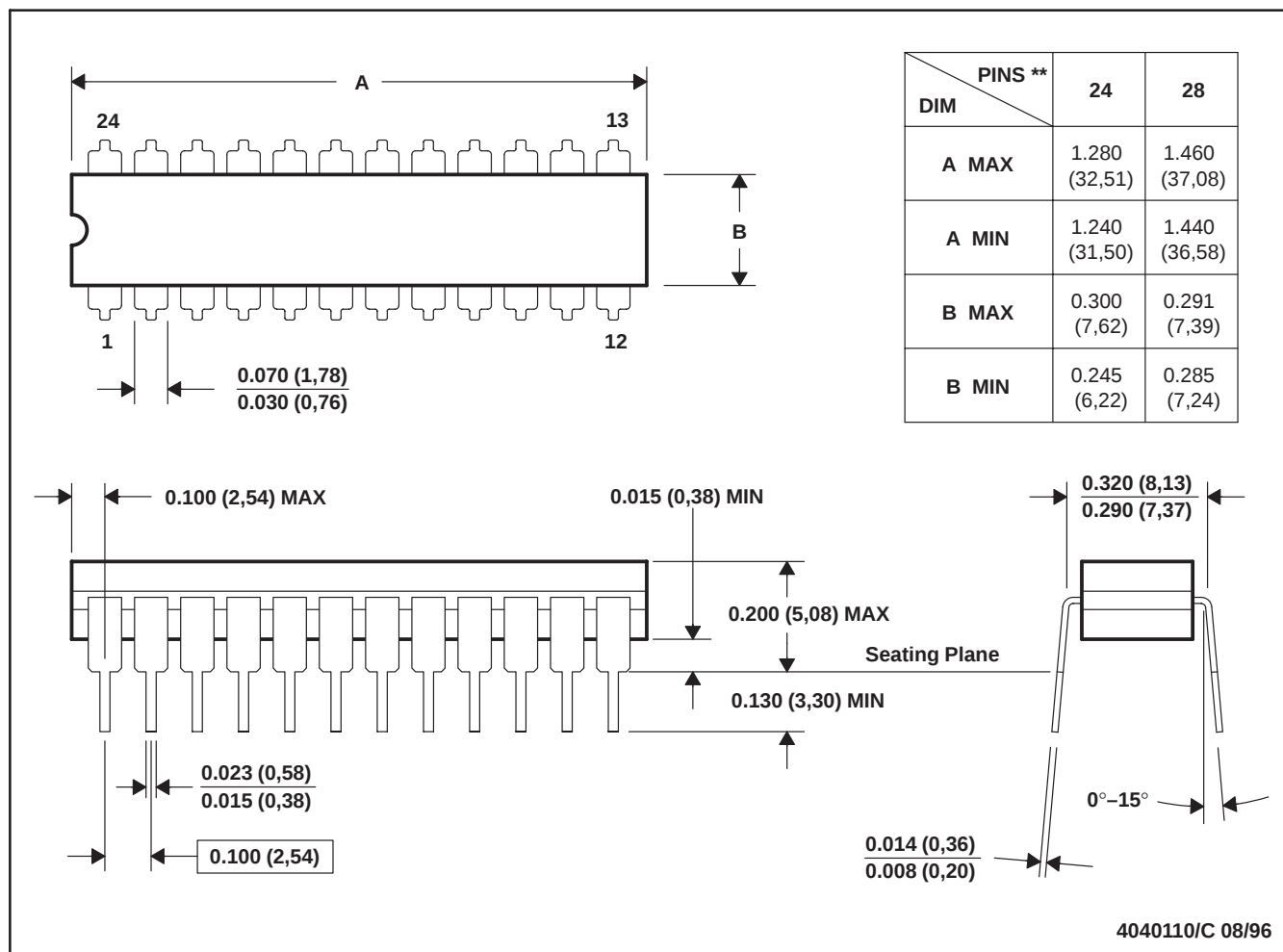
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JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

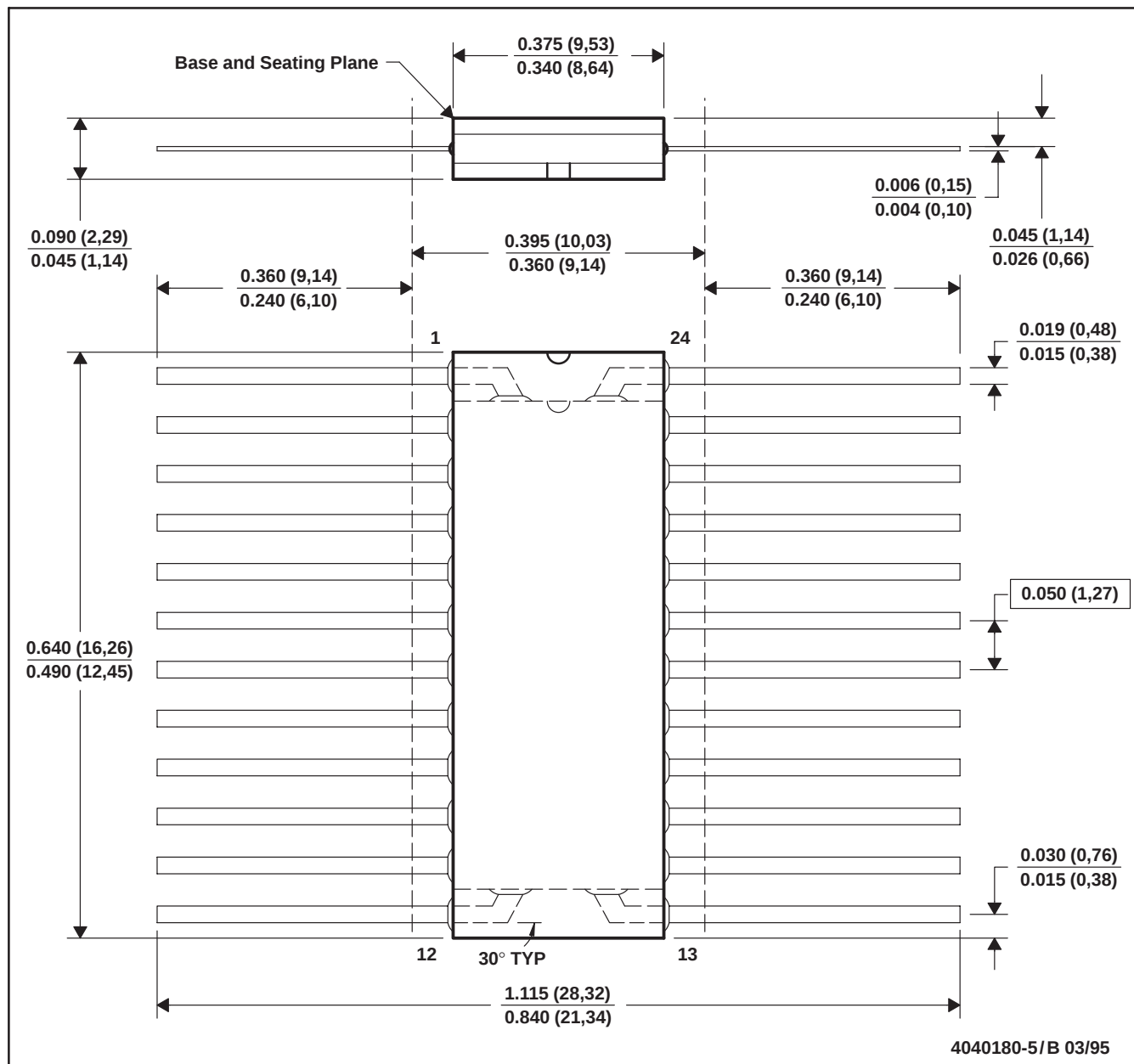
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

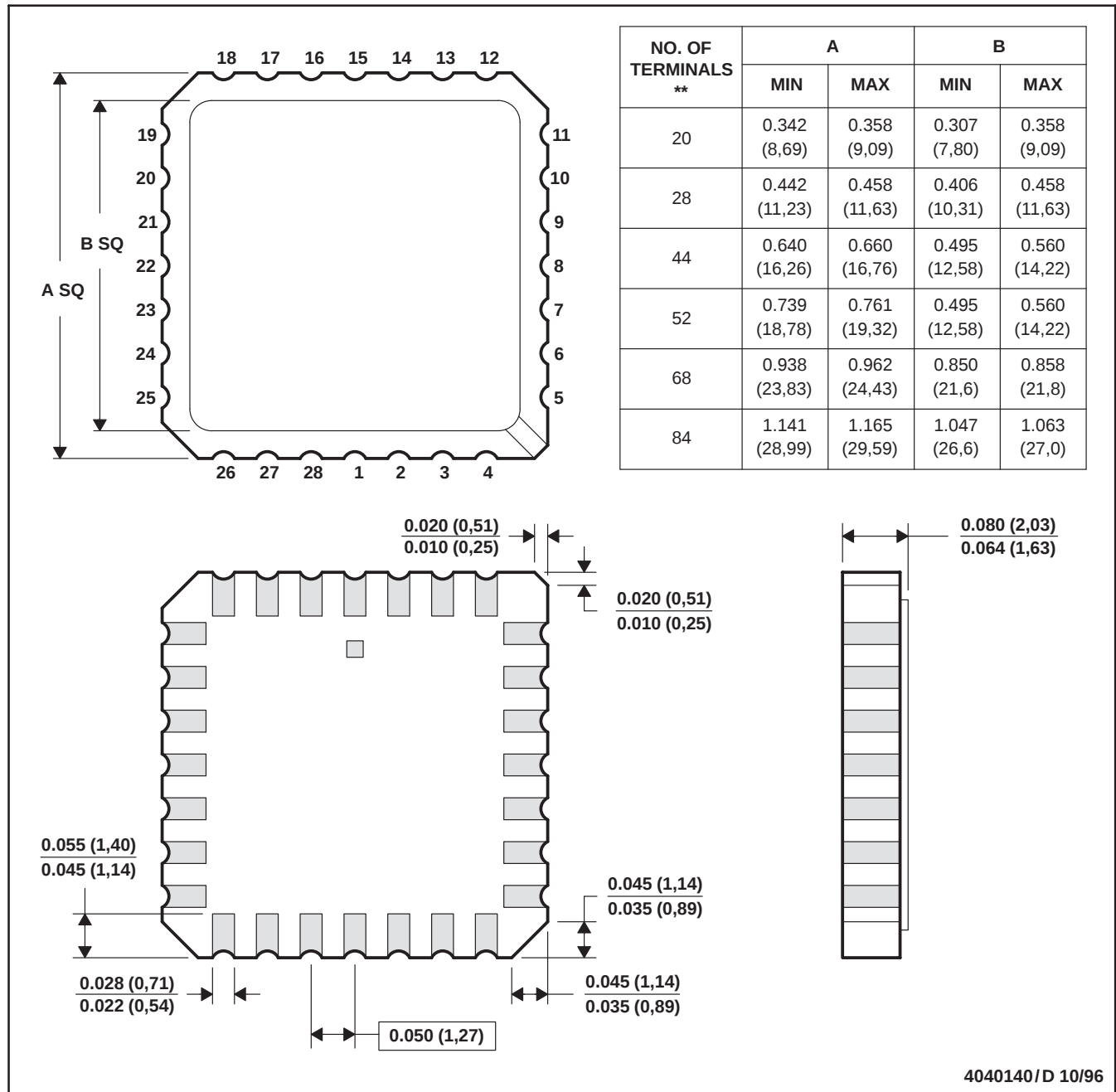


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

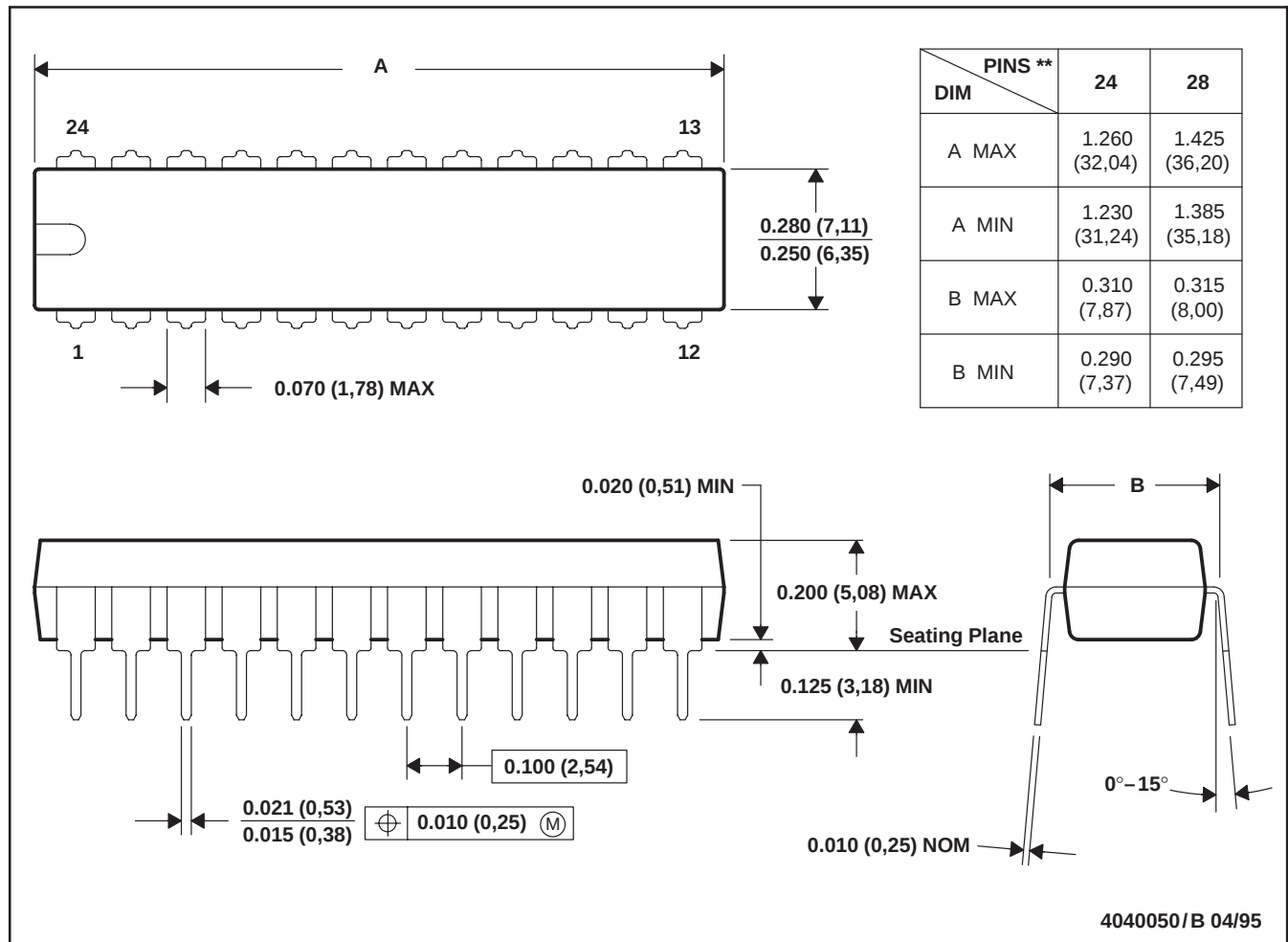


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

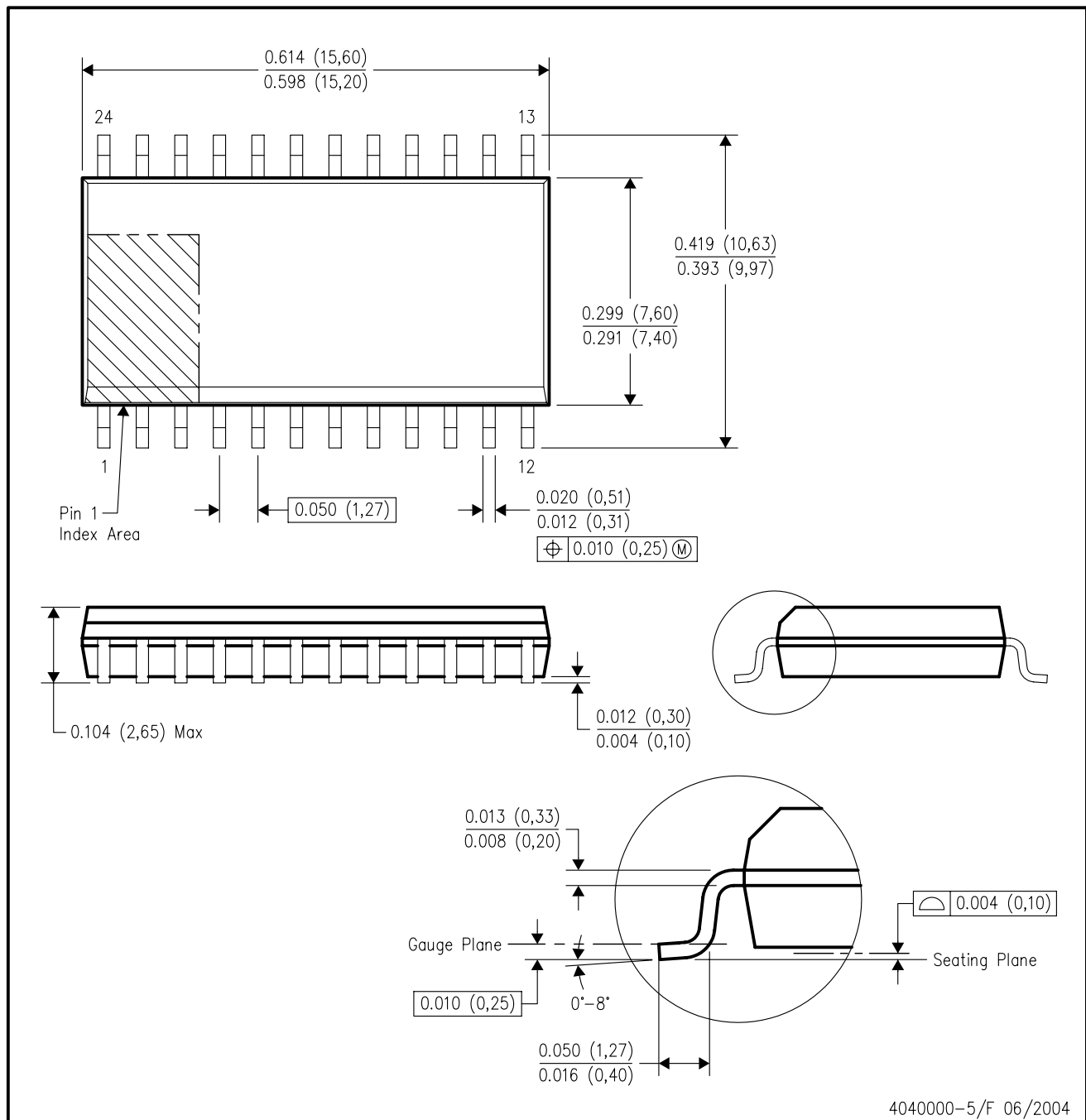
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

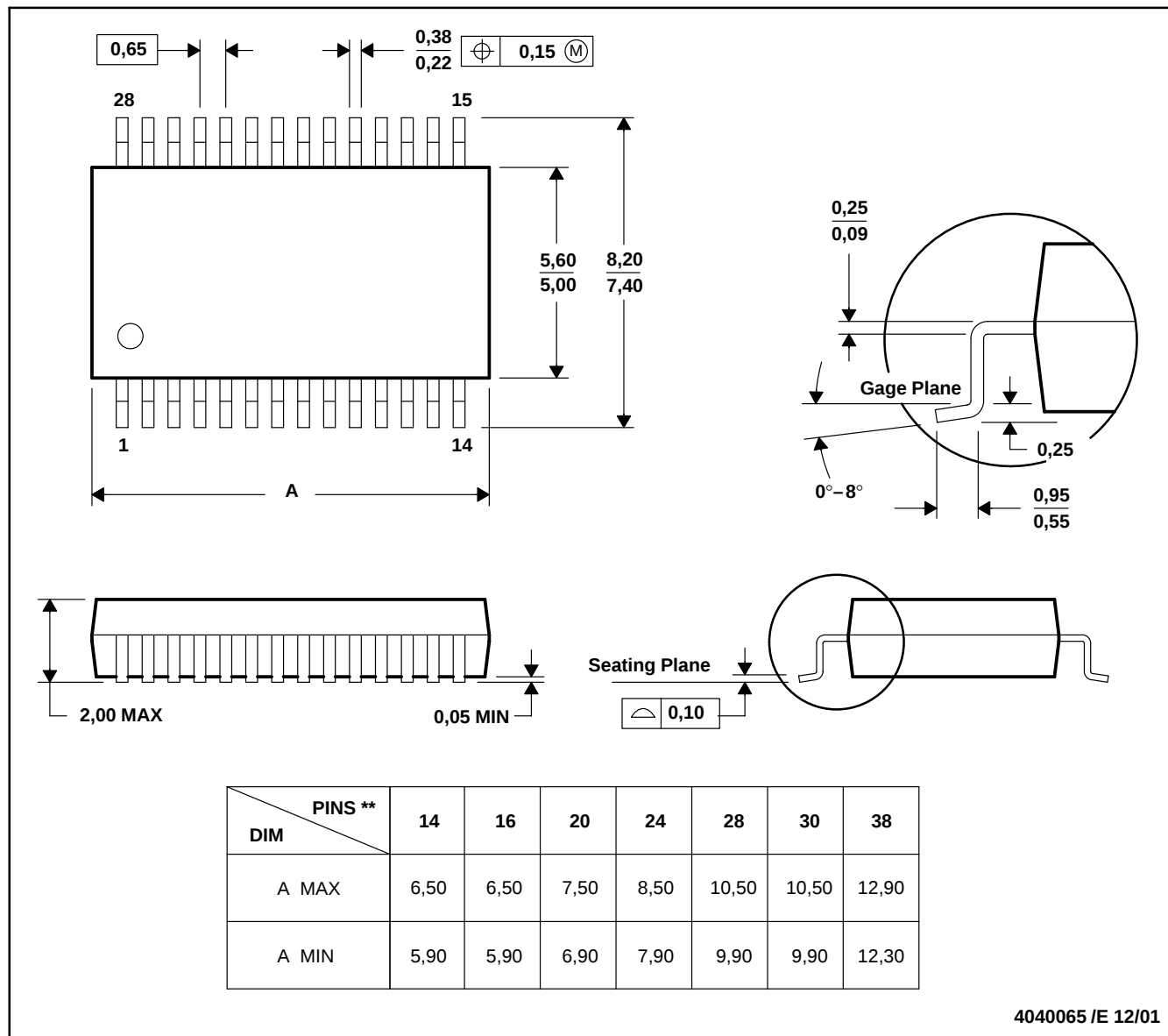


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

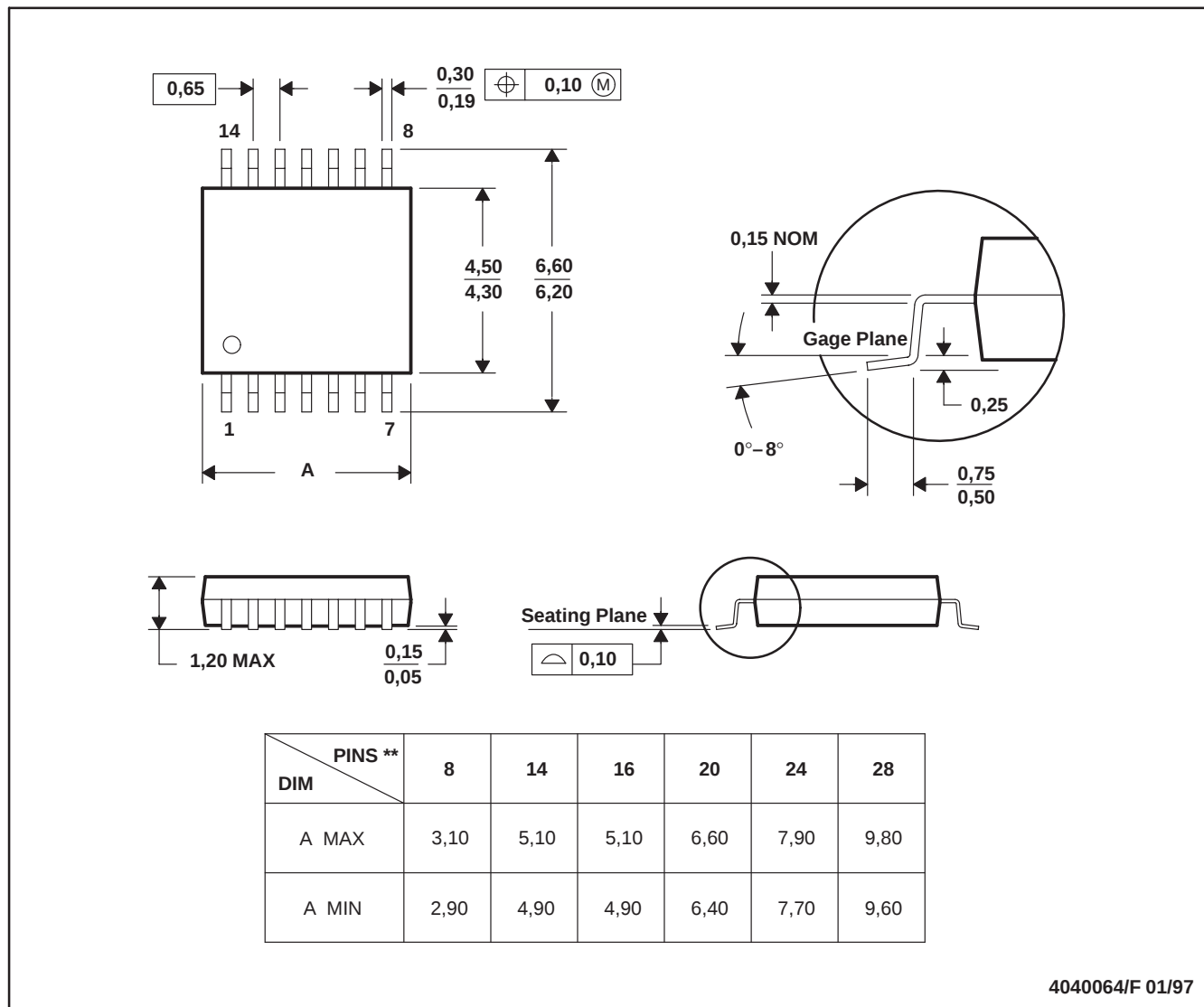


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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