

# SN54AHC273, SN74AHC273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS376E – JUNE 1997 – REVISED JANUARY 2000

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V  $V_{CC}$
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JEDEC 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

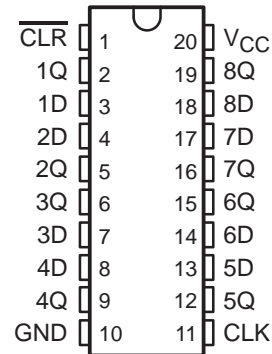
## description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{CLR}$ ) input.

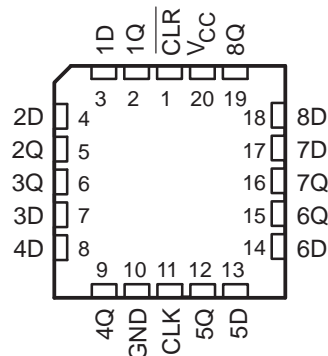
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54AHC273 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC273 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AHC273 . . . J OR W PACKAGE  
SN74AHC273 . . . DB, DGV, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHC273 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{CLR}$	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	$Q_0$



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**TEXAS  
INSTRUMENTS**

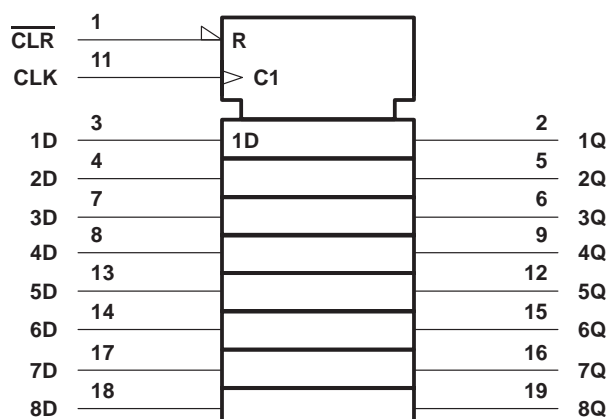
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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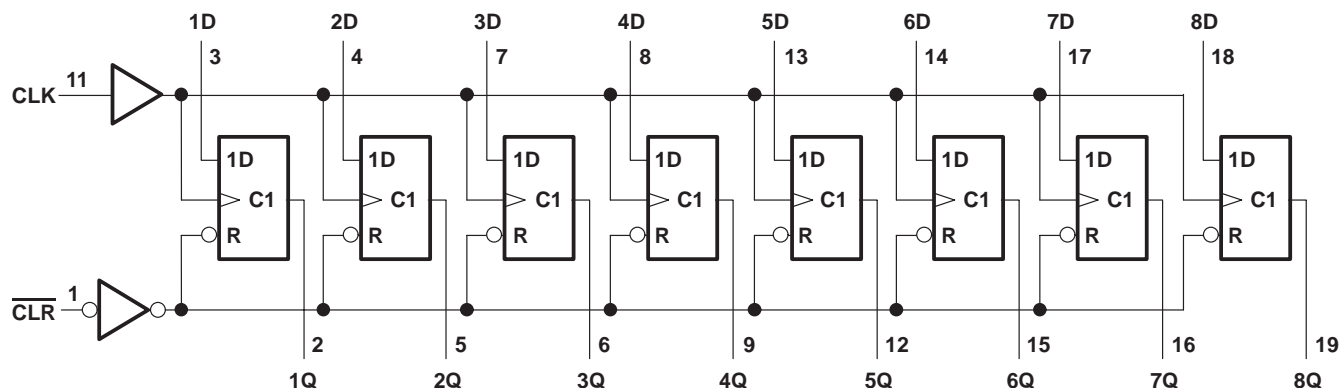
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## logic symbol†

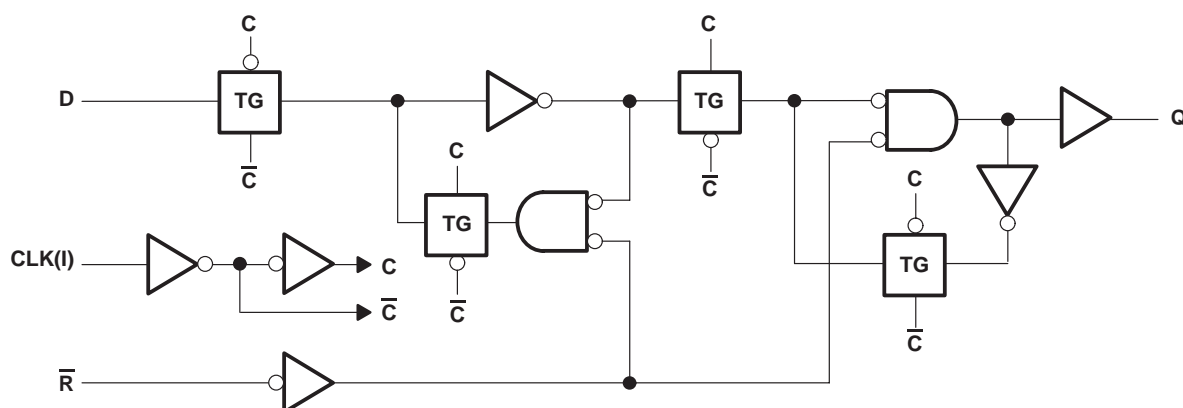


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## logic diagram, each flip-flop (positive logic)



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# SN54AHC273, SN74AHC273

## OCTAL D-TYPE FLIP-FLOPS

### WITH CLEAR

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC273		SN74AHC273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2.5 10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

		SN54AHC273				SN74AHC273				UNIT
		T <sub>A</sub> = 25°C		MIN	MAX	T <sub>A</sub> = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
t <sub>w</sub>	Pulse duration	CLR low	5	6	5	6	ns			
		CLK high or low	5	6.5	5	6.5				
t <sub>su</sub>	Setup time	Data before CLK↑	5.5	6.5	5.5	6.5	ns			
		CLR before CLK↑	2.5	2.5	2.5	2.5				
t <sub>h</sub>	Hold time, data after CLK↑		1.5	2	1	1	ns			

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		SN54AHC273				SN74AHC273				UNIT
		T <sub>A</sub> = 25°C		MIN	MAX	T <sub>A</sub> = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
t <sub>w</sub>	Pulse duration	CLR low	5	5	5	5	ns			
		CLK high or low	5	5	5	5				
t <sub>su</sub>	Setup time	Data before CLK↑	4.5	4.5	4.5	4.5	ns			
		CLR before CLK↑	2	2	2	2				
t <sub>h</sub>	Hold time, data after CLK↑		1.5	2	1	1	ns			



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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	75*	120*		65*		65		MHz
			$C_L = 50\text{ pF}$	50	75		45		45		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		8.9*	13.6*	1*	16*	1	16	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$		8.7*	13.6*	1*	16*	1	16	ns
$t_{\text{PHL}}$					8.7*	13.6*	1*	16*	1	16	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		11.4	17.1	1	19.5	1	19.5	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$		11.2	17.1	1	19.5	1	19.5	ns
$t_{\text{PHL}}$					11.2	17.1	1	19.5	1	19.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1.5**				1.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	120*	165*		100*		100		MHz
			$C_L = 50\text{ pF}$	80	110		70		70		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		5.2*	8.5*	1*	10*	1	10	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$		5.8*	9*	1*	10.5*	1	10.5	ns
$t_{\text{PHL}}$					5.8*	9*	1*	10.5*	1	10.5	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		6.7	10.5	1	12	1	12	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$		7.3	11	1	12.5	1	12.5	ns
$t_{\text{PHL}}$					7.3	11	1	12.5	1	12.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1**				1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)**

PARAMETER		SN74AHC273			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

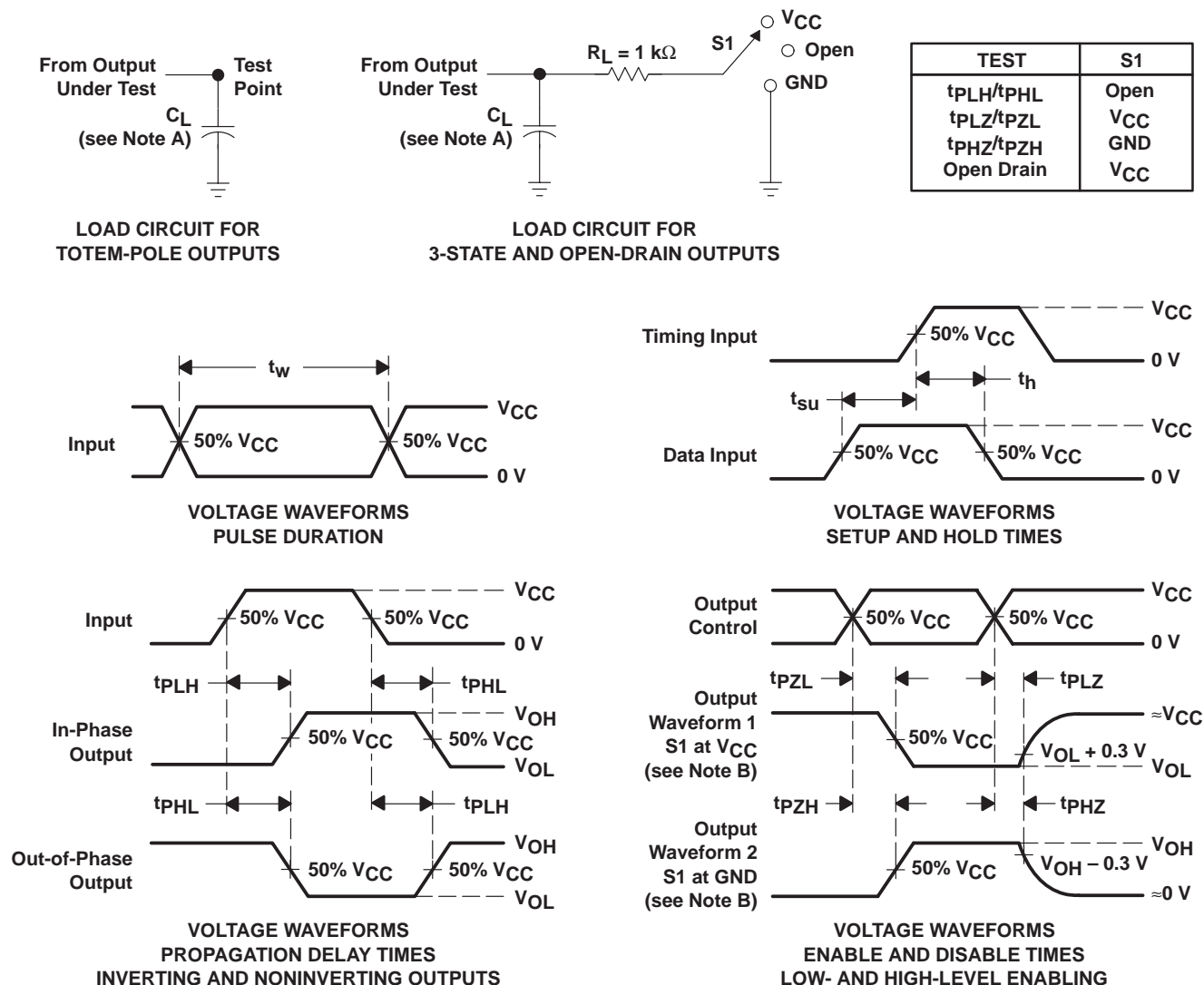
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	31	pF



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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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