SDAS099C - JUNE 1986 - REVISED MAY 1996

•	Applications: - Dual 2-Line to 4-Line Decoder	_	D OR N PACKAGE (TOP VIEW)		
	- Dual 1-Line to 4-Line Demultiplexer	٦.,۲	∇	٦.,	
	- 3-Line to 8-Line Decoder	1 <u>C</u> <u> </u> 1 1 <u>G</u> <u> </u> 2	16	J V <u>C</u> C] 2C	
	- 1-Line to 8-Line Demultiplexer	ВП3	15 14	1 2 <u>G</u>	
	Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words	1Y3 🛚 4		Ā	
•	Package Options Include Plastic	1Y2 5		2Y3	
	Small-Outline (D) Packages and Standard	1Y1 [] 6 1Y0 [] 7	11] 2Y2] 2Y1	
	Plastic (N) 300-mil DIPs	GND [] 8	10 9] 211] 2Y0	
		4.	-	_	

description

One of the main applications of the SN74ALS156 is as a dual 1-line to 4-line decoder/demultiplexer with individual strobes (\overline{G}) and common binary-address inputs in a single 16-pin package. When both sections are enabled, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit enabling or disabling each of the 4-bit sections, as desired.

Data applied to input 1C is inverted at its outputs and data applied at input $2\overline{C}$ is not inverted through its outputs. The inverter following the 1C data input permits use of the SN74ALS156 as a 3-line to 8-line demultiplexer without external gating. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN74ALS156 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Function Tables

2-LINE TO 4-LINE DECODER OR **1-LINE TO 4-LINE DEMULTIPLEXER**

	I	NPUTS	OUTPUTS					
SELECT		STROBE	DATA					
В	Α	1 G	1C	1Y0	1Y1	1Y2	1Y3	
Х	Χ	Н	Х	Н	Н	Н	Н	
L	L	L	Н	L	Н	Н	Н	
L	Н	L	Н	Н	L	Н	Н	
Н	L	L	Н	Н	Н	L	Н	
Н	Н	L	Н	Н	Н	Н	L	
Х	Χ	Х	L	Н	Н	Н	Н	

2-LINE TO 4-LINE DECODER OR **1-LINE TO 4-LINE DEMULTIPLEXER**

	I	NPUTS	OUTPUTS					
SEL	SELECT STROBE		DATA	0011013				
В	Α	2 <mark>G</mark>	2C	2Y0	2Y1	2Y2	2Y3	
Х	Х	Н	Х	Н	Н	Н	Н	
L	L	L	L	L	Н	Н	Н	
L	Н	L	L	Н	L	Н	Н	
Н	L	L	L	Н	Н	L	Н	
Н	Н	L	L	Н	Н	Н	L	
Х	Χ	Х	Н	Н	Н	Н	Н	

3-LINE TO 8-LINE DECODER OR 1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS						OUT	PUTS				
	SELECT		STROBE OR	0	1	2	3	4	5	6	7
ct	В	Α	DATA G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
Х	Х	Χ	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	Н	L	Н	Н	н
L	L	Н	L	Н	L	Н	Н	Н	L	Н	н
L	Н	L	L	Н	Н	L	Н	Н	Н	Н	н
L	Н	Н	L	Н	Н	Н	L	Н	Н	Н	н
Н	L	L	L	Н	Н	Н	Н	L	Н	Н	н
Н	L	Н	L	Н	Н	Н	Н	Н	L	Н	н
Н	Н	L	L	Н	Н	L	Н	Н	Н	L	н
Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	L

† \underline{C} = inputs 1 \underline{C} and 2 $\underline{\overline{C}}$ connected together ‡ \overline{G} = inputs 1 \overline{G} and 2 \overline{G} connected together



2Y2

2Y3

12

logic symbols[†] (alternatives)

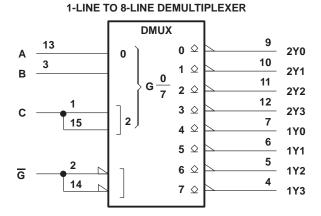
2-LINE TO 4-LINE DECODER X/Y 7 1Y0 0 α ♀ 6 1G 1Y1 1 α \diamondsuit ΕN 1 5 1C 1Y2 **2** α ◊ 4 1Y3 13 3 α ◊ 9 3 0 β ♀ 2Y0 В 2 10 1 β ☆ 2Y1 14 11 & 2G 2 β ◊ 2Y2 15 ΕN 12 2<u>C</u> 3 β ☆ 2Y3

13 Α 0 3 G 3 В 1 **DMUX** 0 🗘 1Y0 6 2 G4 1 🕸 1Y1 1G 5 1C 4 1Y2 2 ♦ 4 3 ☆ 1Y3 9 2Y0 10 14 2Y1 2G 15 11

2<u>C</u>

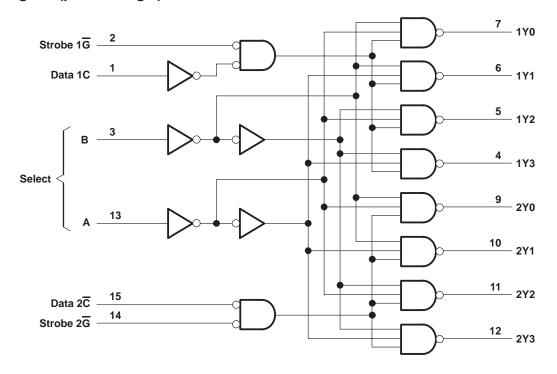
1-LINE TO 4-LINE DEMULTIPLEXER

3-LINE TO 8-LINE DECODER X/Y 9 13 0 🗅 2Y0 Α 10 3 1 ♀ 2Y1 В 2 11 2 ♀ 2Y2 12 3 ♀ 2Y3 7 15 4 ♀ 1Y0 6 5 ♀ 1Y1 5 6 ♀ 1Y2 4 14 ΕN 7 ♦ 1Y3



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Operating free-air temperature range, T _A	°C to 70°C
Storage temperature range, T _{stq} 65°	C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
VOH	High-level output voltage			5.5	V
loL	Low-level output current			8	mA
TA	Operating free-air temperature	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDI	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	$I_I = -18 \text{ mA}$			-1.5	V
Val	V _{CC} = 4.5 V	I _{OL} = 4 mA		0.25	0.4	V
VOL	∨CC = 4.5 V	I _{OL} = 8 mA		0.35	0.5	
IOH	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1	mA
ΙĮ	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1	mA
lін	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20	μΑ
Ι _{ΙL}	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1	μΑ
ICCL	V _{CC} = 5.5 V			5	9	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

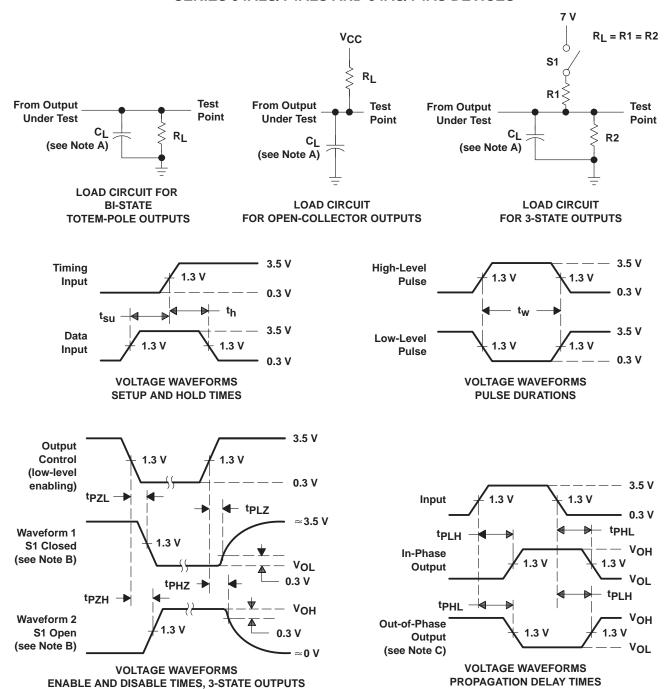
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MA		UNIT
			MIN	MAX	
^t PLH	A, B	1Y, 2Y	7	55	
^t PHL		11, 21	6	25	ns
t _{PLH}		1Y	7	50	ns
t _{PHL}	1C	11	6	23	115
^t PLH	1 G	1Y	7	38	no
^t PHL	1G	1 1	6	22	ns
tPLH	2 C , 2 G	2Y	7	38	nc
^t PHL		Ζ1	6	22	ns

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - D. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_{\Gamma} = t_{f} = 2$ ns, duty cycle = 50%.
 - E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



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