

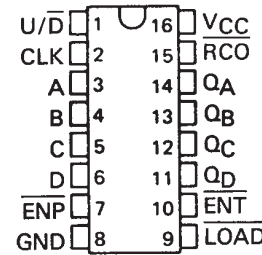
SN54LS169B, SN54S169 SN74LS169B, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

- Programmable Look-Ahead Up/Down Binary Counters
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

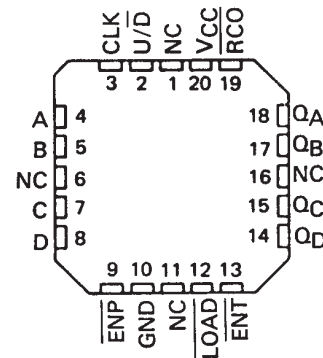
SN54LS169B, SN54S169 . . . J OR W PACKAGE
SN74LS169B, SN74S169 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS169B, SN54S169 . . . FK PACKAGE

(TOP VIEW)



NC-No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high speed counting applications. The 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{\text{ENP}}$, $\overline{\text{ENT}}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input ENT is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the $\overline{\text{ENP}}$ or $\overline{\text{ENT}}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

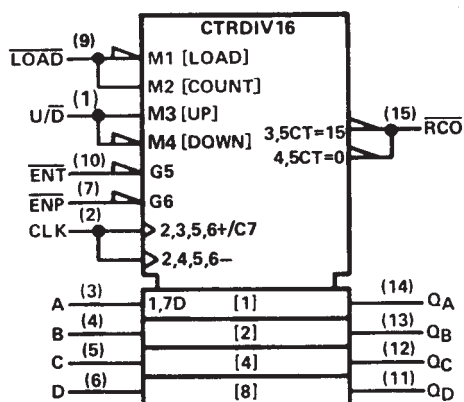
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{\text{ENP}}$, $\overline{\text{ENT}}$, $\overline{\text{LOAD}}$, $\overline{\text{U/D}}$) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169B	35MHz	35MHz	100mW
'S169	70MHz	55MHz	500mW

SN54LS169B, SN54S169
 SN74LS169B, SN74S169
 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

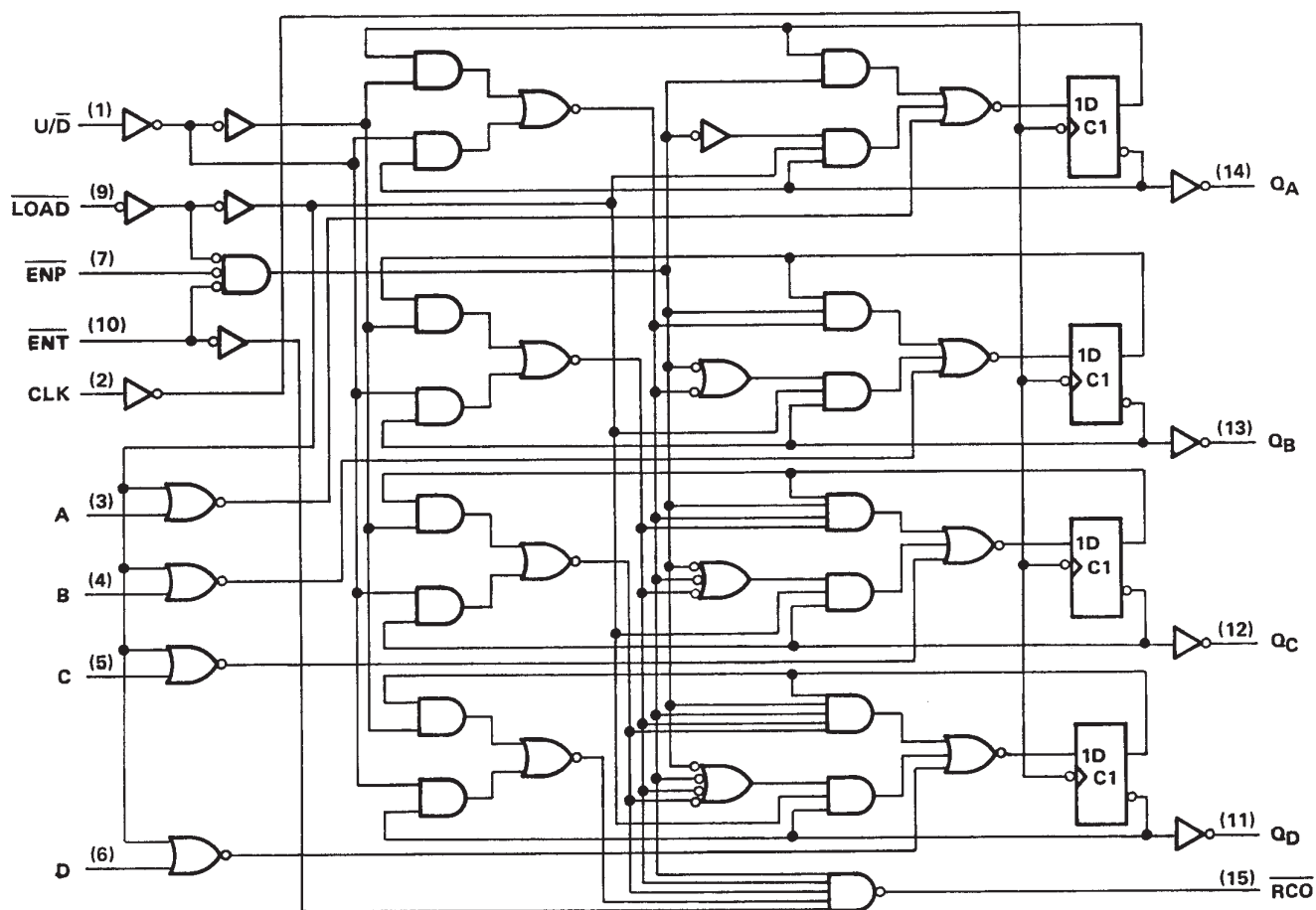
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for D, J, N, and W packages.

SN54LS169B, SN54S169
SN74LS169B, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS
SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

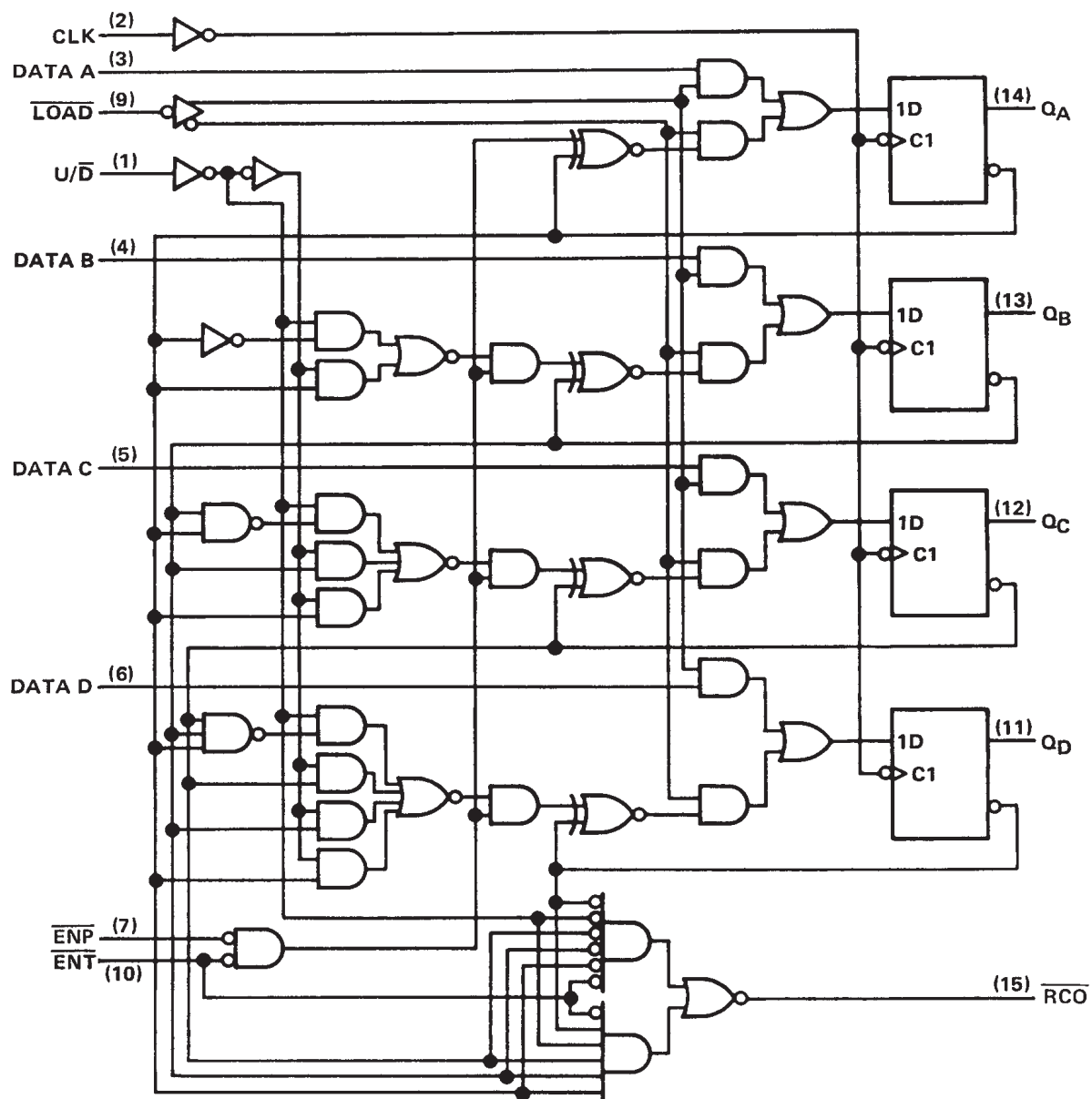
logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

SN54LS169B, SN54S169
 SN74LS169B, SN74S169
 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS
 SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

logic diagram (positive logic)

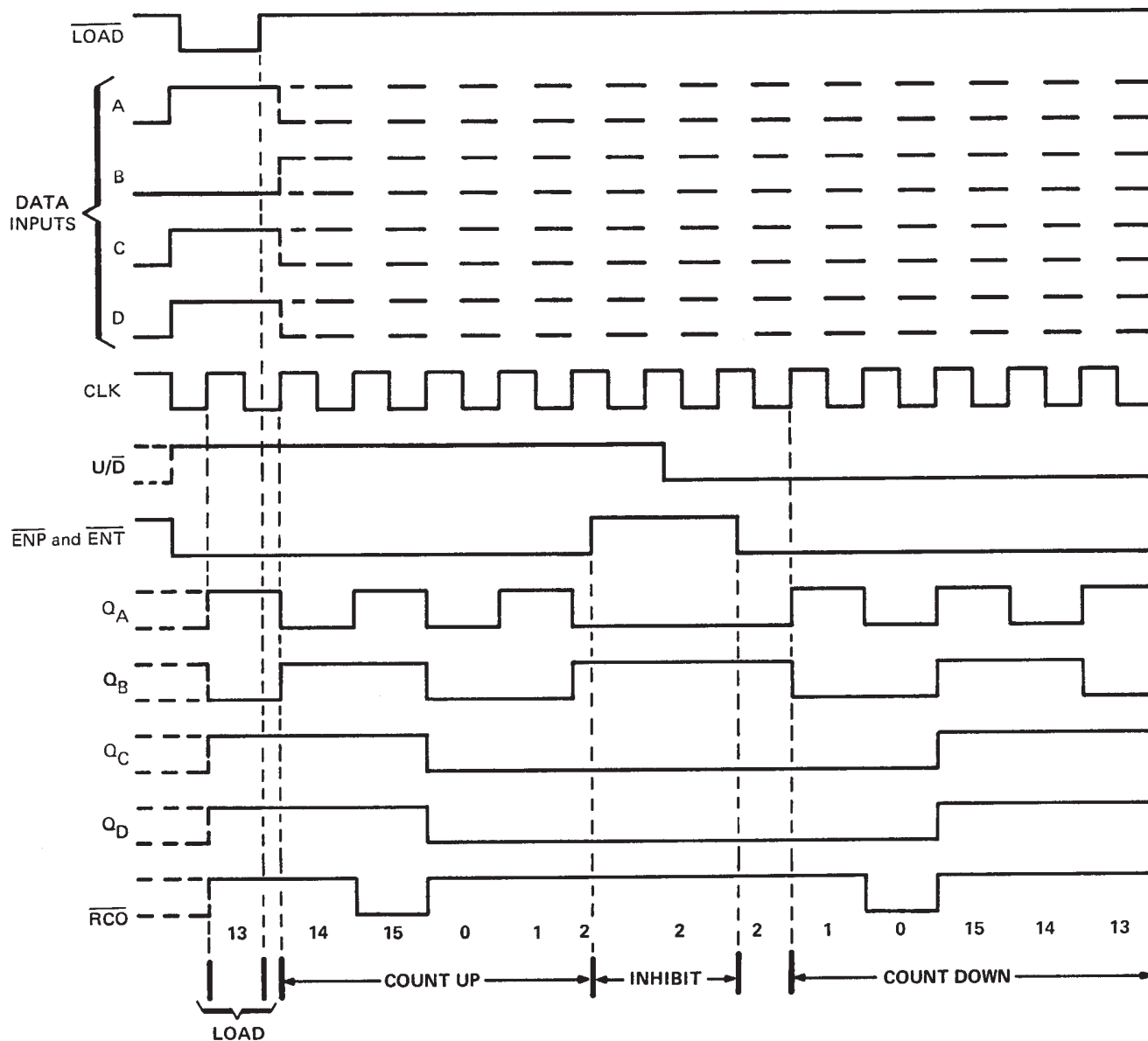


Pin numbers shown are for D, J, N, and W packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



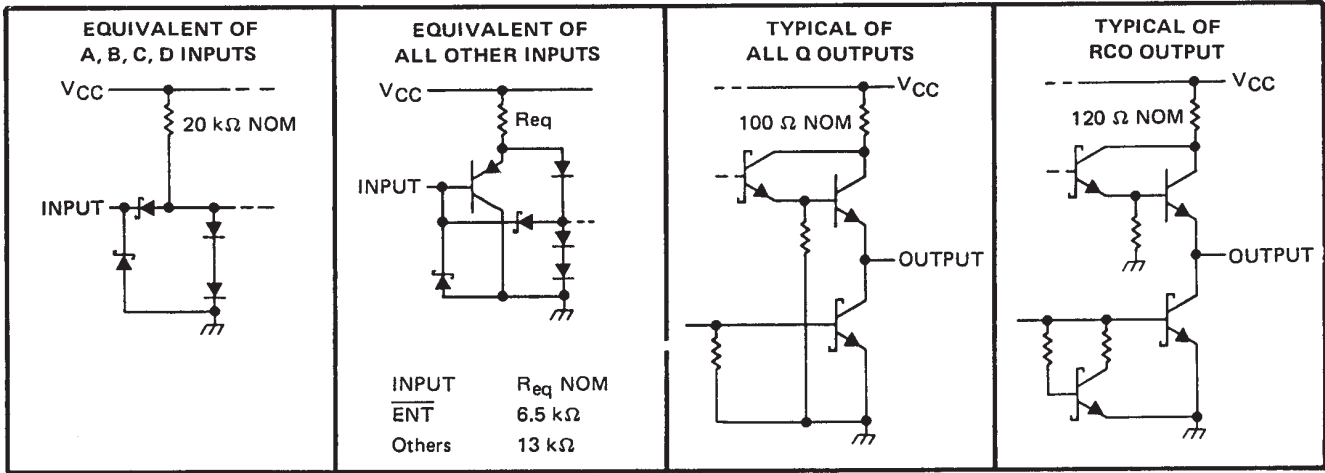
SN54LS169B, SN54S169

SN74LS169B, SN74S169

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1).	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS169B	– 55°C to 125°C
SN74LS169B	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS169B			SN74LS169B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level-input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			– 0.4			– 0.4	mA
				– 1.2			– 1.2	mA
I_{OL}	Low-level output current			4			8	mA
				12			24	mA
f_{clock}	Clock frequency	0		20	0		20	MHz
$t_{w(clock)}$	Width of clock pulse (high or low) (see Figure 1)	25			25			ns
t_{su}	Setup time, (see Figure 1)			30			30	ns
				30			30	
				35			35	
				35			35	
t_h	Hold time at any input with respect to clock (see Figure 1)	0			0			ns
T_A	Operating free-air temperature	– 55		125	0		70	°C

SN54LS169B, SN54S169
SN74LS169B, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†				SN54LS169B		SN74LS169B		UNIT
					MIN	TYP‡	MAX	MIN	
V _{IK}	V _{CC} = MIN, I _I = - 18 mA				- 1.5		- 1.5		V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	RCO	I _{OH} = - 0.4 mA		2.5	3.4	2.7	3.4	V
		Any Q	I _{OH} = - 1.2 mA		2.4	3.2	2.4	3.2	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	RCO	I _{OH} = 4 mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 8 mA				0.35	0.5	
		Any Q	I _{OL} = 12 mA		0.25	0.4	0.25	0.4	
			I _{OL} = 24 mA				0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V				0.1		0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				20		20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	U/D, LOAD, ENP, CLK			- 0.2		- 0.2		mA
		All other inputs			- 0.4		- 0.4		
I _{OS§}	V _{CC} = MAX, V _O = 0 V	RCO			- 20	- 100	- 20	- 100	mA
		Any Q			- 30	- 130	- 30	- 130	
I _{CC}	V _{CC} = MAX, See Note 2				28 45		28 45		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS169B			UNIT
				MIN	TYP	MAX	
f _{max}				20	35		MHz
t _{PLH}	CLK	$\overline{RCO}$	R _L = 2 kΩ, C _L = 15 pF		26	40	ns
t _{PHL}					17	25	
t _{PLH}	$\overline{ENT}$	$\overline{RCO}$			15	25	ns
t _{PHL}					11	20	
t _{PLH}	U/D	$\overline{RCO}$			23	35	ns
t _{PHL}					15	25	
t _{PLH}	CLK	Any Q	R _L = 667 Ω, C _L = 45 pF		16	25	ns
t _{PHL}					17	25	

¶ Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

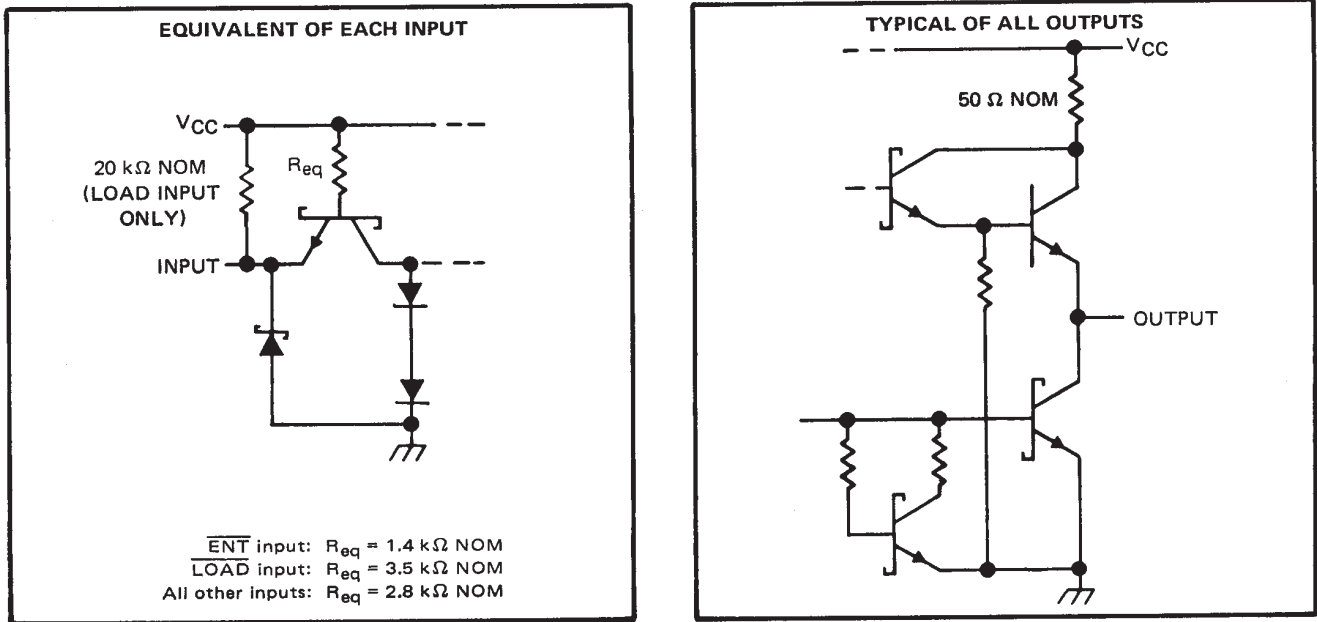
SN54LS169B, SN54S169

SN74LS169B, SN74S169

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (See Note 4)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 5)	5.5 V
Operating free-air temperature range: SN54S169 (see Note 6)	–55°C to 125°C
SN74S169	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

		SN54S169			SN74S169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}				–1			–1	mA
Low-level output current, I _{OL}				20			20	mA
Clock frequency, f _{clock}		0		40	0		40	MHz
Width of clock pulse, t _{w(clock)} (high or low) (see Figure 1)		10			10			ns
Setup time, t _{su} (see Figure 1)	Data inputs A, B, C, D	4			4			ns
	ENT or ENT	14			14			
	Load	9			6			
	U/D	20			20			
Hold time at any input with respect to clock, t _h (see Figure 1)		1			1			ns
Operating free-air temperature, T _A (see Note 6)		–55		125	0		70	°C

- NOTES:
4. Voltage values, except interemitter voltage, are with respect to network ground terminal.

5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs ENT and ENT.

6. A SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, RθCA, of not more than 26°C/W.

SN54LS169B, SN54S169
SN74LS169B, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S169			SN74S169			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA		0.5			0.5		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	ENT		100			100		μA
	Load		-10	-200		-10	-200	
	Other inputs		50			50		
I _{IL} Low-level input current	ENT		-4			-4		mA
	Other inputs		-2			-2		
I _{OS} Short-circuit output current§	V _{CC} = MAX,	-40		-100	-40		-100	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2		100	160		100	160	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	U/D = HIGH			U/D = LOW			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}			C _L = 15 pF, R _L = 280 Ω, See Figures 2 and 3 and Note 3	40	70		40	55		MHz
t _{PLH}	CLK	RCO			14	21		14	21	ns
t _{PHL}					20	28		20	28	
t _{PLH}					8	15		8	15	
t _{PHL}	CLK	Any Q			11	15		11	15	ns
t _{PLH}					7.5	11		6	12	
t _{PHL}					15	22		15	25	
t _{PLH} ◇	ENT	RCO			9	15		8	15	ns
t _{PHL} ◇					10	15		16	22	
t _{PHL} ◇	U/D	RCO								

¶ t_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

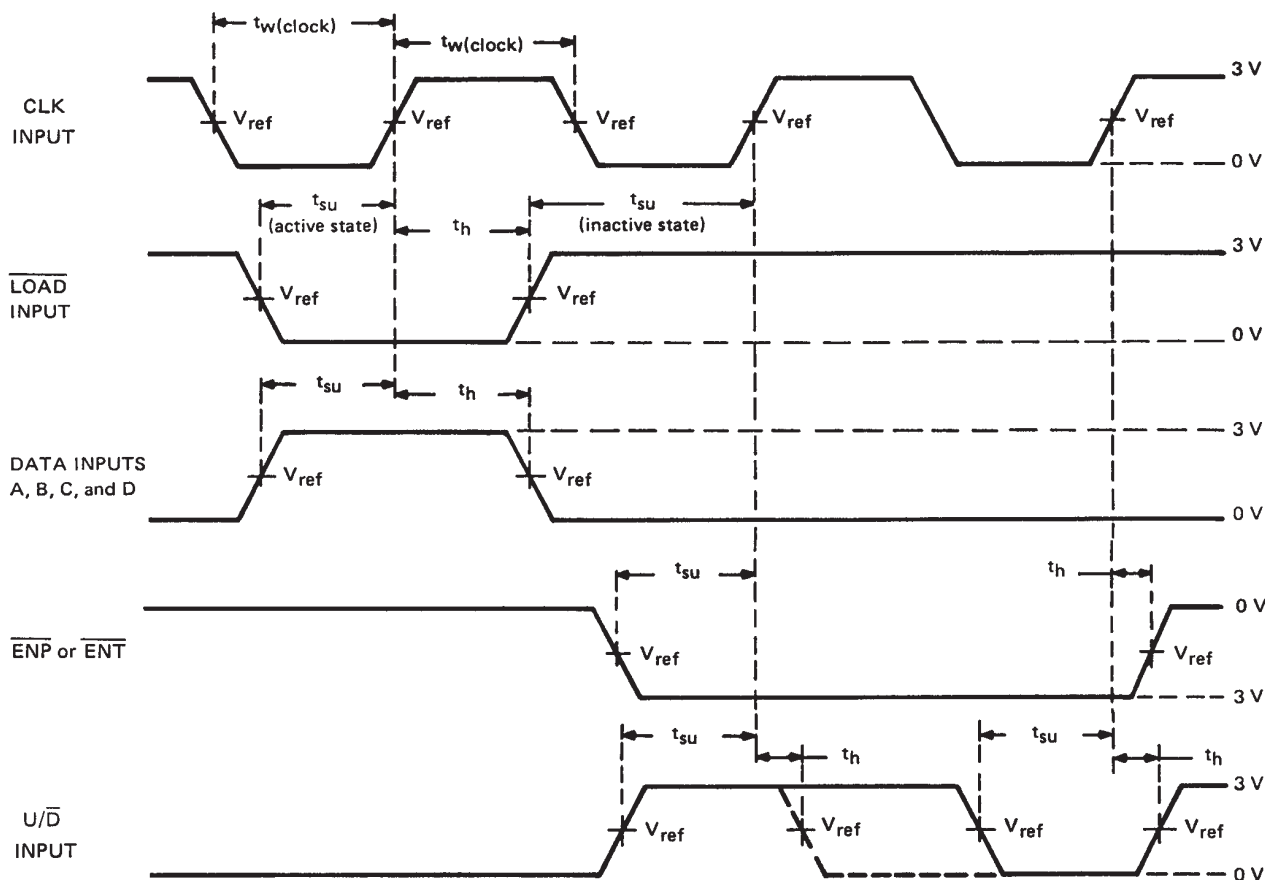
Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15 for 'S169), the ripple carry output will be out of phase.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**SN54LS169B, SN54S169
SN74LS169B, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS**

SDLS134 – OCTOBER 1976 – REVISED MARCH 1988

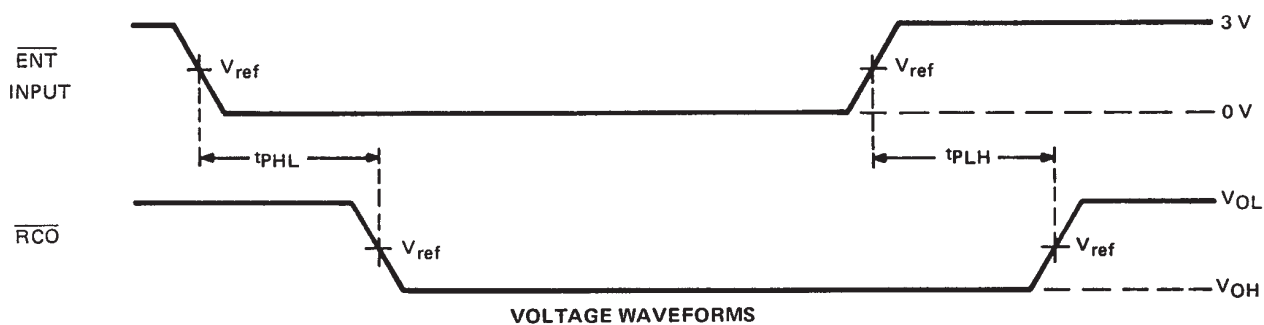
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for 'LS169B, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$, and for 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
B. For 'LS169B, $V_{ref} = 1.3 \text{ V}$; for 'S168 and 'S169, $V_{ref} = 1.5 \text{ V}$.

FIGURE 1—PULSE WIDTHS, SETUP TIMES, HOLD TIMES



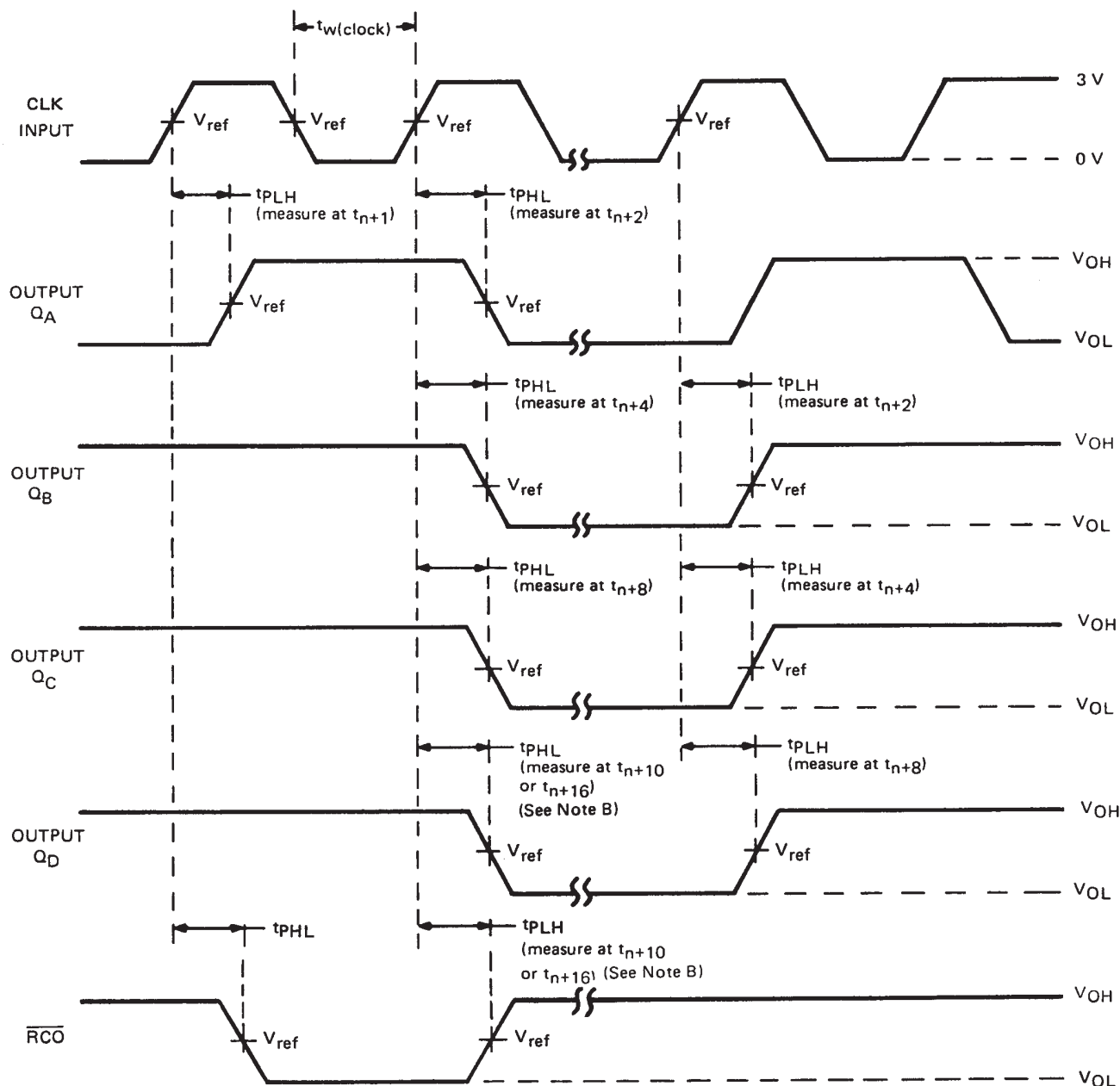
VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $PRR \leq \text{MHz}$, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for 'LS169B, $t_r \leq 15 \text{ ns}$, $t_f \leq 5 \text{ ns}$; and for 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
B. t_{PLH} and t_{PHL} from enable T input to ripple carry output assume that the counter is at the maximum count, all Q outputs high.
C. For 'LS169B, $V_{ref} = 1.3 \text{ V}$; for 'S169, $V_{ref} = 1.5 \text{ V}$.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.

FIGURE 2—PROPAGATION DELAY TIMES TO CARRY OUTPUT



PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{\text{out}} \approx 50 \Omega$; for 'LS169B, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$, and 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$. Vary PRR to measure f_{max} .
 B. Outputs Q_D and carry are tested at t_{n+16} , where t_n is the bit-time when all outputs are low.
 C. For 'LS169B, $V_{\text{ref}} = 1.3 \text{ V}$; for 'S169, $V_{\text{ref}} = 1.5 \text{ V}$.

FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
80018022A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8001802EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
8001802EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
8001802FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
8001802FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54S169J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54S169J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74LS169BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS169BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS169BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS169BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS169BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS169BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S169J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74S169J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74S169N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S169N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S169N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S169N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54LS169BFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS169BFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS169BJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS169BW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS169BW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S169FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SNJ54S169FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S169J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S169J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S169W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54S169W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

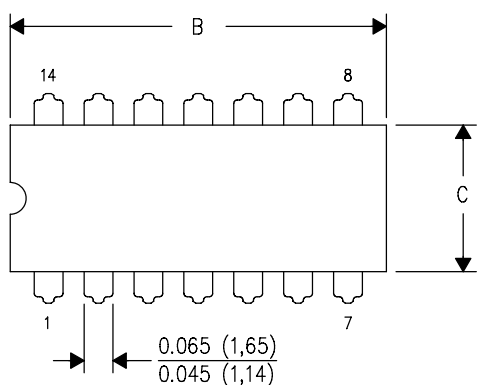
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

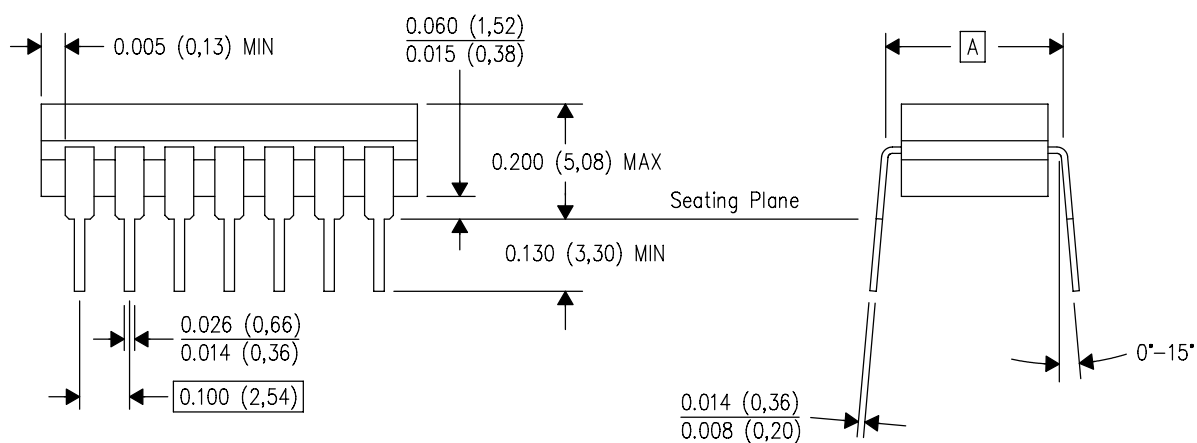
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

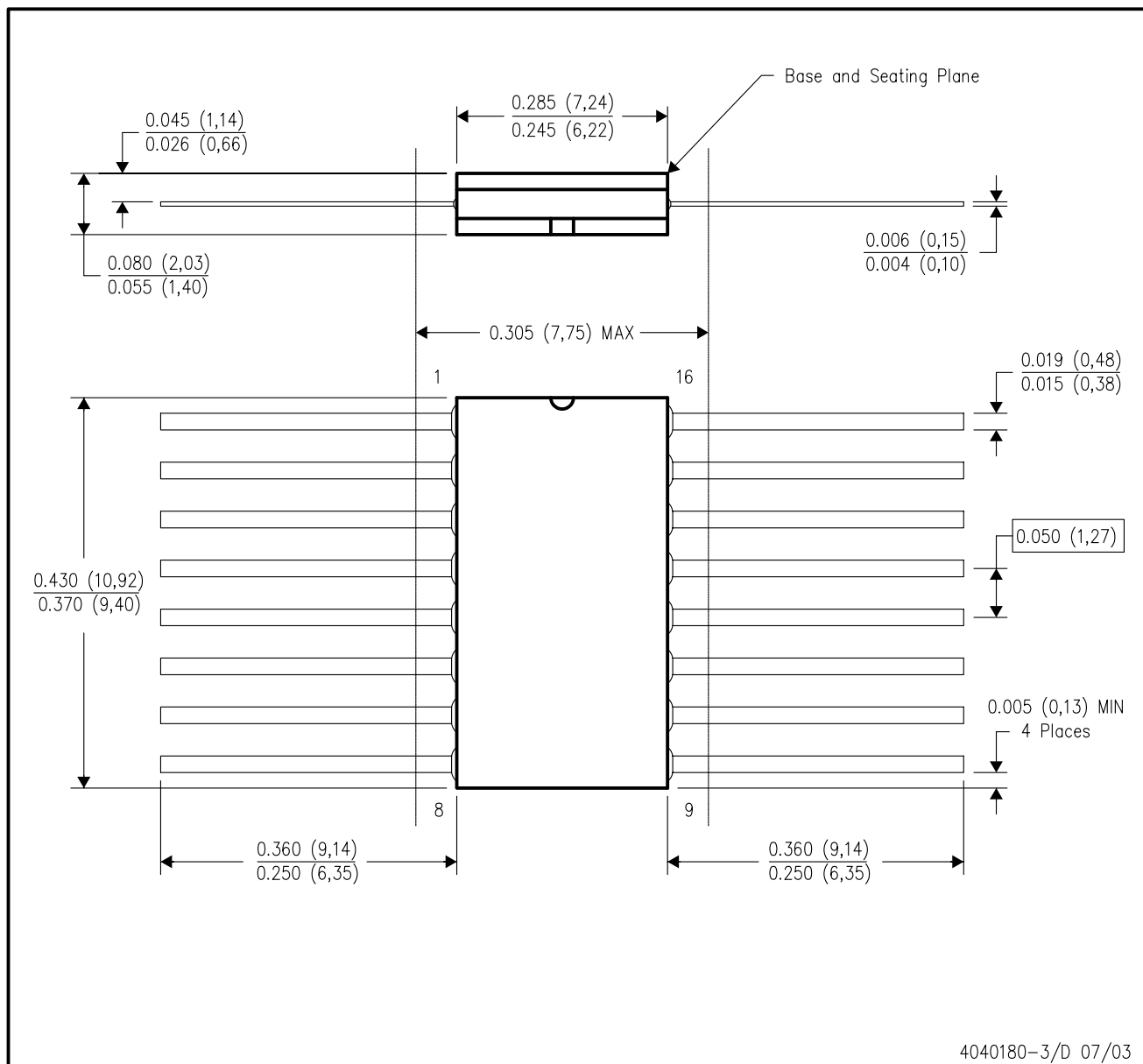


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

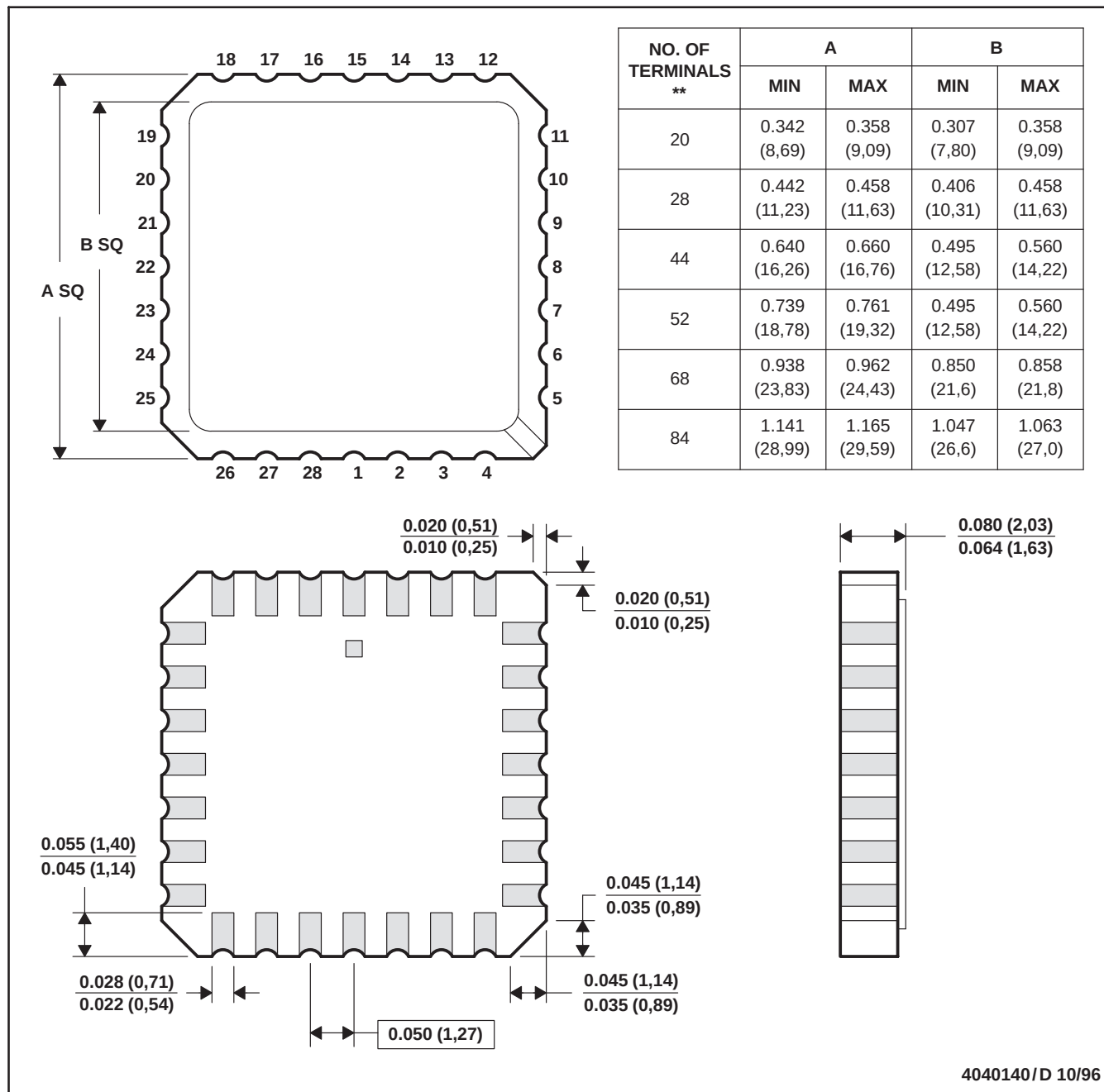


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

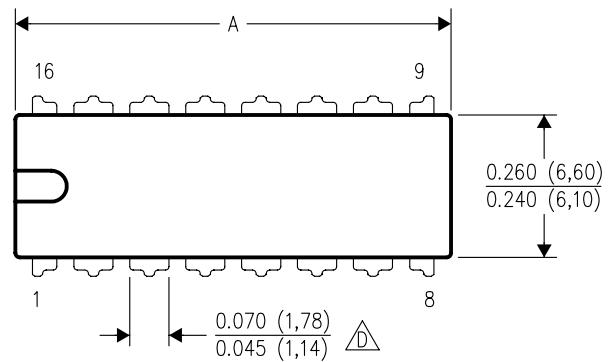


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

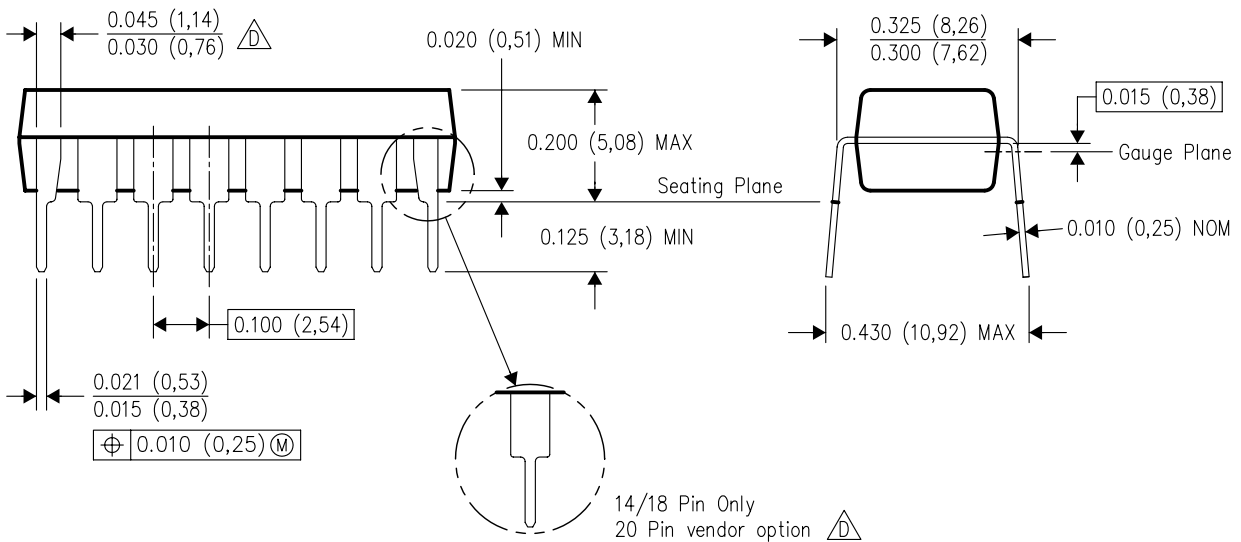
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

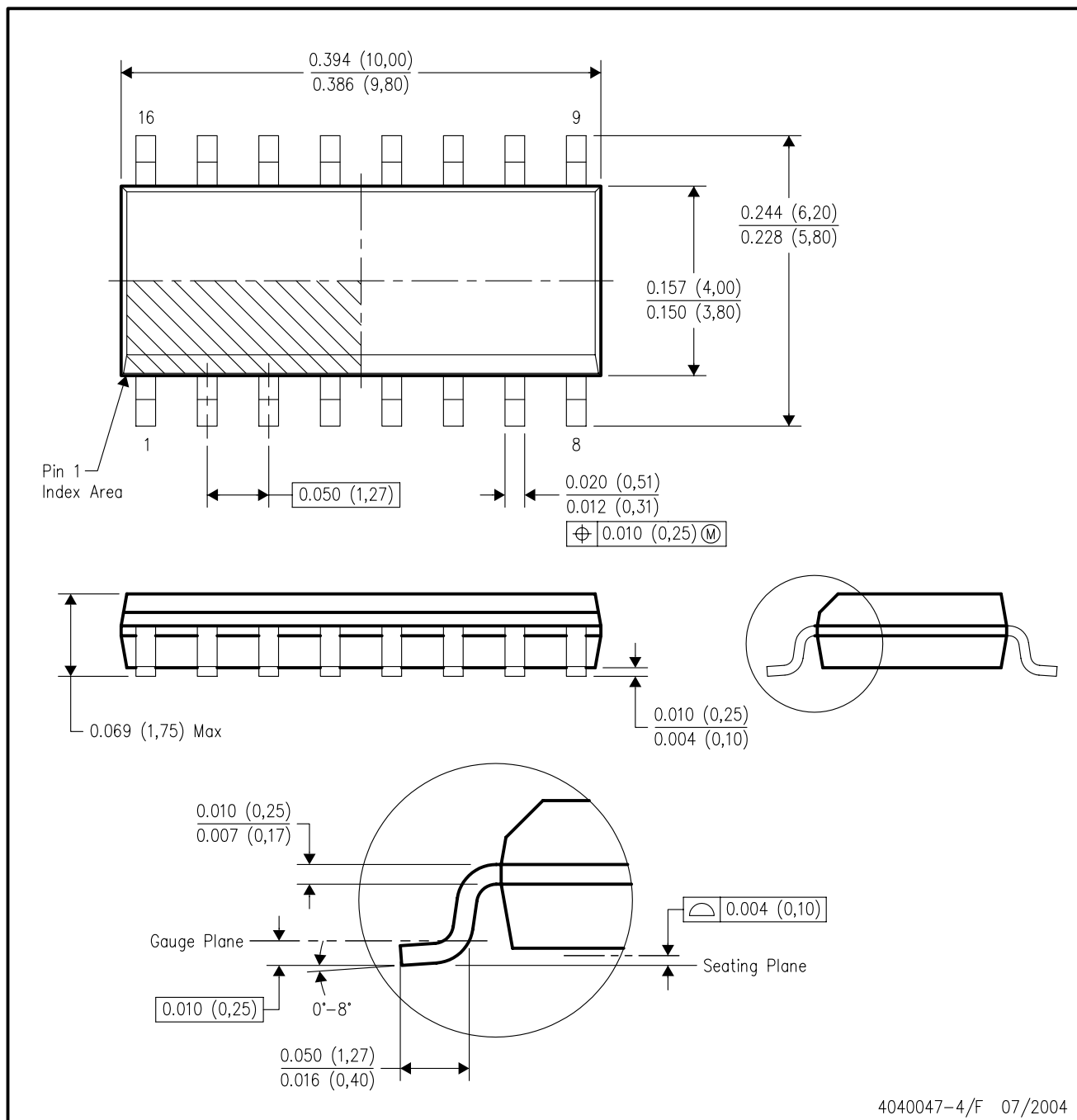


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



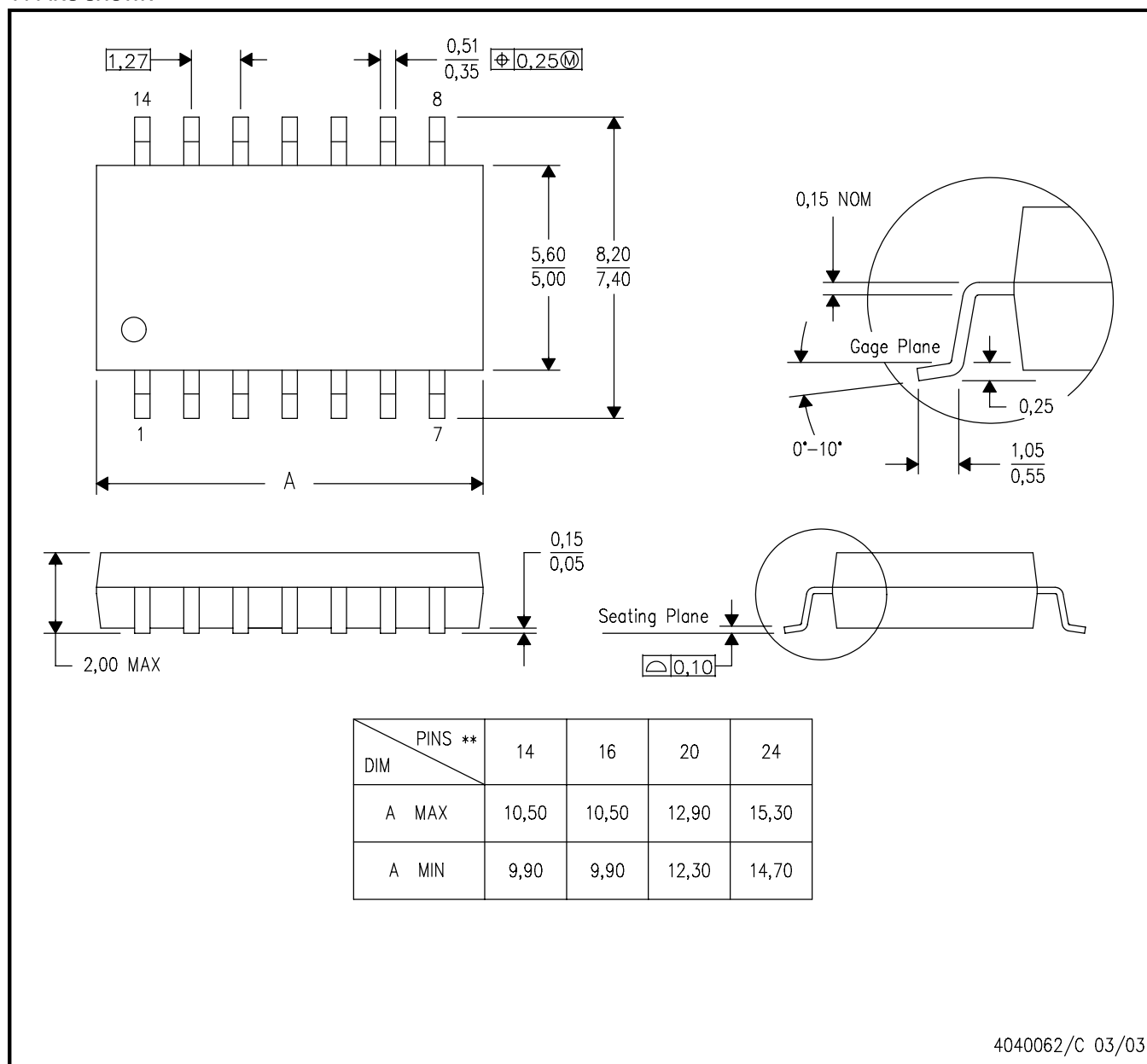
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated