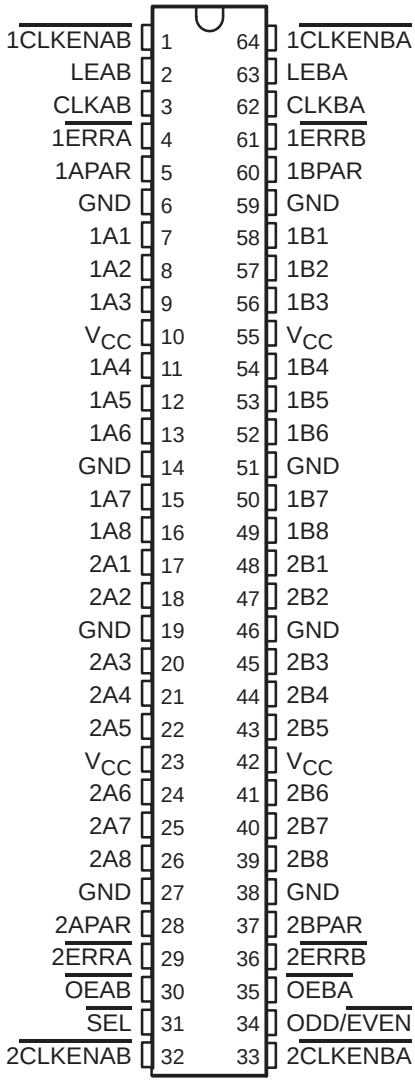
- **Member of the Texas Instruments *Widebus+*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Simultaneously Generates and Checks Parity**
- **Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down-Mode Operation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class I**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver, or it can generate/check parity from the two 8-bit data buses in either direction.

The SN74LVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) inputs. It also provides parity-enable ($\overline{\text{SEL}}$) and parity-select (ODD/$\overline{\text{EVEN}}$) inputs and separate error-signal ($\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$) outputs for checking parity. The direction of data flow is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. When $\overline{\text{SEL}}$ is low, the parity functions are enabled. When $\overline{\text{SEL}}$ is high, the parity functions are disabled, and the device acts as an 18-bit registered transceiver.

description (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74LVCH16901 is characterized for operation from –40°C to 85°C.

Function Tables

FUNCTION†

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar, but uses $\overline{OEBA}$, LEBA, and $\overline{CLKENBA}$.
‡ Output level before the indicated steady-state input conditions were established
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY ENABLE

INPUTS			OPERATION OR FUNCTION	
$\overline{SEL}$	$\overline{OEBA}$	$\overline{OEAB}$		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.	Q_A data to B, Q_B data to A
H	L	H		Q_B data to A
H	H	L		Q_A data to B
H	H	H		Isolation

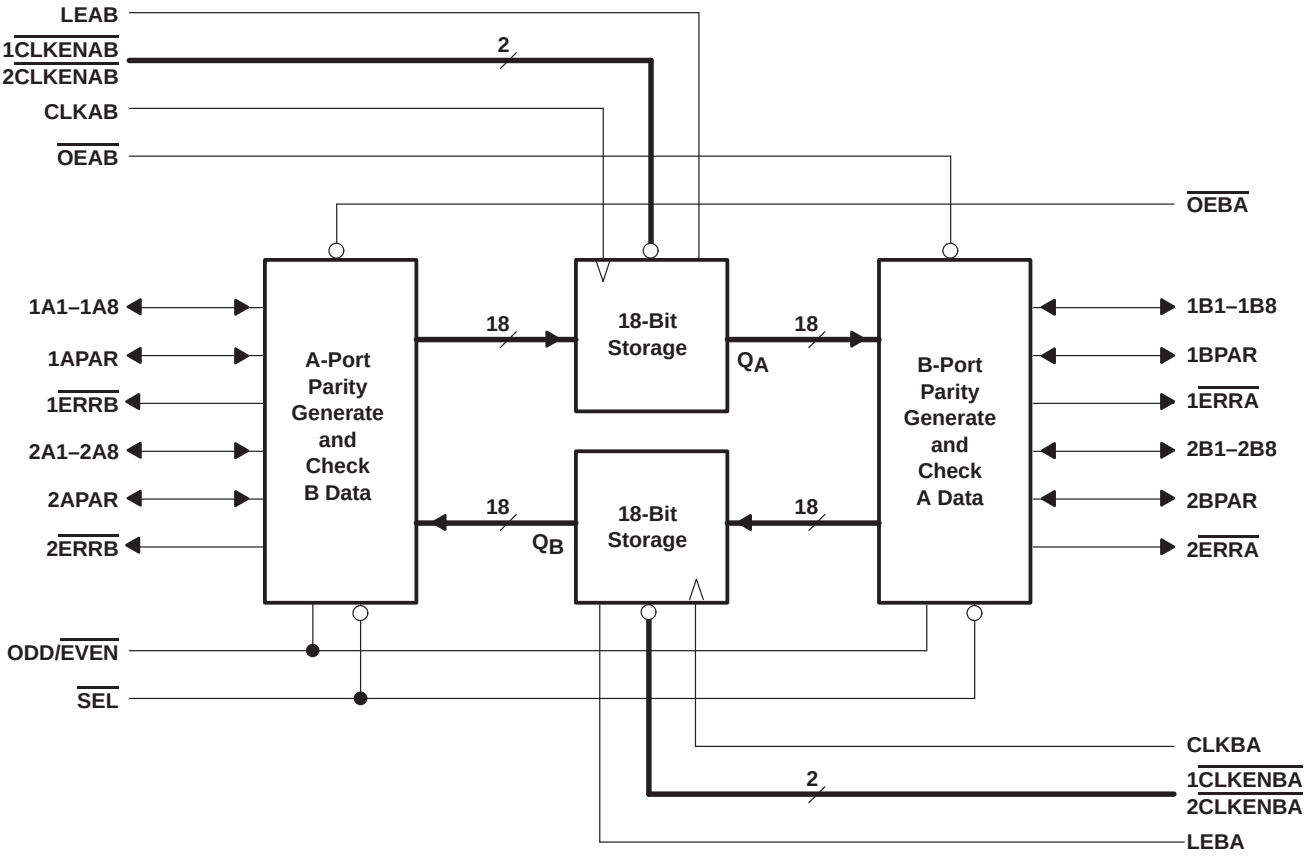
Function Tables (Continued)

PARITY

INPUTS								OUTPUTS			
$\overline{SEL}$	$\overline{OEBA}$	$\overline{OEAB}$	ODD/$\overline{EVEN}$	Σ OF INPUTS A1–A8 = H	Σ OF INPUTS B1–B8 = H	APAR	BPAR	APAR	$\overline{ERRA}$	BPAR	$\overline{ERRB}$
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE†	Z	PE†	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO‡	Z	PO‡	Z

† Parity output is set to the level so that the specific bus side is set to even parity.
‡ Parity output is set to the level so that the specific bus side is set to odd parity.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 73°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3 state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		1.65 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.7			
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2.2			
V_{OL}		I_{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.7	
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±5	μA
$I_{I(hold)}$	A or B ports	V_I = 0.58 V		1.65 V	25			μA
		V_I = 1.07 V			–25			
		V_I = 0.7 V		2.3 V	45			
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±600	
I_{off}		V_I or V_O = 5.5 V		0			±10	μA
I_{OZ}§		V_O = 0 to 5.5 V		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			20	μA
		3.6 V ≤ V_I ≤ 5.5 V¶					20	
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		7		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		9.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current, but not $I_{I(hold)}$.
¶ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V_{CC} = 1.8 V†		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			125		125		125		125	MHz
t_w	Pulse duration	CLK↑	4		3		3		3		ns
		LE high	3		3		3		3		
t_{su}	Setup time	A, APAR or B, BPAR before CLK↑	4.7		2.7		2.8		2.5		ns
		$\overline{CLKEN}$ before CLK↑	4.5		2.9		2.9		2.5		
		A, APAR or B, BPAR before LE↓	0		2.2		2.1		2		
t_h	Hold time	A, APAR or B, BPAR after CLK↑	0		1.2		1.2		1.3		ns
		$\overline{CLKEN}$ after CLK↑	0		1.3		1.3		1.5		
		A, APAR or B, BPAR after LE↓	1		1.7		1.9		1.7		

† Texas Instruments SPICE simulation data

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

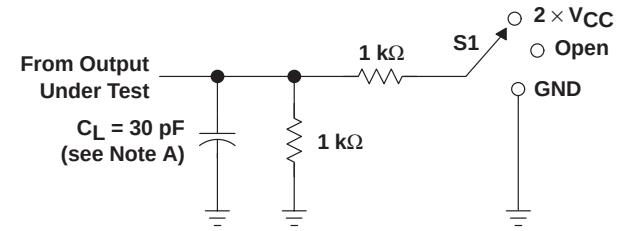
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V†	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	125		125		125		MHz
t_{pd}	A or B	B or A	5.9	1	6.2		5.8	1	5.4	ns
		BPAR or APAR	12.7	2	9.9		8.6	2	7.7	
	APAR or BPAR	BPAR or APAR	7	1	6.7		6.2	1	5.7	
		$\overline{ERRA}$ or $\overline{ERRB}$	13	2	10.7		9.7	2	8.5	
	ODD/$\overline{EVEN}$	$\overline{ERRA}$ or $\overline{ERRB}$	9.9	1.5	9.7		8.9	1.5	7.8	
		BPAR or APAR	10.4	1.5	9.3		8.6	1.5	7.5	
	$\overline{SEL}$	BPAR or APAR	6.9	1	7.1		6.9	1	6.1	
	CLKAB or CLKBA	A or B	6.9	1	7.4		6.8	1	6.1	
		BPAR or APAR parity feedthrough	8.5	1.5	8.1		7.3	1.5	6.6	
		BPAR or APAR parity generated	14.1	2.5	11.2		9.7	2	8.7	
		$\overline{ERRA}$ or $\overline{ERRB}$	14.3	2.5	11.5		9.9	2	8.9	
	LEAB or LEBA	A or B	6.8	1	7		6.5	1	5.8	
		BPAR or APAR parity feedthrough	7.9	1.5	7.7		7	1.5	6.3	
		BPAR or APAR parity generated	13.6	2.5	10.8		9.3	2	8.4	
		$\overline{ERRA}$ or $\overline{ERRB}$	13.5	2.5	10.9		9.5	2	8.5	
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR	6.8	1.4	7.3		7.1	1	6.3	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR	6.9	1.3	7.1		6.2	1.5	5.9	ns
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$	7.4	1.4	7.2		6.5	1	5.9	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$	9.3	1.3	8.3		7.5	1	6.7	ns
t_{en}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$	7.6	1.4	7.7		7.5	1	6.5	ns
t_{dis}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$	7.8	1.3	7.4		6.4	1.5	5.9	ns

† Texas Instruments SPICE simulation data

operating characteristics, T_A = 25°C

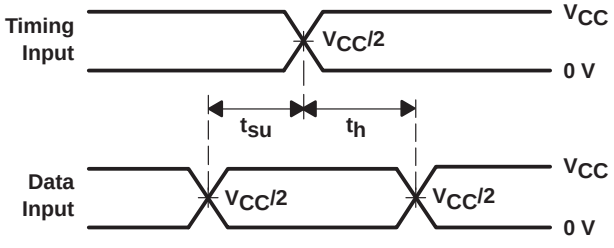
PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	37	52	68	pF
		Outputs disabled		16	22	28	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8 V

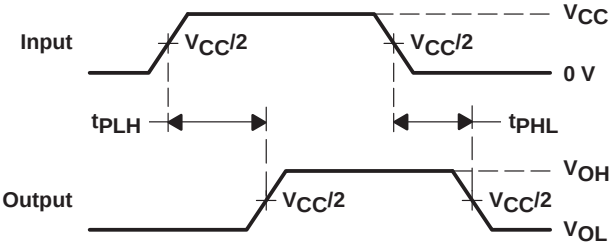


LOAD CIRCUIT

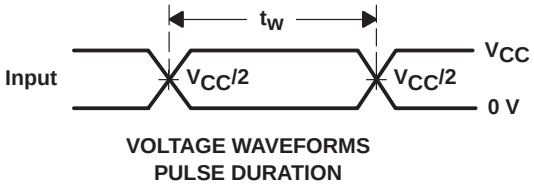
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND



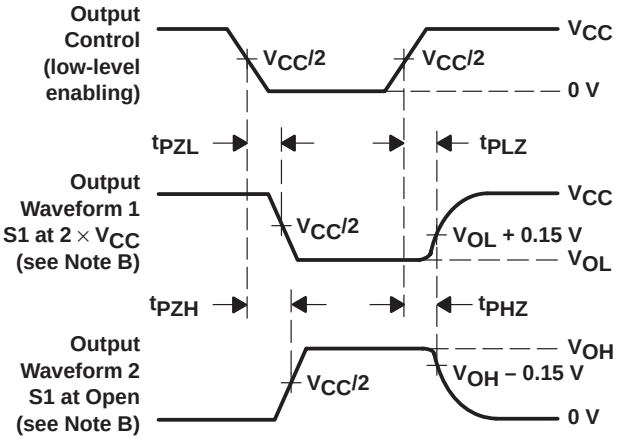
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

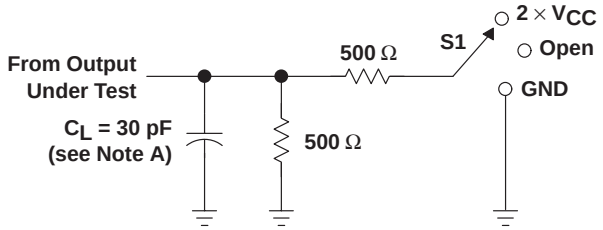


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

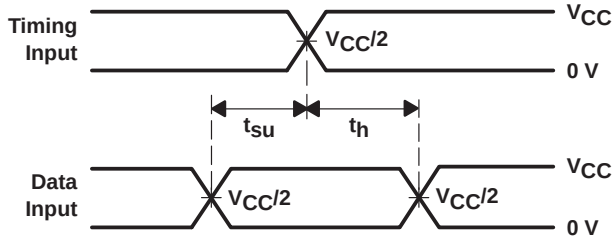
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

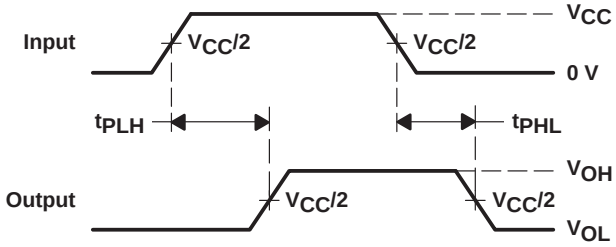


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

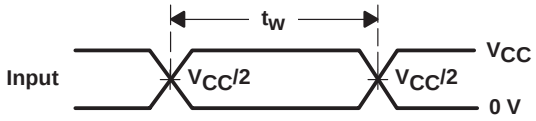
LOAD CIRCUIT



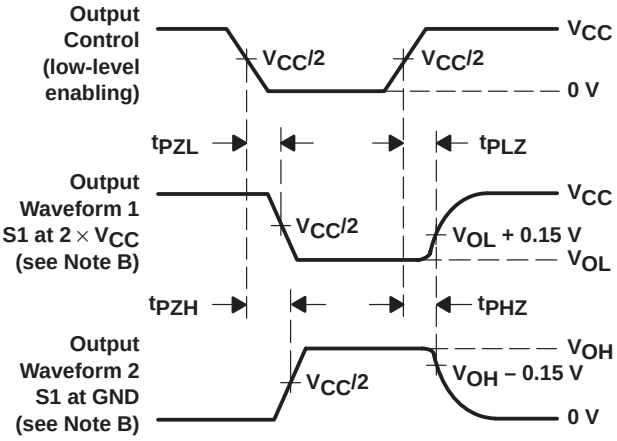
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

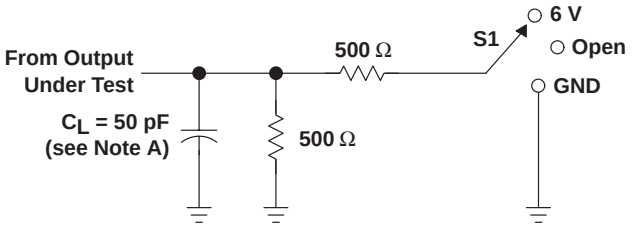


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

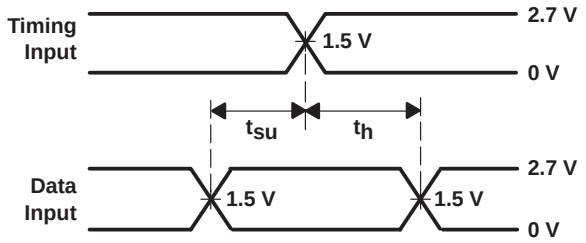
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

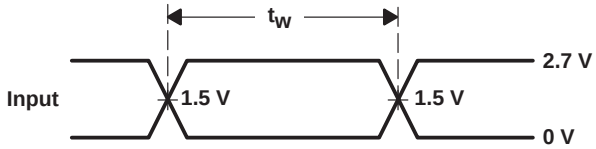


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

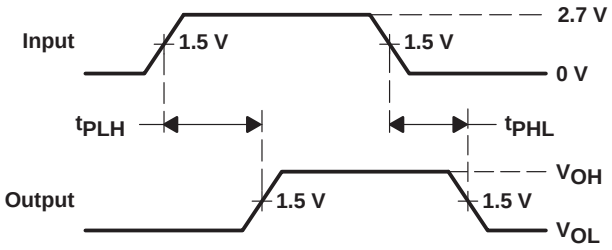
LOAD CIRCUIT



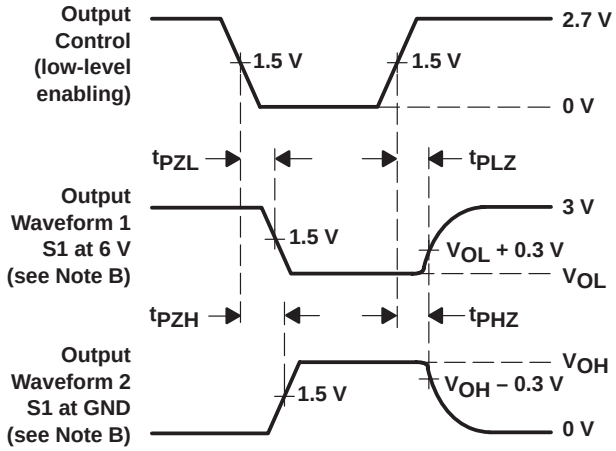
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

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