

# SN54AHC16245, SN74AHC16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS328C – MARCH 1996 – REVISED JULY 1998

- **Members of the Texas Instruments Widebus™ Family**
- **Operating Range 2-V to 5.5-V  $V_{CC}$**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

## description

The 'AHC16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

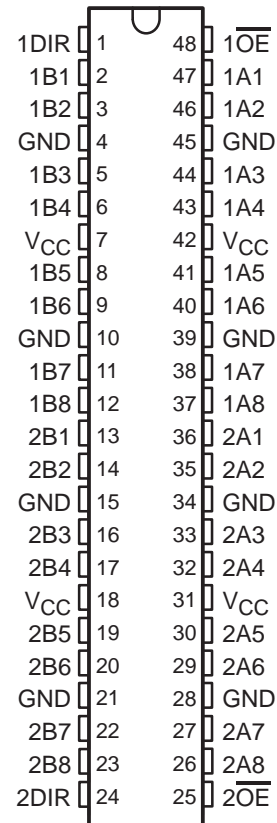
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16245 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC16245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**SN54AHC16245 . . . WD PACKAGE**  
**SN74AHC16245 . . . DGG, DGV, OR DL PACKAGE**  
(TOP VIEW)



PRODUCT PREVIEW



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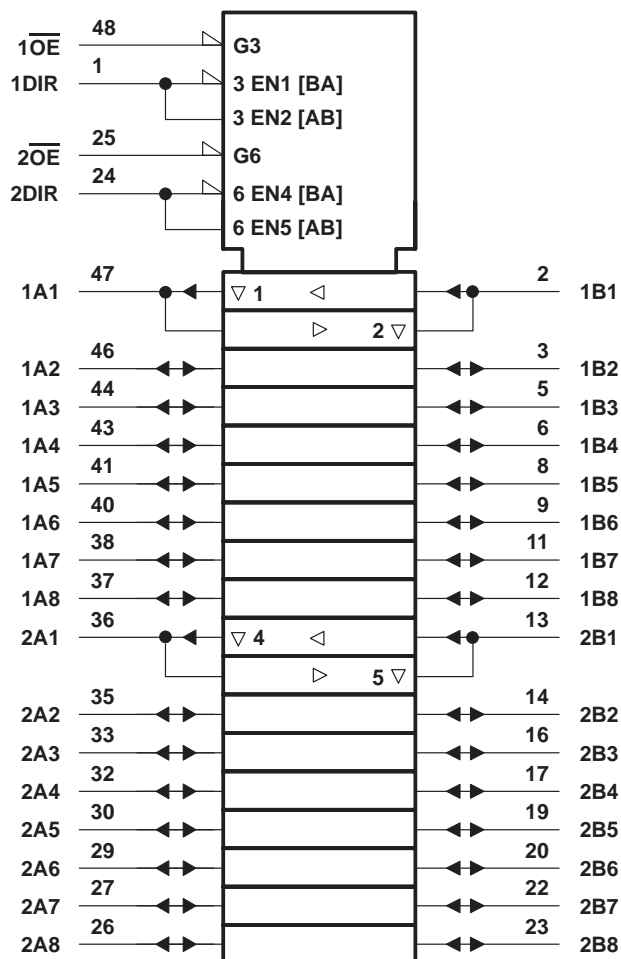
# SN54AHC16245, SN74AHC16245

## 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

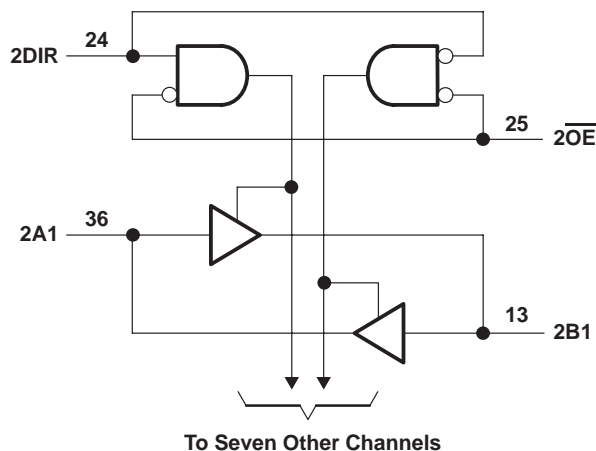
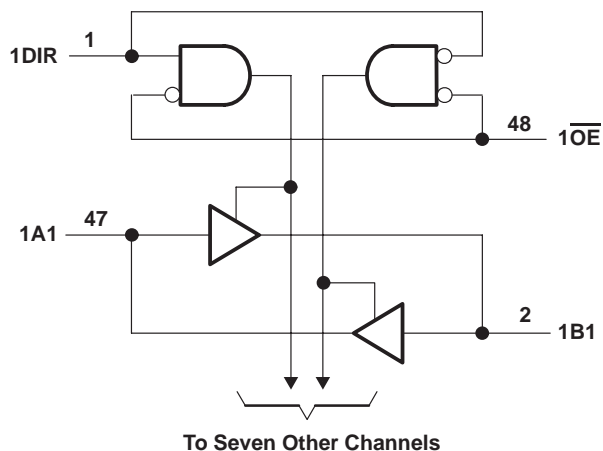
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 25$ mA
Continuous current through each $V_{CC}$ or GND	.....	$\pm 75$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):		
DGG package	.....	89°C/W
DGV package	.....	93°C/W
DL package	.....	94°C/W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

1. The input and output voltage ratings may be exceeded if the input and output currents are limited.
2. The package thermal impedance is calculated in accordance with JEDEC 51.

			SN54AHC16245		SN74AHC16245		UNIT	
					MIN	MAX	MIN	MAX
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V	
		V <sub>CC</sub> = 3 V	2.1		2.1			
		V <sub>CC</sub> = 5.5 V	3.85		3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		0.5		V	
		V <sub>CC</sub> = 3 V	0.9		0.9			
		V <sub>CC</sub> = 5.5 V	1.65		1.65			
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V	
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	−50		−50		μA	
		V <sub>CC</sub> = 3.3 ± 0.3 V	−4		−4		mA	
		V <sub>CC</sub> = 5 ± 0.5 V	−8		−8			
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50		50		μA	
		V <sub>CC</sub> = 3.3 ± 0.3 V	4		4		mA	
		V <sub>CC</sub> = 5 ± 0.5 V	8		8			
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 ± 0.3 V	100		100		ns/V	
		V <sub>CC</sub> = 5 ± 0.5 V	20		20			
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C	

# PRODUCT PREVIEW

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC16245		SN74AHC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA		2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
	I <sub>OH</sub> = -4 mA		3 V	2.58			2.48		2.48		
			4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA		2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA		3 V			0.36		0.5		0.44	
			4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	µA
	$\overline{\text{OE}}$ or DIR					±0.1		±1		±1	
I <sub>OZ</sub> <sup>†</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> ( $\overline{\text{OE}}$ ) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			±0.25		±2.5		±2.5	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	µA
C <sub>i</sub>	$\overline{\text{OE}}$ or DIR	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10				10	pF
C <sub>io</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4						pF

<sup>†</sup> The parameter I<sub>OZ</sub> includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC16245		SN74AHC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> *	A or B	B or A	C <sub>L</sub> = 15 pF		5.8	8.4	1	10	1	10	ns
t <sub>PHL</sub> *					5.8	8.4	1	10	1	10	
t <sub>PZH</sub> *	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 15 pF		8.5	13.2	1	15.5	1	15.5	ns
t <sub>PZL</sub> *					8.5	13.2	1	15.5	1	15.5	
t <sub>PHZ</sub> *	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 15 pF		8.9	12.5	1	15.5	1	15.5	ns
t <sub>PLZ</sub> *					8.9	12.5	1	15.5	1	15.5	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 50 pF		8.3	11.9	1	13.5	1	13.5	ns
t <sub>PHL</sub>					8.3	11.9	1	13.5	1	13.5	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 50 pF		11	16.7	1	19	1	19	ns
t <sub>PZL</sub>					11	16.7	1	19	1	19	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	C <sub>L</sub> = 50 pF		11.5	15.8	1	18	1	18	ns
t <sub>PLZ</sub>					11.5	15.8	1	18	1	18	
t <sub>sk(o)</sub> <sup>‡</sup>			C <sub>L</sub> = 50 pF			1.5**				1.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

‡ Skew between any two outputs of the same package switching in the same direction



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16245		SN74AHC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}^*$	A or B	B or A	$C_L = 15\text{ pF}$	4	5.5		1	6.5	1	6.5	ns
$t_{PHL}^*$				4	5.5		1	6.5	1	6.5	
$t_{PZH}^*$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$	5.8	8.5		1	10	1	10	ns
$t_{PZL}^*$				5.8	8.5		1	10	1	10	
$t_{PHZ}^*$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$	5.6	7.8		1	9.2	1	9.2	ns
$t_{PLZ}^*$				5.6	7.8		1	9.2	1	9.2	
$t_{PLH}$	A or B	B or A	$C_L = 50\text{ pF}$	5.5	7.5		1	8.5	1	8.5	ns
$t_{PHL}$				5.5	7.5		1	8.5	1	8.5	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$	7.3	10.6		1	12	1	12	ns
$t_{PZL}$				7.3	10.6		1	12	1	12	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$	7	9.7		1	11	1	11	ns
$t_{PLZ}$				7	9.7		1	11	1	11	
$t_{sk(o)}^\dagger$			$C_L = 50\text{ pF}$		1**					1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		SN74AHC16245			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.9		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage		3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	14	pF

PRODUCT PREVIEW



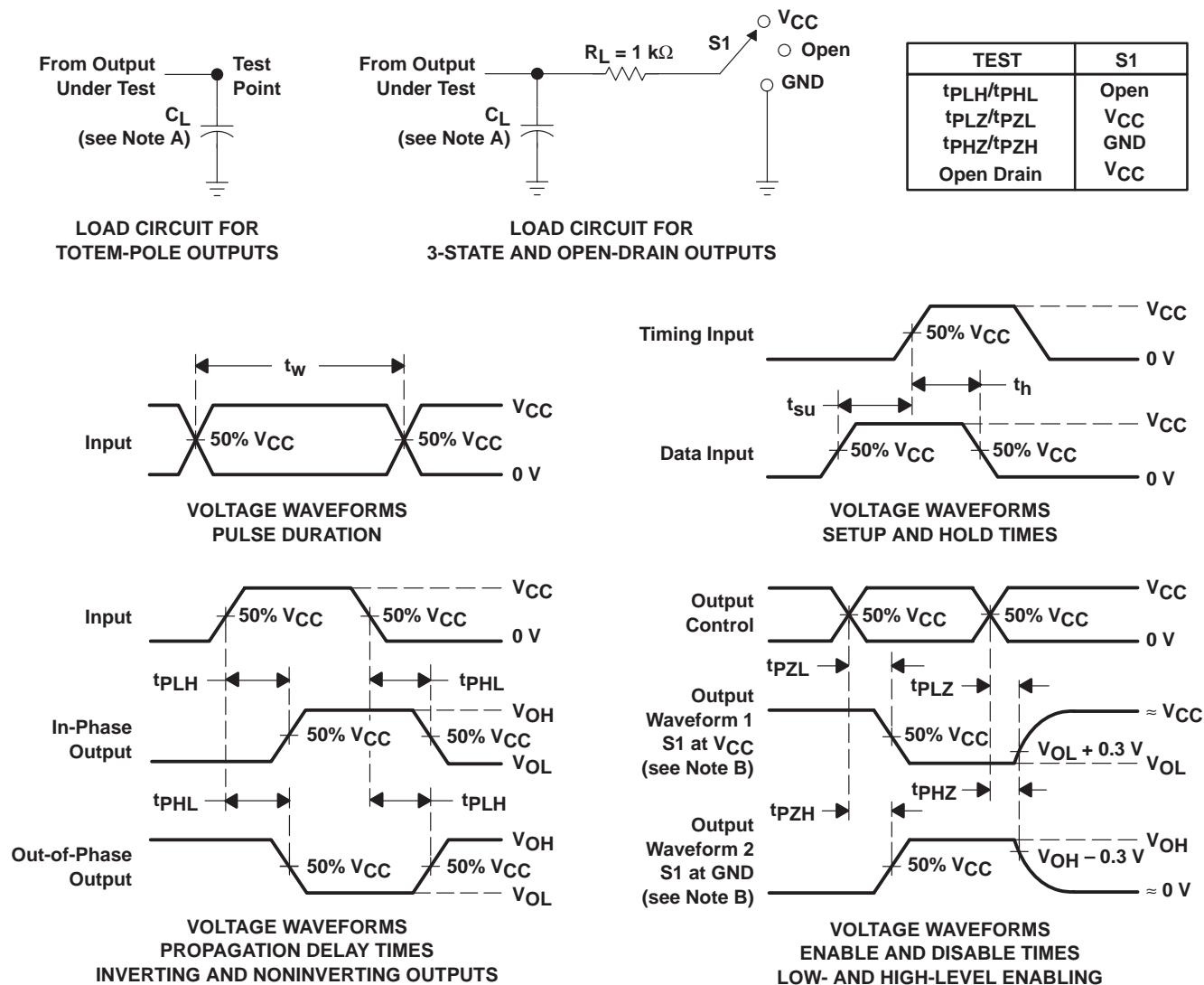
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## 16-BIT BUS TRANSCEIVERS

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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