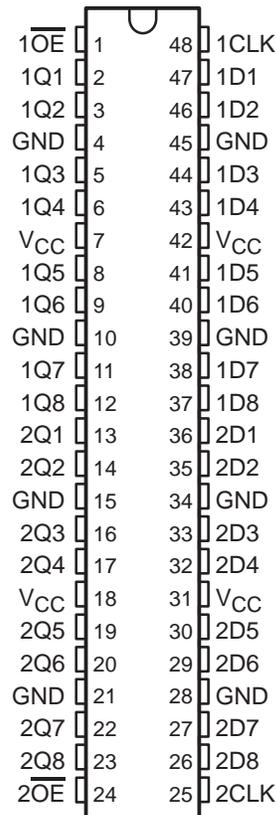


SN54AHC16374, SN74AHC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **3-State Outputs Drive Bus Lines Directly**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16374 . . . WD PACKAGE
SN74AHC16374 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHC16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16374 is characterized for operation from –40°C to 85°C.



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 **TEXAS
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SN54AHC16374, SN74AHC16374

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

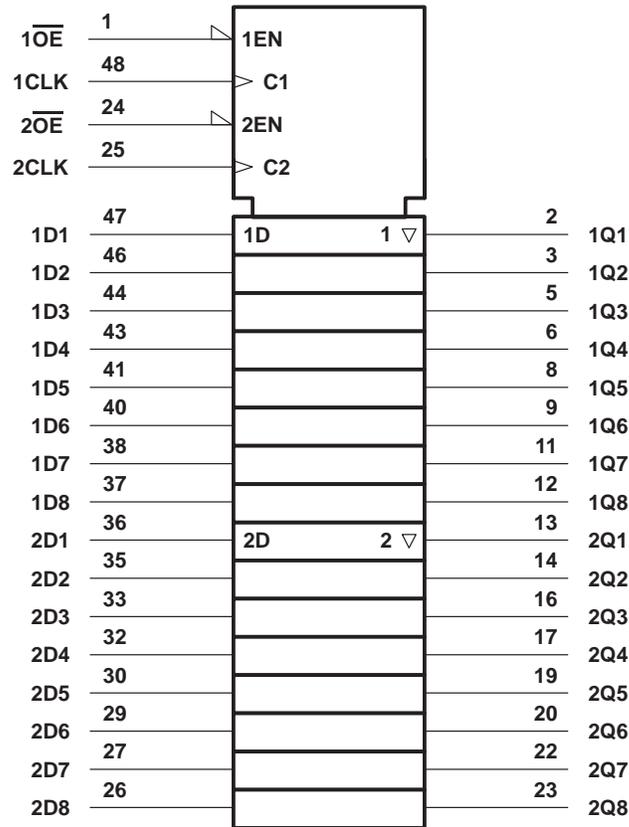
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each 8-bit flip-flop)

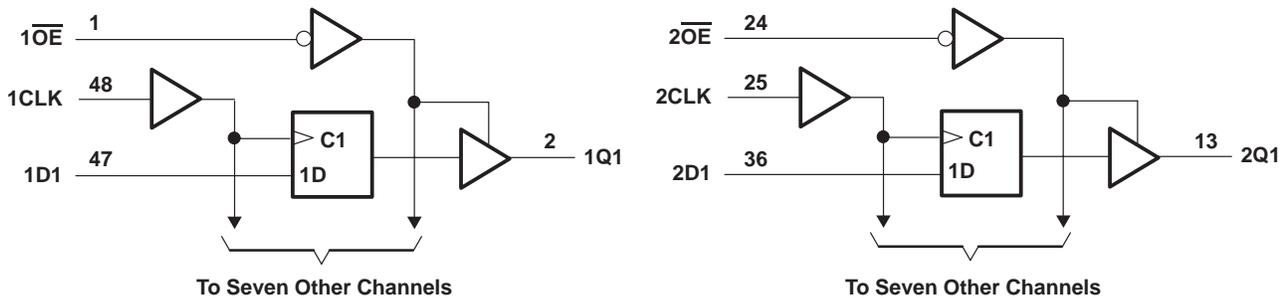
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54AHC16374, SN74AHC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through each V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54AHC16374		SN74AHC16374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5		V
		$V_{CC} = 3$ V		2.1		
		$V_{CC} = 5.5$ V		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		V
		$V_{CC} = 3$ V		0.9		
		$V_{CC} = 5.5$ V		1.65		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		μ A
		$V_{CC} = 3.3$ V ± 0.3 V		–4		mA
		$V_{CC} = 5$ V ± 0.5 V		–8		
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		μ A
		$V_{CC} = 3.3$ V ± 0.3 V		4		mA
		$V_{CC} = 5$ V ± 0.5 V		8		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC16374		SN74AHC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	40	μA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10			10	pF	
C _o	V _O = V _{CC} or GND	5 V		3.5					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHC16374		SN74AHC16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t _{su}	Setup time, data before CLK↑	4.5		4		4		ns
t _h	Hold time, data after CLK↑	2		2		2		ns

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHC16374		SN74AHC16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, CLK high or low	5		5		5		ns
t _{su}	Setup time, data before CLK↑	3		3		3		ns
t _h	Hold time, data after CLK↑	2		2		2		ns

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16374		SN74AHC16374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	80*	130*		70*		70		MHz
			C _L = 50 pF	55	85		50		50		
t _{PLH}	CLK	Q	C _L = 15 pF		9*	15*	1*	17*	1	17	ns
t _{PHL}					9*	15*	1*	17*	1	17	
t _{PZH}	\overline{OE}	Q	C _L = 15 pF		8*	13*	1*	15*	1	15	ns
t _{PZL}					8*	13*	1*	15*	1	15	
t _{PHZ}	\overline{OE}	Q	C _L = 15 pF		9*	14*	1*	16*	1	16	ns
t _{PLZ}					10*	14*	1*	16*	1	16	
t _{PLH}	CLK	Q	C _L = 50 pF		10.6	16.2	1	18.5	1	18.5	ns
t _{PHL}					10.6	16.2	1	18.5	1	18.5	
t _{PZH}	\overline{OE}	Q	C _L = 50 pF		9.6	14.9	1	16	1	16	ns
t _{PZL}					9.6	14.9	1	16	1	16	
t _{PHZ}	\overline{OE}	Q	C _L = 50 pF		10.2	15.5	1	17	1	17	ns
t _{PLZ}					11.8	15.5	1	17	1	17	
t _{sk(o)}			C _L = 50 pF			1.5**				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16374		SN74AHC16374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	130*	185*		110*		110		MHz
			C _L = 50 pF	85	120		75		75		
t _{PLH}	CLK	Q	C _L = 15 pF		5.4*	9.1*	1*	10.1*	1	10.1	ns
t _{PHL}					5.4*	9.1*	1*	10.1*	1	10.1	
t _{PZH}	\overline{OE}	Q	C _L = 15 pF		5.1*	9.1*	1*	10.1*	1	10.1	ns
t _{PZL}					5.1*	9.1*	1*	10.1*	1	10.1	
t _{PHZ}	\overline{OE}	Q	C _L = 15 pF		5*	9.5*	1*	10.5*	1	10.5	ns
t _{PLZ}					5*	9.5*	1*	10.5*	1	10.5	
t _{PLH}	CLK	Q	C _L = 50 pF		6.9	10.1	1	11.5	1	11.5	ns
t _{PHL}					6.9	10.1	1	11.5	1	11.5	
t _{PZH}	\overline{OE}	Q	C _L = 50 pF		6.6	10.1	1	11.5	1	11.5	ns
t _{PZL}					6.6	10.1	1	11.5	1	11.5	
t _{PHZ}	\overline{OE}	Q	C _L = 50 pF		6.1	10.5	1	11.5	1	11.5	ns
t _{PLZ}					6.1	10.5	1	11.5	1	11.5	
t _{sk(o)}			C _L = 50 pF			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC16374			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.36	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.16	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

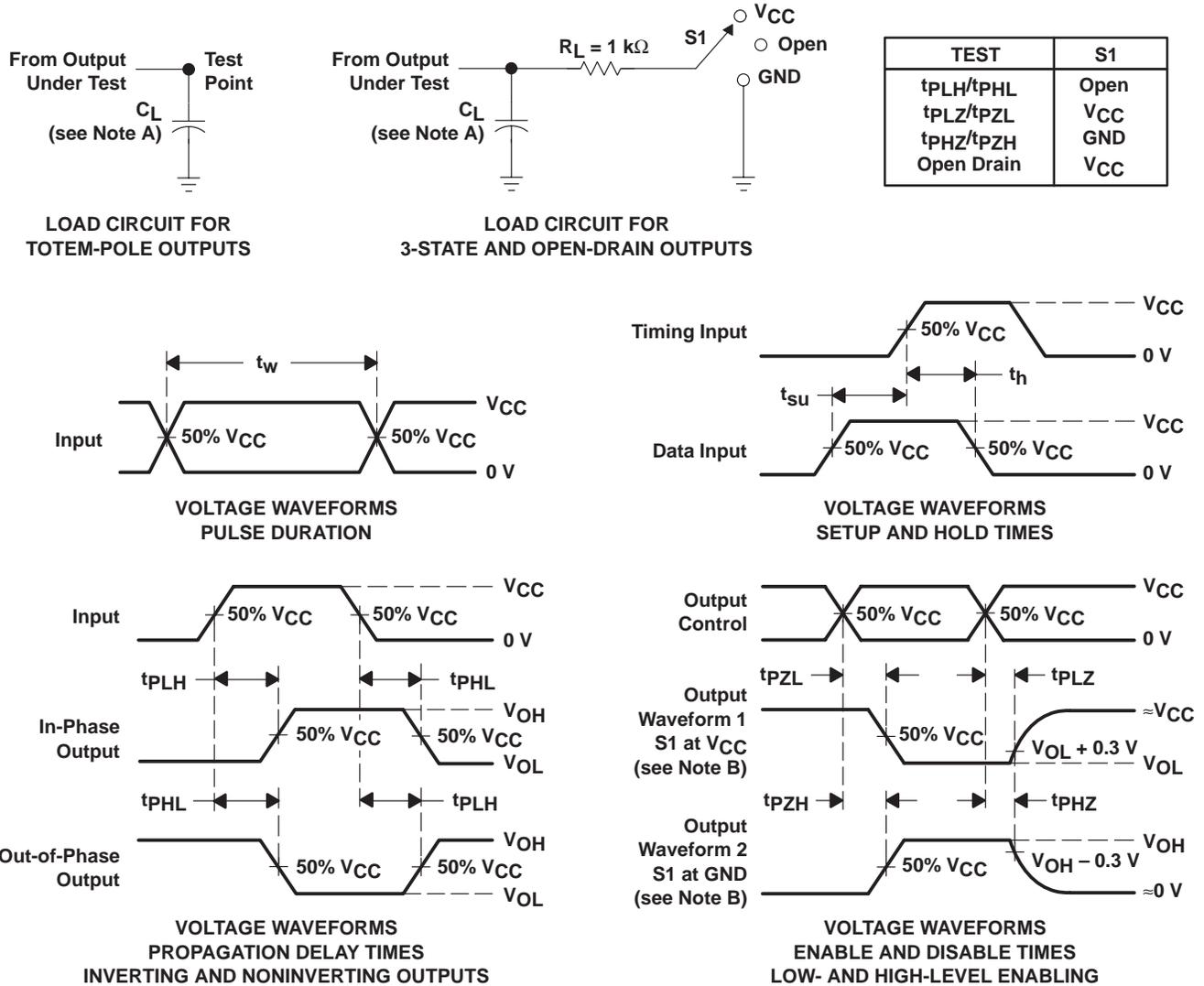
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	32	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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