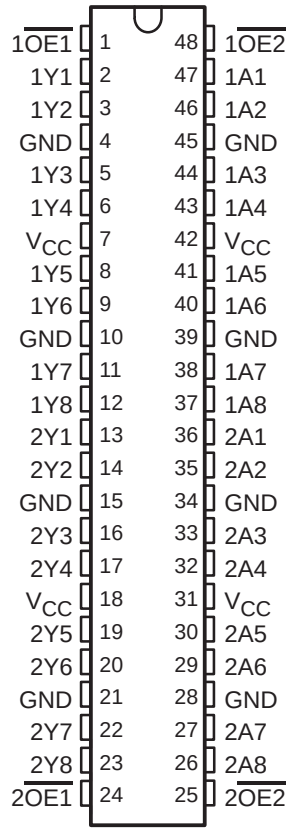
- **Members of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Distributed $V_{CC}$ and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54AHCT16540 . . . WD PACKAGE**
**SN74AHCT16540 . . . DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




## description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

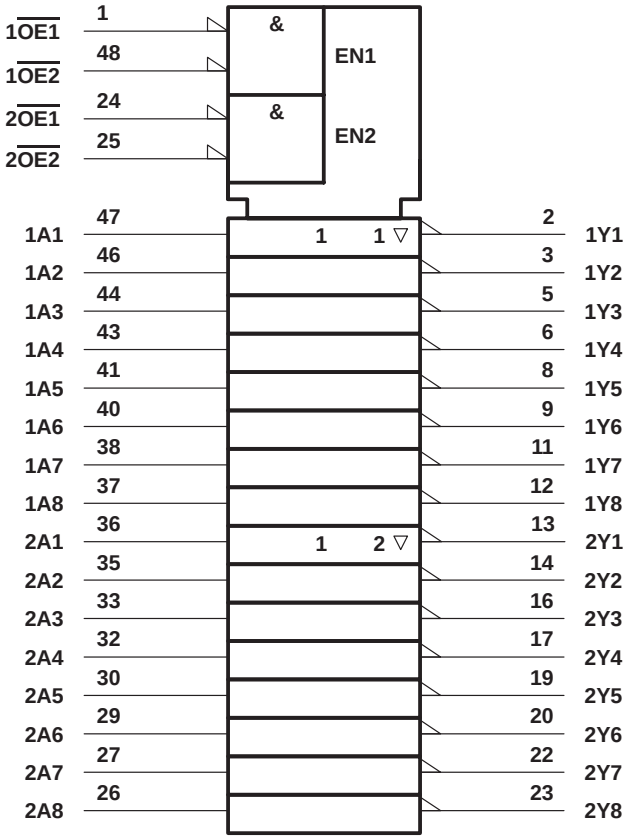
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16540 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each 8-bit buffer/driver)**

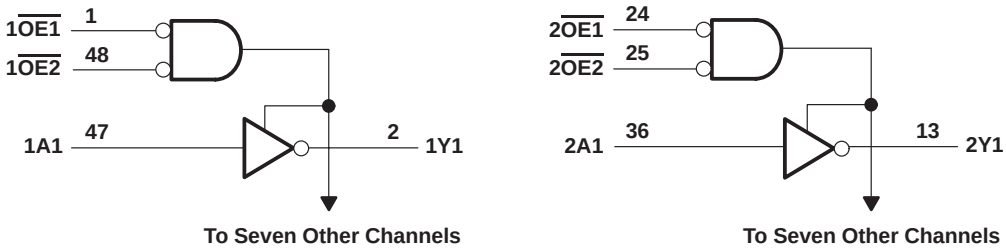
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
DL package . . . . . 63°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

| | | SN54AHCT16540 | | SN74AHCT16540 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |



NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT16540 | | SN74AHCT16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | | ±1 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |



* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHCT16540 | | SN74AHCT16540 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4** | 8.5** | 1** | 10** | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4** | 8.5** | 1** | 10** | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.5** | 10.4** | 1** | 12** | 1 | 12 | ns |
| $t_{PZL}$ | | | | | 5.5** | 10.4** | 1** | 12** | 1 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5** | 10.4** | 1** | 12** | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 5** | 10.4** | 1** | 12** | 1 | 12 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6 | 9.5 | 1** | 11** | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6 | 9.5 | 1 | 11 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.5 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PZL}$ | | | | | 7.5 | 11.4 | 1 | 13 | 1 | 13 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | 13 | 1 | 13 | ns |
| $t_{PLZ}$ | | | | | 8 | 11.4 | 1 | 13 | 1 | 13 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1*** | | | | 1 | ns |



** On products compliant to MIL-PRF-38535, this parameter is not production tested.
*** On products compliant to MIL-PRF-38535, this parameter does not apply.

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

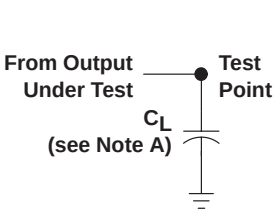
| PARAMETER | | SN74AHCT16540 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.7 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are for surface-mount packages only.

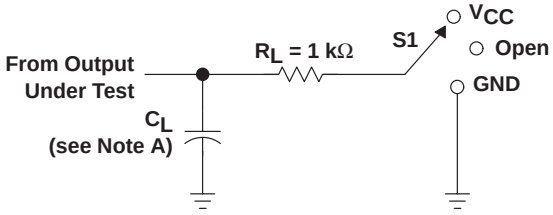
## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 14 | pF |

## PARAMETER MEASUREMENT INFORMATION

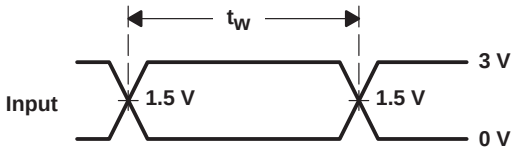



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

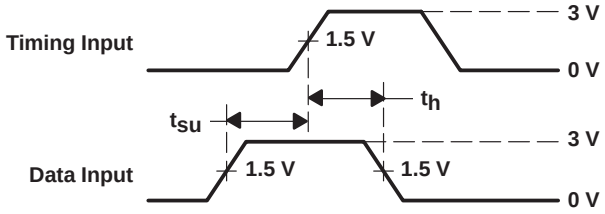



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

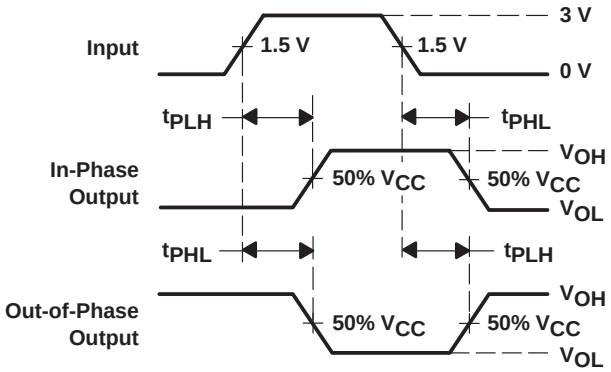
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



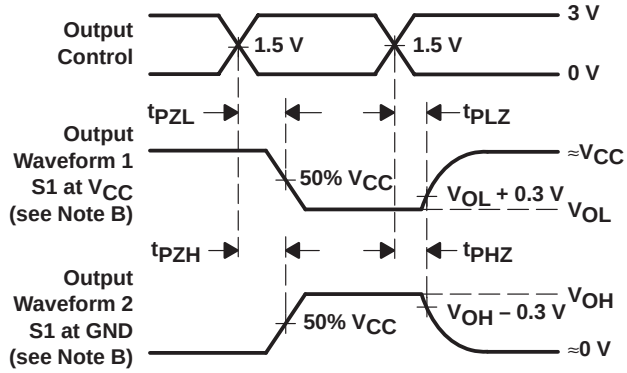

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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