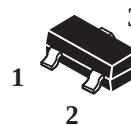
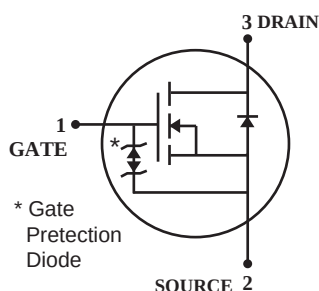


### N-Channel Enhancement Mode Power MOSFET

**(Pb)** Lead(Pb)-Free



**SOT-23**

#### Features:

- \* Low on-resistance.
- \* Fast switching speed.
- \* Low-voltage drive.
- \* Easily designed drive circuits.
- \* Easy to parallel.
- \* Pb-Free package is available.
- \* Esd Protected:2000V

#### Maximum Ratings( $T_A = 25^\circ\text{C}$ Unless Otherwise Specified)

| Parameter               |            | Symbol         | Limits          | Unit             |
|-------------------------|------------|----------------|-----------------|------------------|
| Drain-source voltage    |            | $V_{DSS}$      | 60              | V                |
| Gate-source voltage     |            | $V_{GSS}$      | $\pm 20$        | V                |
| Drain current           | Continuous | $I_D$          | 115             | mA               |
|                         | Pulsed     | $I_{DP}^{*1}$  | 0.8             | A                |
| Drain reverse current   | Continuous | $I_{DR}$       | 115             | mA               |
|                         | Pulsed     | $I_{DRP}^{*1}$ | 0.8             | A                |
| Total power dissipation |            | $P_D^{*2}$     | 225             | mW               |
| Channel temperature     |            | $T_{ch}$       | 150             | $^\circ\text{C}$ |
| Storage temperature     |            | $T_{stg}$      | $-55 \sim +150$ | $^\circ\text{C}$ |

1.  $P_w \leq 10\mu\text{s}$ , Duty cycle  $\leq 1\%$ .

2. When mounted on a  $1 \times 0.75 \times 0.062$  inch glass epoxy board.

#### Device Marking

2N7002K = RK

## Electrical characteristics (Ta=25°C)

| Parameter                                                                                  | Symbol         | Min. | Typ. | Max.     | Unit     |
|--------------------------------------------------------------------------------------------|----------------|------|------|----------|----------|
| Gate-source leakage current<br>$V_{GS}=\pm 20V, V_{DS}=0V$                                 | $I_{GSS}$      | –    | –    | $\pm 10$ | $\mu A$  |
| Drain-source breakdown voltage<br>$I_D=10\mu A, V_{GS}=0V$                                 | $V_{(BR) DSS}$ | 60   | –    | –        | V        |
| Zero gate voltage drain current<br>$V_{DS}=60V, V_{GS}=0V$                                 | $I_{DSS}$      | –    | –    | 1        | $\mu A$  |
| Gate threshold voltage<br>$V_{DS}=V_{GS}, I_D=250\mu A$                                    | $V_{GS(th)}$   | 1    | 1.85 | 2.5      | V        |
| Drain-source on-state resistance<br>$I_D=0.5A, V_{GS}=10V$<br>$I_D=0.05A, V_{GS}=5V$       | $R_{DS(on)}^*$ | –    | –    | 7.5      | $\Omega$ |
|                                                                                            |                | –    | –    | 7.5      |          |
| Forward transfer admittance<br>$V_{DS}=10V, I_D=0.2A$                                      | $ Y_{fs} ^*$   | 80   | –    | –        | mS       |
| Input capacitance<br>$V_{DS}=25V, V_{GS}=0V, f=1MHz$                                       | $C_{iss}$      | –    | 25   | 50       | pF       |
| Output capacitance<br>$V_{DS}=25V, V_{GS}=0V, f=1MHz$                                      | $C_{oss}$      | –    | 10   | 25       | pF       |
| Reverse transfer capacitance<br>$V_{DS}=25V, V_{GS}=0V, f=1MHz$                            | $C_{rss}$      | –    | 3.0  | 5.0      | pF       |
| Turn-on delay time<br>$I_D=200mA, V_{DD}=30V, V_{GS}=10V, R_L=150\Omega, R_{GS}=10\Omega$  | $t_{d(on)}^*$  | –    | 12   | 20       | ns       |
| Turn-off delay time<br>$I_D=200mA, V_{DD}=30V, V_{GS}=10V, R_L=150\Omega, R_{GS}=10\Omega$ | $t_{d(off)}^*$ | –    | 20   | 30       | ns       |

\*  $PW \leq 300\mu s$ , Duty cycle  $\leq 1\%$

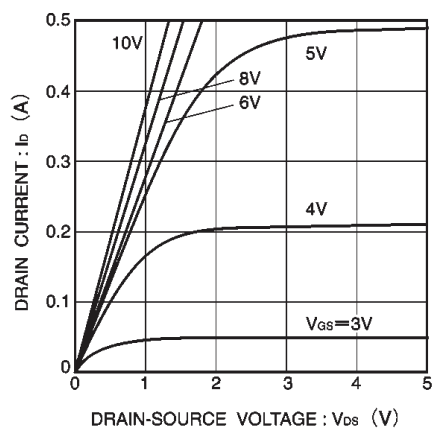


Fig.1 Typical output characteristics

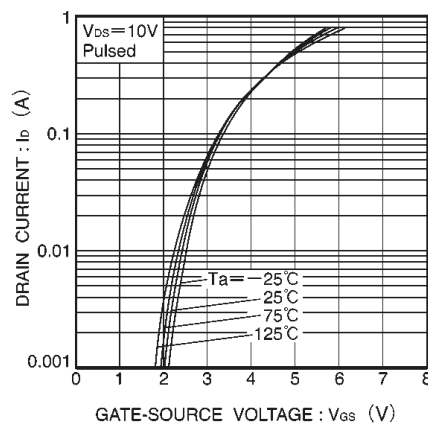


Fig.2 Typical transfer characteristics

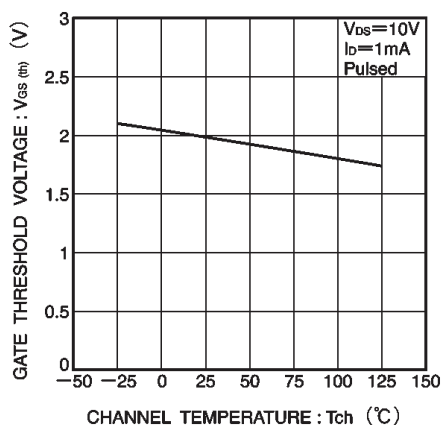


Fig.3 Gate threshold voltage vs. channel temperature

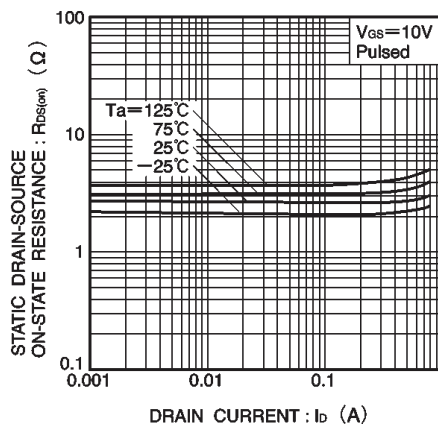


Fig.4 Static drain-source on-state resistance vs. drain current ( I )

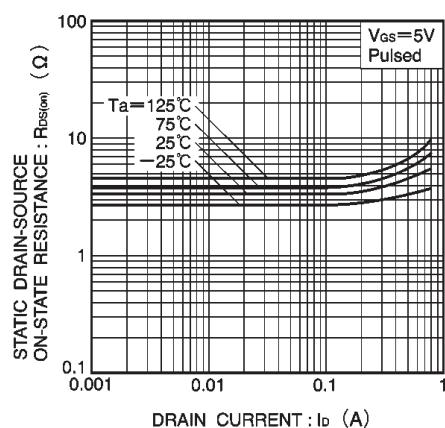


Fig.5 Static drain-source on-state resistance vs. drain current ( II )

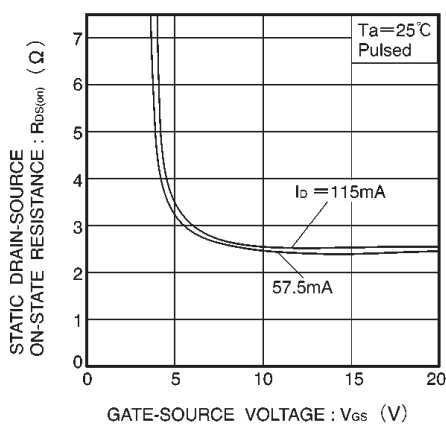


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

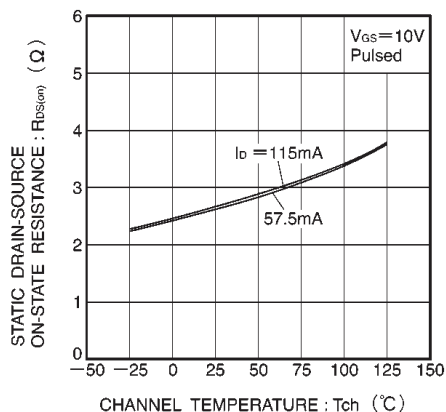


Fig.7 Static drain-source on-state resistance vs. channel temperature

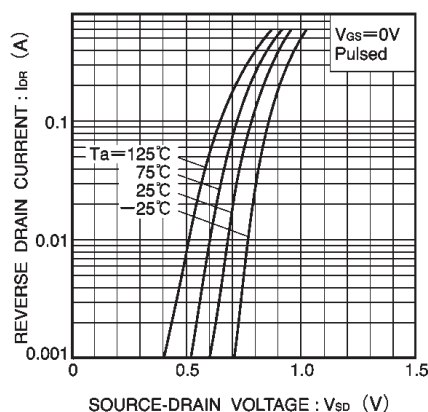


Fig.8 Reverse drain current vs. source-drain voltage (I)

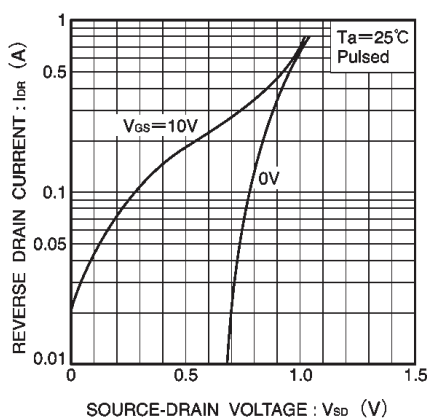


Fig.9 Reverse drain current vs. source-drain voltage (II)

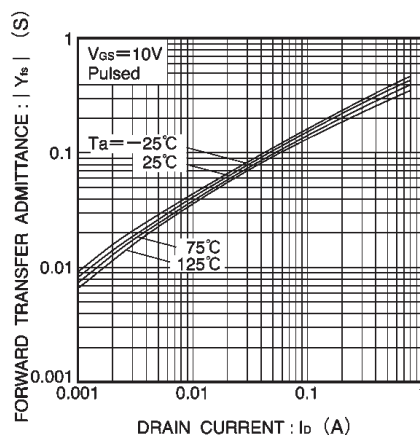


Fig.10 Forward transfer admittance vs. drain current

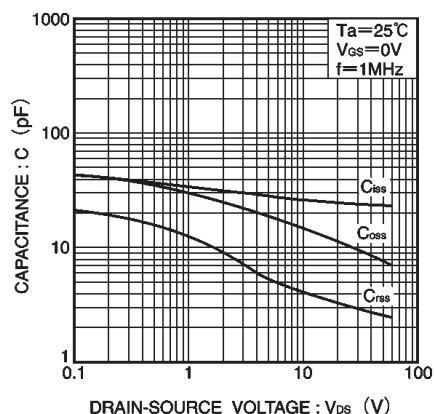


Fig.11 Typical capacitance vs. drain-source voltage

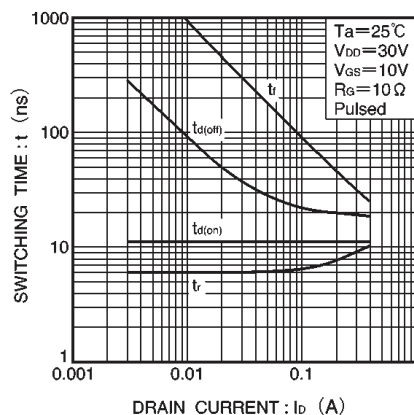


Fig.12 Switching characteristics  
(See Figures 13 and 14 for the measurement circuit and resultant waveforms)

## Switching characteristics measurement circuit

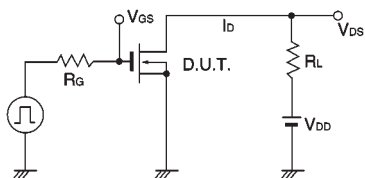


Fig.13 Switching time measurement circuit

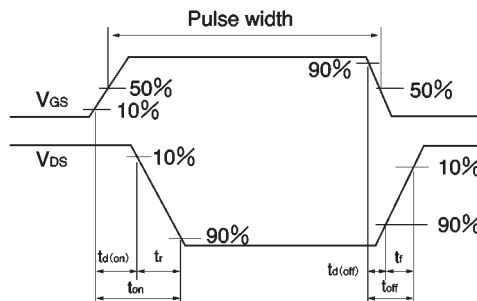
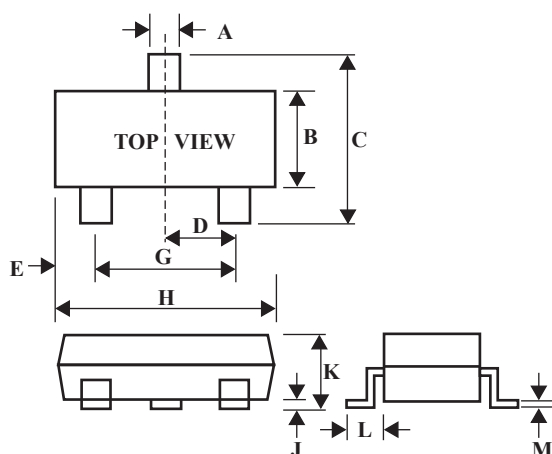


Fig.14 Switching time waveforms

## SOT-23 Outline Dimension



| SOT-23 |       |      |
|--------|-------|------|
| Dim    | Min   | Max  |
| A      | 0.35  | 0.51 |
| B      | 1.19  | 1.40 |
| C      | 2.10  | 3.00 |
| D      | 0.85  | 1.05 |
| E      | 0.46  | 1.00 |
| G      | 1.70  | 2.10 |
| H      | 2.70  | 3.10 |
| J      | 0.01  | 0.13 |
| K      | 0.89  | 1.10 |
| L      | 0.30  | 0.61 |
| M      | 0.076 | 0.25 |