

**2N80**

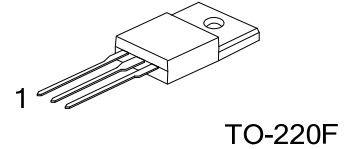
Preliminary

Power MOSFET**2 Amps, 800 Volts****N-CHANNEL POWER MOSFET**

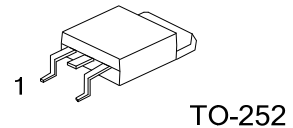
■ DESCRIPTION

The UTC **2N80** is an N-channel mode Power FET using UTC's advanced technology to provide customers planar stripe and DMOS technology. This technology is specialized in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **2N80** is universally applied in high efficiency switch mode power supply.



TO-220F



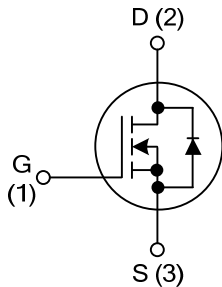
TO-252

■ FEATURES

* 2.4A, 800V, $R_{DS(on)} = 6.3\Omega$ @ $V_{GS} = 10V$

* High switching speed

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N80L-TF3-T	2N80G-TF3-T	TO-220F	G	D	S	Tube
2N80L-TN3-R	2N80G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

2N80L-TF3-T (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube, R: Tape Reel (2) TF3: TO-220F, TN3: TO-252 (3) G: Halogen Free, L: Lead Free
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■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	800	V
Gate-Source Voltage		V_{GS}	± 30	V
Avalanche Current (Note 1)		I_{AR}	2.4	A
Drain Current	Continuous	I_D	2.4	A
	Pulsed (Note 1)	I_{DM}	9.6	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	180	mJ
	Repetitive (Note 1)	E_{AR}	8.5	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.0	V/ns
Power Dissipation	TO-220F	P_D	24	W
	TO-252		43	W/ $^{\circ}\text{C}$
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^{\circ}\text{C}$

Note : Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	PACKAGE	SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F	θ_{JA}	62.5	$^{\circ}\text{C/W}$
	TO-252		110	$^{\circ}\text{C/W}$
Junction to Case	TO-220F	θ_{JC}	5.2	$^{\circ}\text{C/W}$
	TO-252		2.85	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	800			V
Breakdown Voltage Temperature Coefficient		ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =250μA		0.9		V/°C
Drain-Source Leakage Current		I _{DSS}	V _{DS} =800V, V _{GS} =0V			10	μA
			V _{DS} =640V, T _C =125°C			100	
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3.0		5.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.2A		4.9	6.3	Ω
Forward Transconductance (Note 4)		g _{FS}	V _{DS} =50V, I _D =1.2A		2.65		S
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		425	550	pF
Output Capacitance		C _{OSS}			45	60	pF
Reverse Transfer Capacitance		C _{RSS}			5.5	7.0	pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 4,5)		Q _G	V _{GS} =10V, V _{DS} =640V, I _D =2.4A		12	15	nC
Gate to Source Charge (Note 4,5)		Q _{GS}			2.6		nC
Gate to Drain Charge (Note 4,5)		Q _{GD}			6.0		nC
Turn-ON Delay Time (Note 4,5)		t _{D(ON)}	V _{DD} =400V, I _D =2.4A, R _G =25Ω		12	35	ns
Rise Time (Note 4,5)		t _R			30	70	ns
Turn-OFF Delay Time (Note 4,5)		t _{D(OFF)}			25	60	ns
Fall-Time (Note 4,5)		t _F			28	65	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				2.4	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				9.6	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =2.4A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 4)		t _{RR}	I _S =2.4A, V _{GS} =0V, dI _F /dt=100A/μs		480		ns
Reverse Recovery Charge (Note 4)		Q _{RR}			2.0		μC

Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L = 59mH, I_{AS} = 2.4A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C

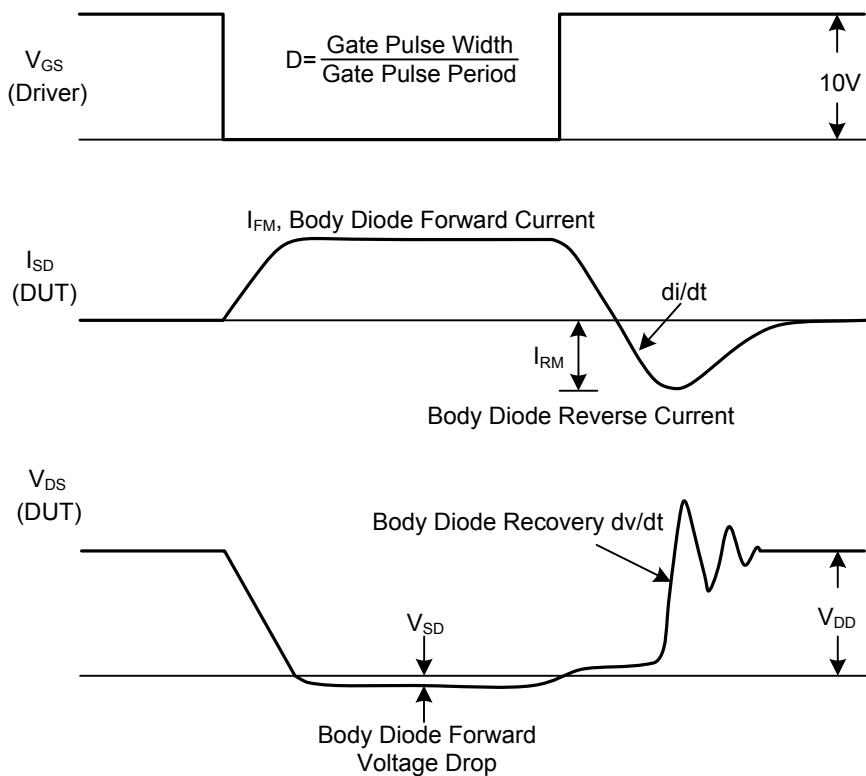
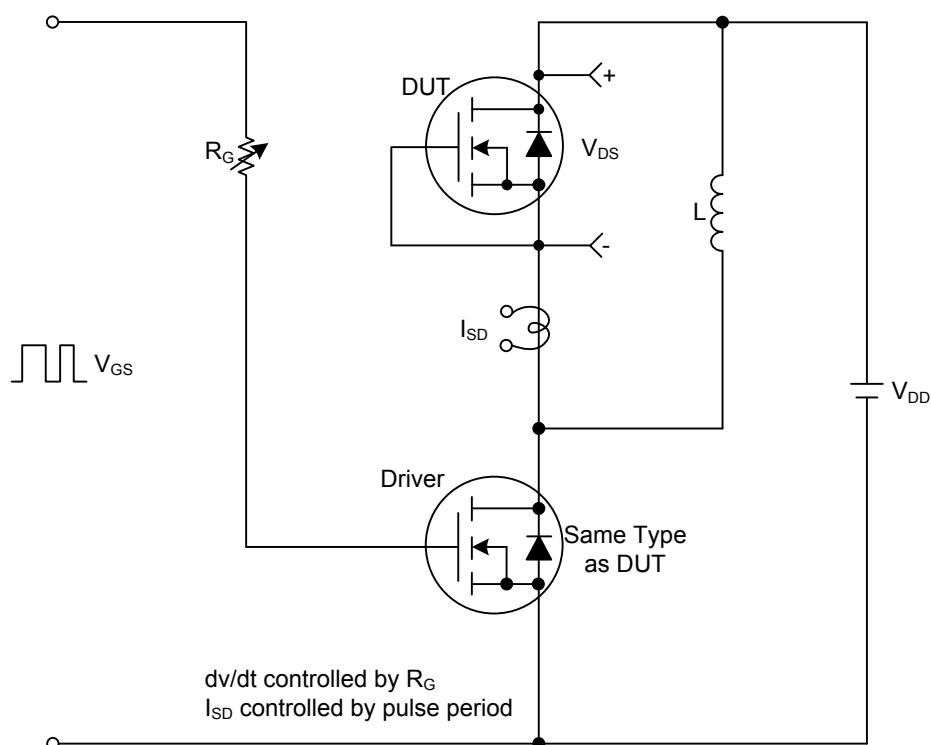
3. I_{SD} ≤ 2.4A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

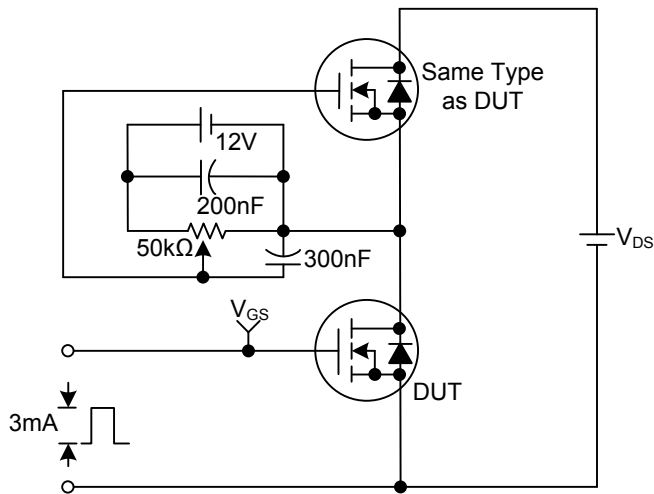
5. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

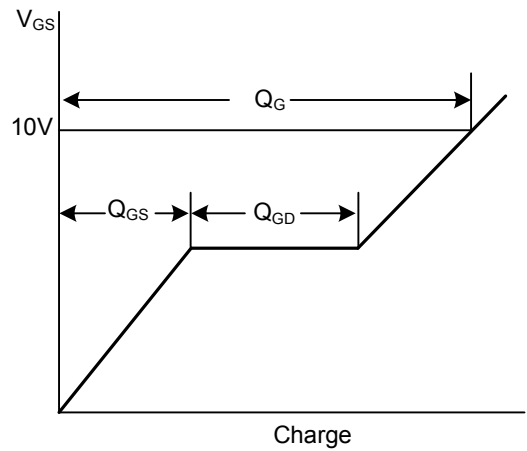
Peak Diode Recovery dv/dt Test Circuit & Waveforms



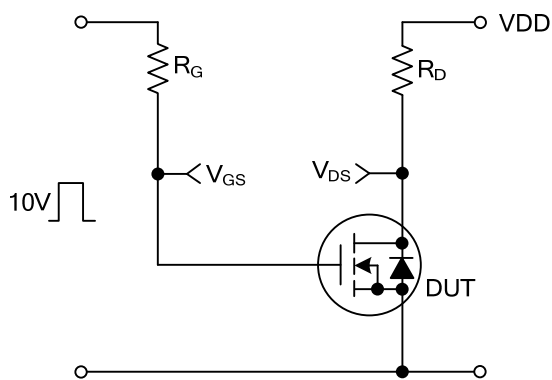
Gate Charge Test Circuit



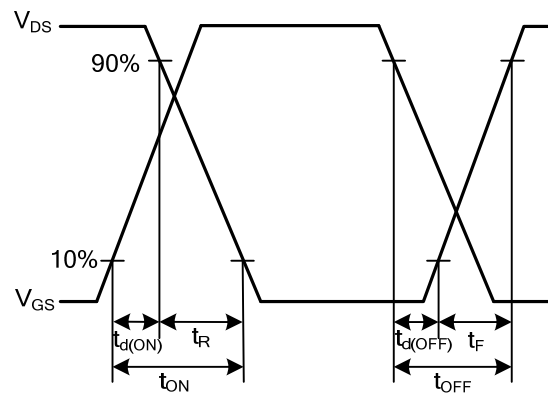
Gate Charge Waveforms



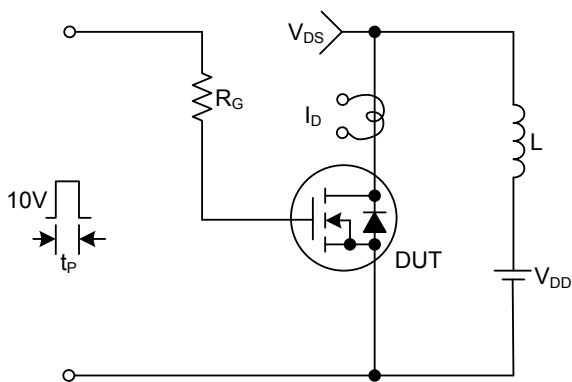
Resistive Switching Test Circuit



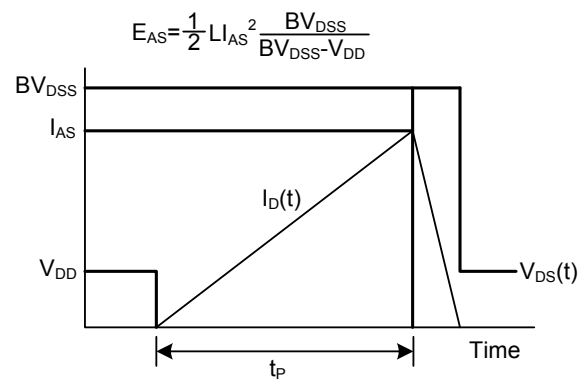
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



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