

STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME Main Power Supply For TFT-LCD Display Module

TYPE **B D 8 1 5 0 K V T**

FEATURES 5-channel outputs for TFT-LCD Display
11-channel OP-AMP included

●ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	LIMITS	UNIT
Power Supply Voltage	VCC	15	V
Regulator Supply Voltage	REGVCC	15	V
Driver Supply Voltage	PVCC	15	V
Junction Temperature	Tjmax	125	°C
Power Dissipation	Pd	1000*1	mW
Operating Temperature Range	Topr	-30~85	°C
Storage Temperature Range	Tstg	-55~150	°C

*1 Pd derated at 10mW/°C for temperatures above Ta=25°C,
mounted on 70×70×1.6mm Glass-epoxy PCB.

●OPERATING CONDITIONS (Ta=-30°C~+85°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power Supply Voltage	VCC	2.7	13	V
Regulator Supply Voltage	REGVCC	4.5	14.7	V
Driver Supply Voltage	PVCC	2.7	13	V

★This product is not designed for protection against radioactive rays.

★The product described in this specification is a strategic product(and/or Service) subject to COCOM regulations. It should not be exported without Authorization from the appropriate government.

Status of this document

The Japanese version of this document is the formal specification.

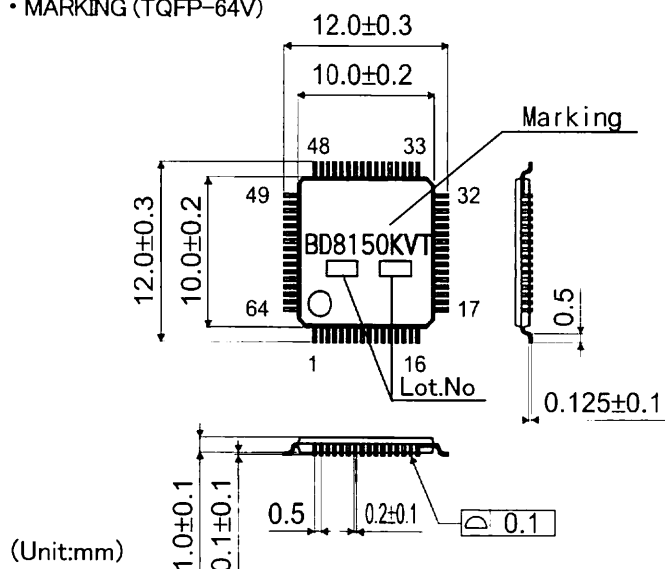
A customer may use this translation version only for a reference to help reading the formal version.

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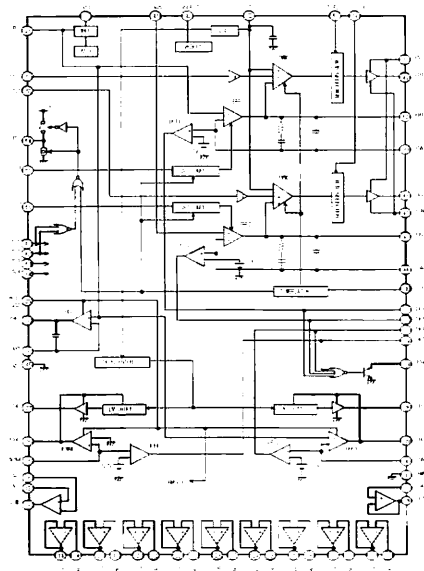
●ELECTRICAL CHARACTERISTICS (Unless otherwise specified VCC=5V,REGVCC=12V,Ta=25°C)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
[ERR AMP1,2 BLOCK]						
Input Offset Voltage	Vos12	-10	0	10	mV	
Feed Back Voltage	FB1	1.225	1.25	1.275	V	ERRAMP1 Only
[PWM&DRV BLOCK]						
Sink Current	Ipsk12	70	130	200	mA	GD1,2=5V
Source Current	Ipsc12	-245	-160	-85	mA	GD1,2=0V
[OSCILLATOR BLOCK]						
Switching Frequency	Fsw12	0.8	1.0	1.2	MHz	
[CHARGE PUMP DRIVER ERR AMP3,4 BLOCK]						
Feed Back Voltage	FB3	1.212	1.25	1.288	V	
	FB4	—	0	—	V	
[DRIVER BLOCK]						
Switching Frequency	Fsw34	200	250	300	kHz	
[LOW DROPOUT REGULATOR]						
Feed Back Voltage	FBR	1.237	1.25	1.263	V	Buffer, I _o =-10mA
Short Current	I _o	—	-130	-50	mA	VREG=0V
Load Regulation	RegL	—	1	10	mV	I _o =1→10mA
[OP-AMP BLOCK]						
Input Offset Voltage	Voso	-10	0	10	mV	
Drive Current	I _{oo}	20	50	—	mA	
Load Regulation	ΔV _o	—	1	10	mV	I _o =+1~-1mA
Output Voltage High	V _{oh}	REGVCC-1.0	REGVCC-0.8	—	V	I _o =-1mA, I _N +=REGVCC
Output Voltage Low	V _{oh} l	—	0.1	0.16	V	I _o =1mA, I _N +=0V
[BG BLOCK]						
BG Voltage	V _{ref}	1.225	1.250	1.275	V	I _o =-0.1mA
Short Current	I _{ovr}	0.2	1	—	mA	BG=0V
[VREF17 BLOCK]						
VREF17 Voltage	V _{ref} 17	1.666	1.700	1.734	V	I _o =-0.1mA
Short Current	I _{ovr} 17	0.2	1	—	mA	VREF17=0V
[UNDER VOLTAGE LOCK OUT BLOCK]						
Threshold Voltage	V _{uv} lo	2.327	2.45	2.573	V	
[SUPPLY CURRENT]						
Stand-by Current	I _{stb}	—	0	10	μA	
Average Supply Current	I _{cc}	1.1	2	2.9	mA	

●PHYSICAL DIMENSION • MARKING (TQFP-64V)



● BLOCK DIAGRAM



*Please refer to Technical note concerning application circuit, and etc.

● PIN NO. & FUNCTION TABLE

PIN NO.	PIN NAME	FUNCTION	PIN NO.	PIN NAME	FUNCTION
1	DET1	DC/DC detector output 1	33	SCP	Connect timer latch capacitor
2	DET2	DC/DC detector output 2	34	ENABLE	All channel output enable
3	DET3	Charge pump detector output 3	35	NON4	Charge pump feed back input 4
4	DET4	Charge pump detector output 4	36	FB4	Charge pump E/A output 4
5	IN0	Buffer amp 0 input	37	CD4	Charge pump driver output 4
6	IN1	Buffer amp 1 input	38	CD3	Charge pump driver output 3
7	IN2	Buffer amp 2 input	39	FB3	Charge pump E/A output 3
8	IN3	Buffer amp 3 input	40	INV3	Charge pump feed back input 3
9	IN4	Buffer amp 4 input	41	BG	Reference voltage monitor
10	IN5	Buffer amp 5 input	42	VREF17	1.7V Reference Voltage
11	IN6	Buffer amp 6 input	43	NON2	DC/DC E/A non inverting input 2
12	IN7	Buffer amp 7 input	44	INV2	DC/DC E/A inverting input 2
13	IN8	Buffer amp 8 input	45	FB2	DC/DC E/A output 2
14	IN9	Buffer amp 9 input	46	GND	Ground
15	IN+	Op-amp non inverting input	47	PGND	Power ground
16	IN-	Op-amp inverting input	48	GD2	DC/DC driver output 2
17	AMPGND	Buffer amp and op-amp ground	49	GD1	DC/DC driver output 1
18	COM	Op-amp output	50	PVCC	Power VCC supply
19	OUT9	Buffer amp 9 output	51	VCC	VCC supply
20	OUT8	Buffer amp 8 output	52	FB1	DC/DC E/A output 1
21	OUT7	Buffer amp 7 output	53	INV1	DC/DC E/A inverting input 1
22	OUT6	Buffer amp 6 output	54	PG	Pch FET switch driver output
23	OUT5	Buffer amp 5 output	55	SS1	Connect soft start capacitor 1
24	OUT4	Buffer amp 4 output	56	SS2	Connect soft start capacitor 2
25	OUT3	Buffer amp 3 output	57	UDSEL1	Step up/down select switch 1
26	OUT2	Buffer amp 2 output	58	UDSEL2	Step up/down select switch 2
27	OUT1	Buffer amp 1 output	59	DTC1	Dead time control voltage input1
28	OUT0	Buffer amp 0 output	60	DTC2	Dead time control voltage input2
29	REGVCC	Charge pump, Regulator, op-amp and buffer amp power supply	61	CTL4	Charge pump control switch 4
30	VREG	Regulator output	62	CTL3	Charge pump control switch 3
31	INV5	Regulator negative feed back input	63	CTL2	DC/DC control switch 2
32	CT	Ramp wave monitor	64	CTL1	DC/DC control switch 1

●Operation Notes

1. Absolute maximum range

This product are produced with strict quality control, but might be destroyed in using beyond absolute maximum ratings. Open IC destroyed a failure mode cannot be defined (like Short mode, or Open mode). Therefore physical security countermeasure, like fuse, is to be given when a specified mode to be beyond absolute maximum ratings is considered.

2. Ground potential

GND terminal should be a lowest voltage potential every state.

Please make sure all pins which is over ground even if include transient feature.

3. Setting of heat

Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions..

4. Short Circuit between Terminal and Soldering

Don' t short-circuit between Output pin and VDD pin, Output pin and GND pin, or VDD pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

5. Electromagnetic Field

Mal-function may happen when the device is used in the strong electromagnetic field.

6. Ground wiring patterns

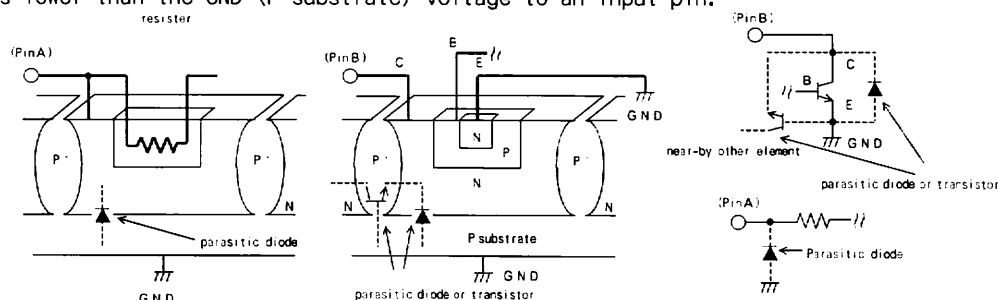
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

7. This IC is a monolithic IC which has P+ isolation in the P substrate and between the various pins.

A P-N junction is formed from this P layer and the N layer of each pin.

For example, when a resistor and a transistor is connected to a pin.

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly, you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.



SIMPLIFIED STRUCTURE OFBI-POLAR IC

8. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

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