

PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL[®] CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

- **Choice of Operating Speeds**
 High-Speed, A Devices . . . 25 MHz Min
 Half-Power, A-2 Devices . . . 16 MHz Min
- **Choice of Input/Output Configuration**
- **Package Options Include Both Ceramic DIP and Chip Carrier in Addition to Ceramic Flat Package**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORT S
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

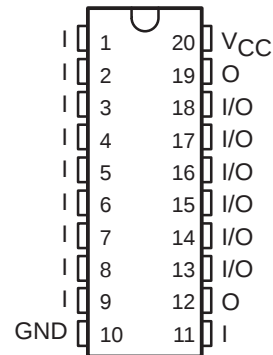
These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

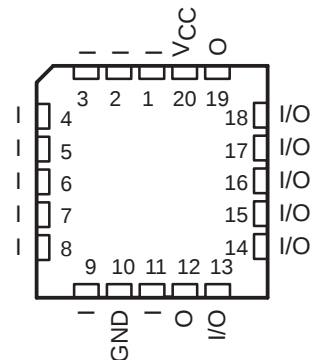
**PAL16L8'
J OR W PACKAGE**

(TOP VIEW)



**PAL16L8'
FK PACKAGE**

(TOP VIEW)



PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



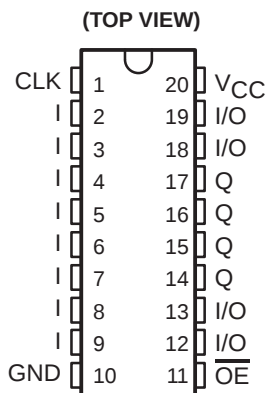
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1992, Texas Instruments Incorporated

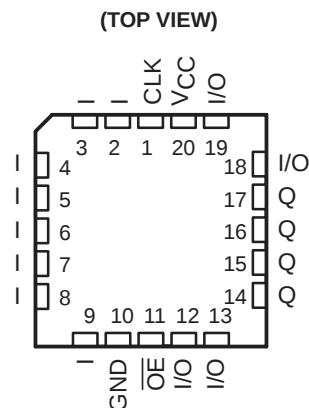
PAL16R4AM, PAL16R4A-2M, PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL[®] CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

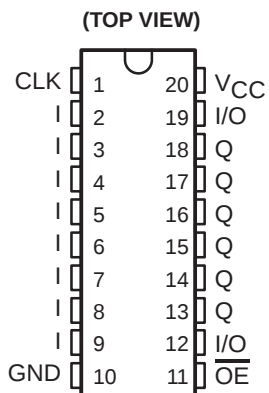
PAL16R4'
J OR W PACKAGE



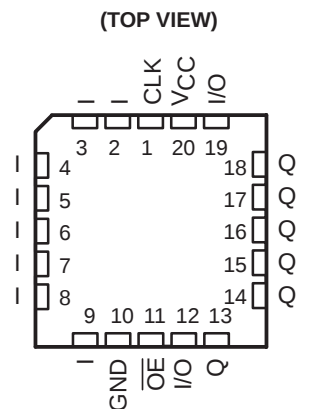
PAL16R4'
FK PACKAGE



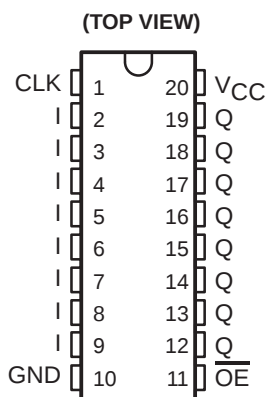
PAL16R6'
J OR W PACKAGE



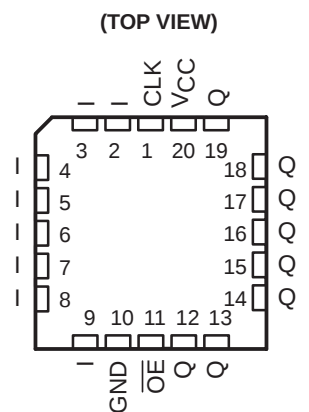
PAL16R6'
FK PACKAGE



PAL16R8'
J OR W PACKAGE



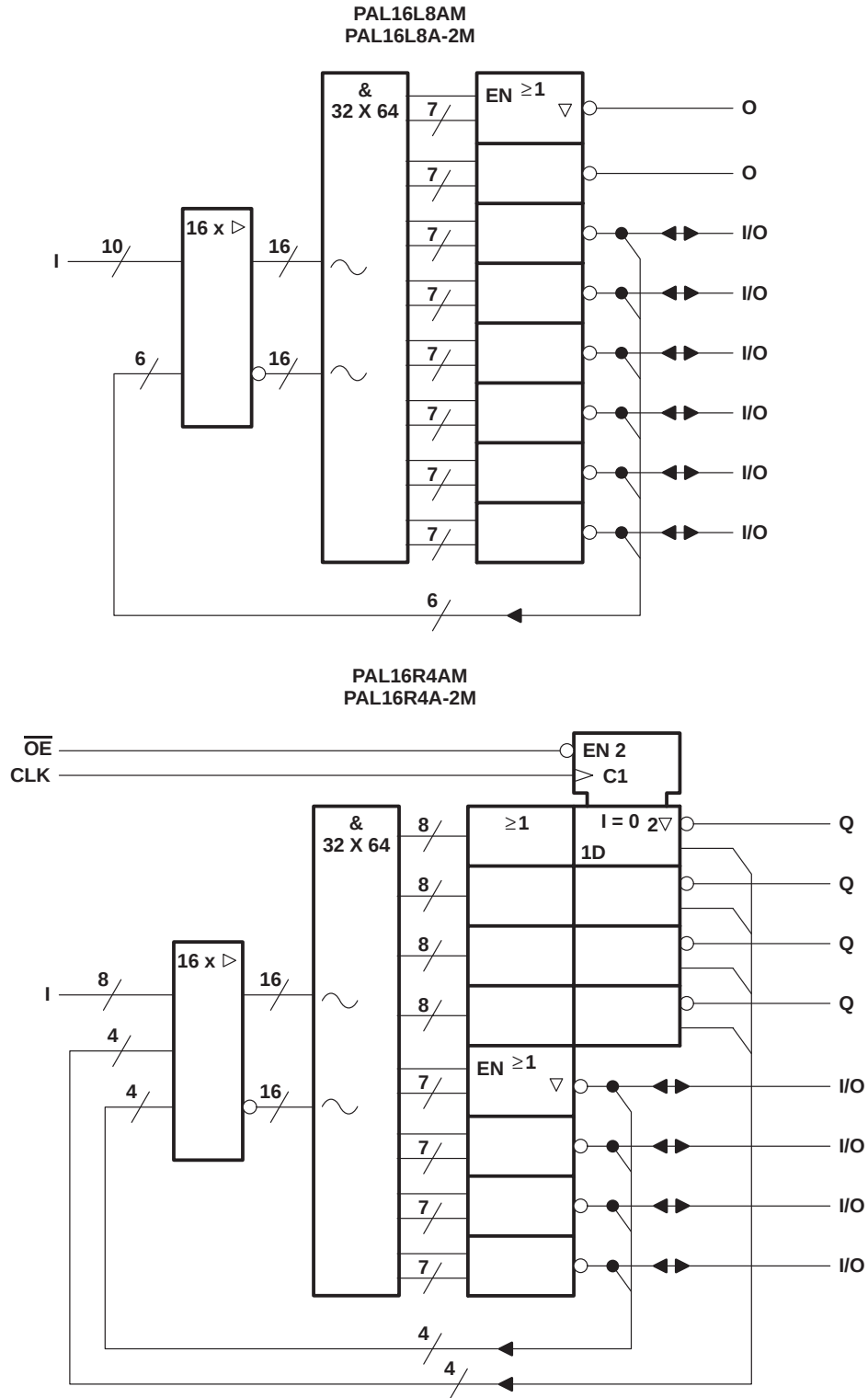
PAL16R8'
FK PACKAGE



PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M STANDARD HIGH-SPEED PAL[®] CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

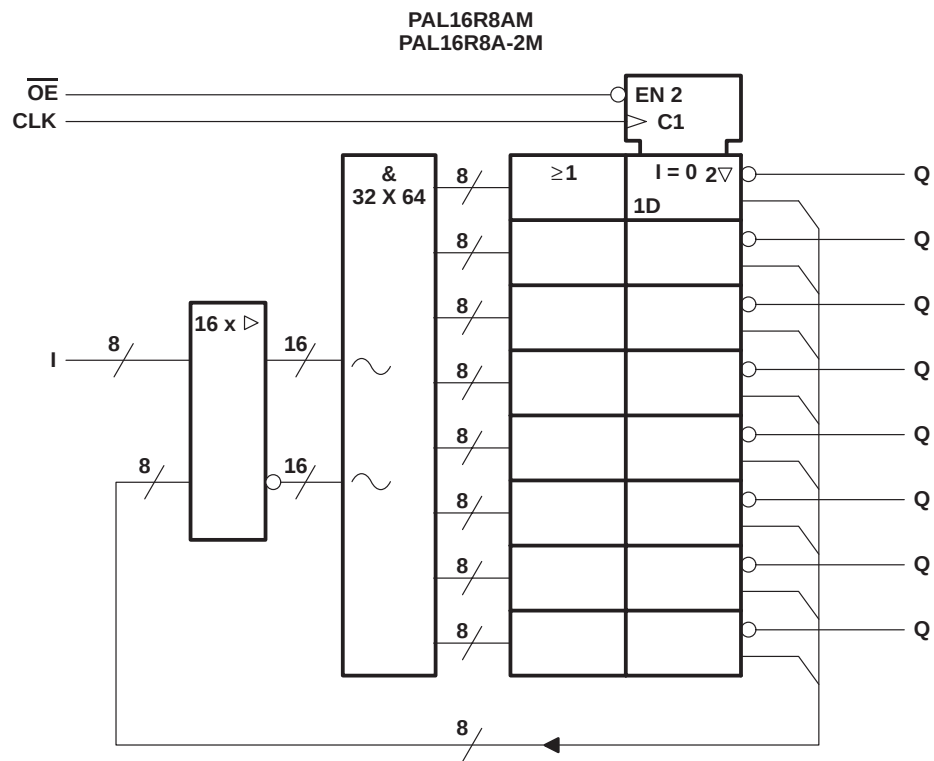
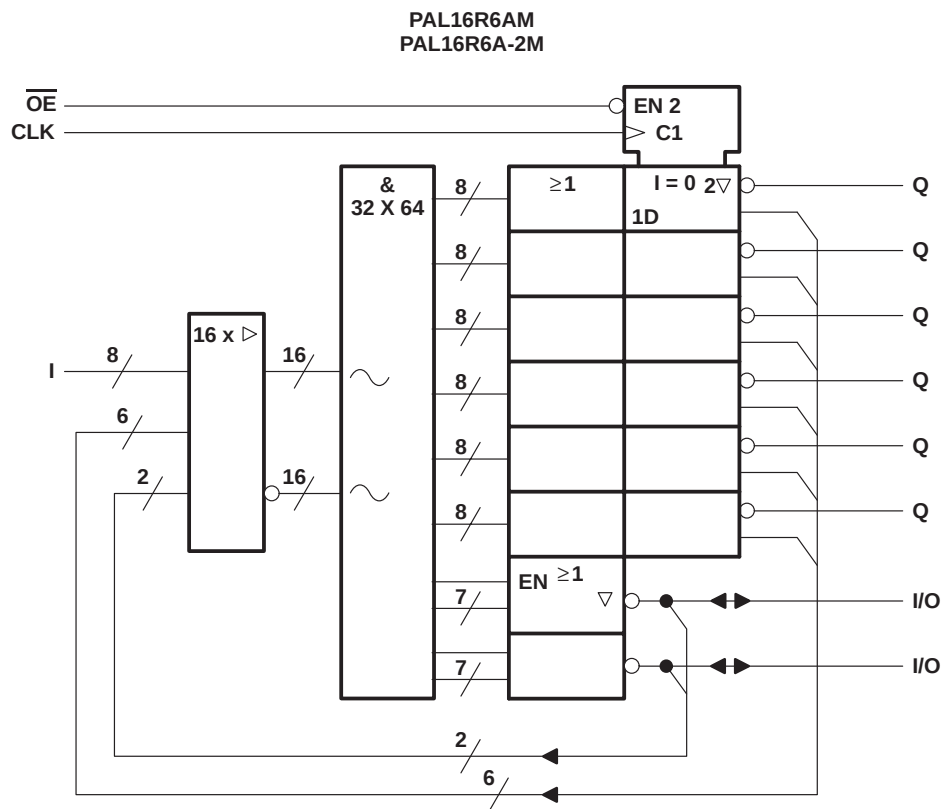
functional block diagrams (positive logic)



PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL[®] CIRCUITS

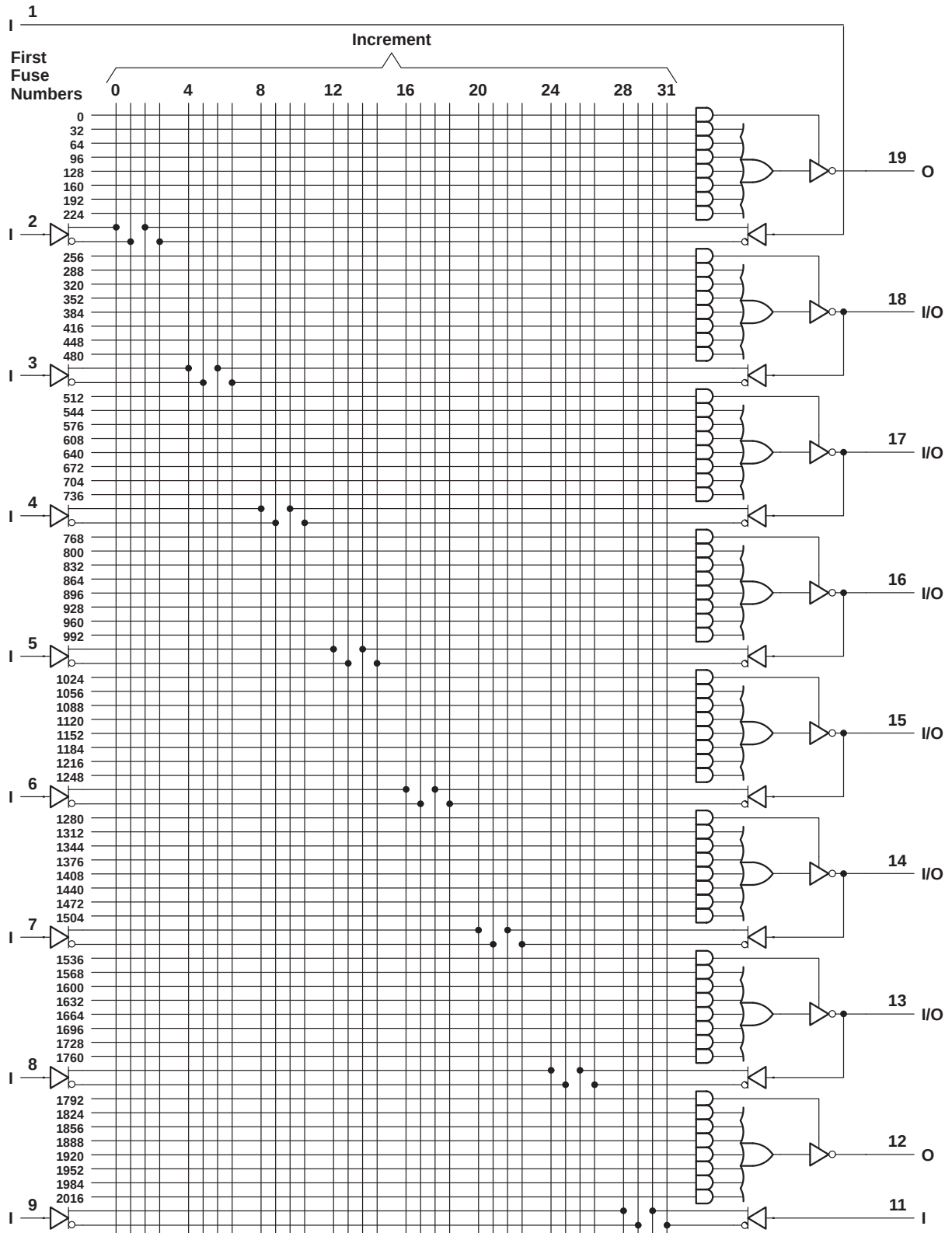
SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

functional block diagrams (positive logic)



~ denotes fused inputs

logic diagram (positive logic)

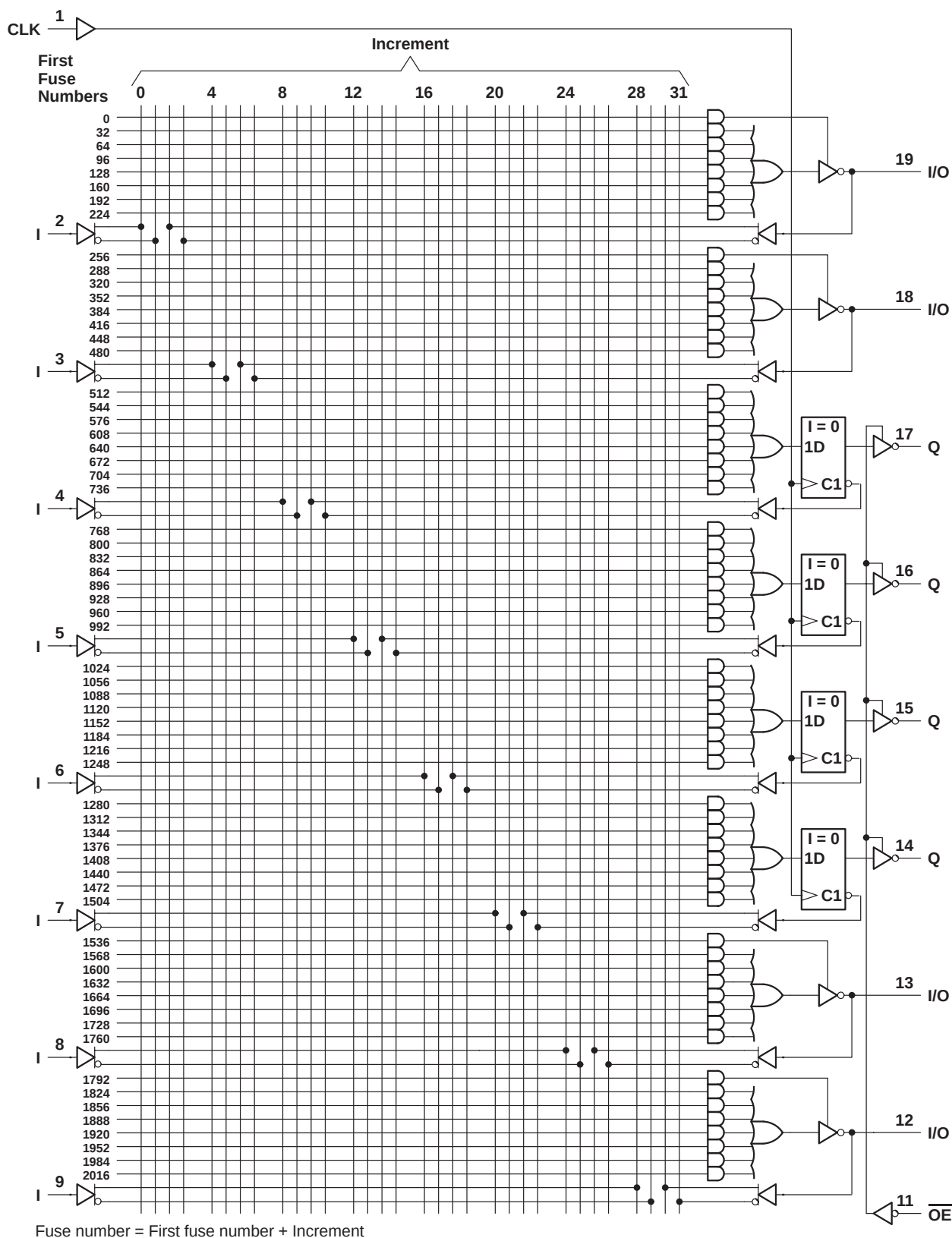


Fuse number = First fuse number + Increment

PAL16R4AM, PAL16R4A-2M STANDARD HIGH-SPEED PAL® CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

logic diagram (positive logic)



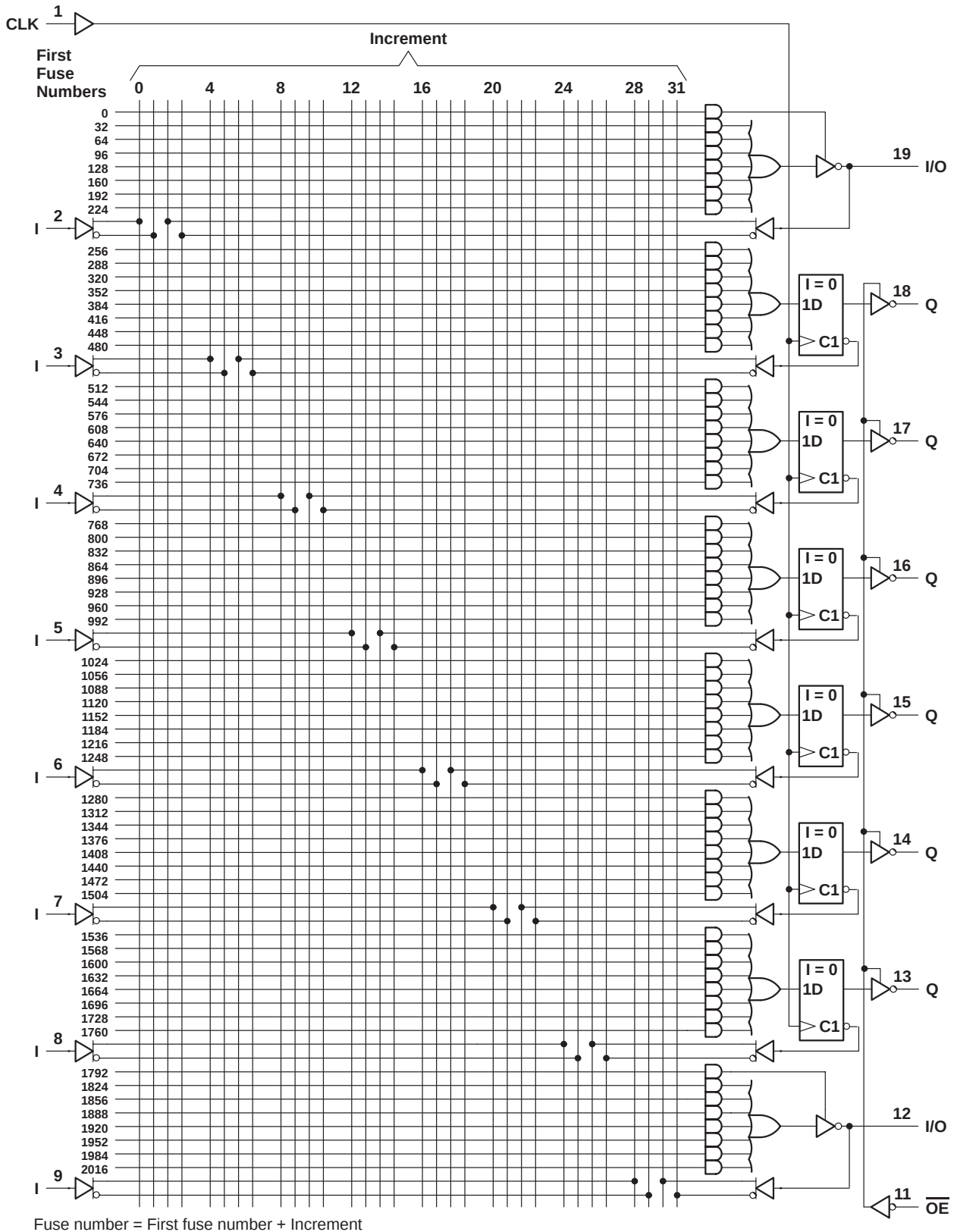
TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PAL16R6AM, PAL16R6A-2M STANDARD HIGH-SPEED PAL® CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

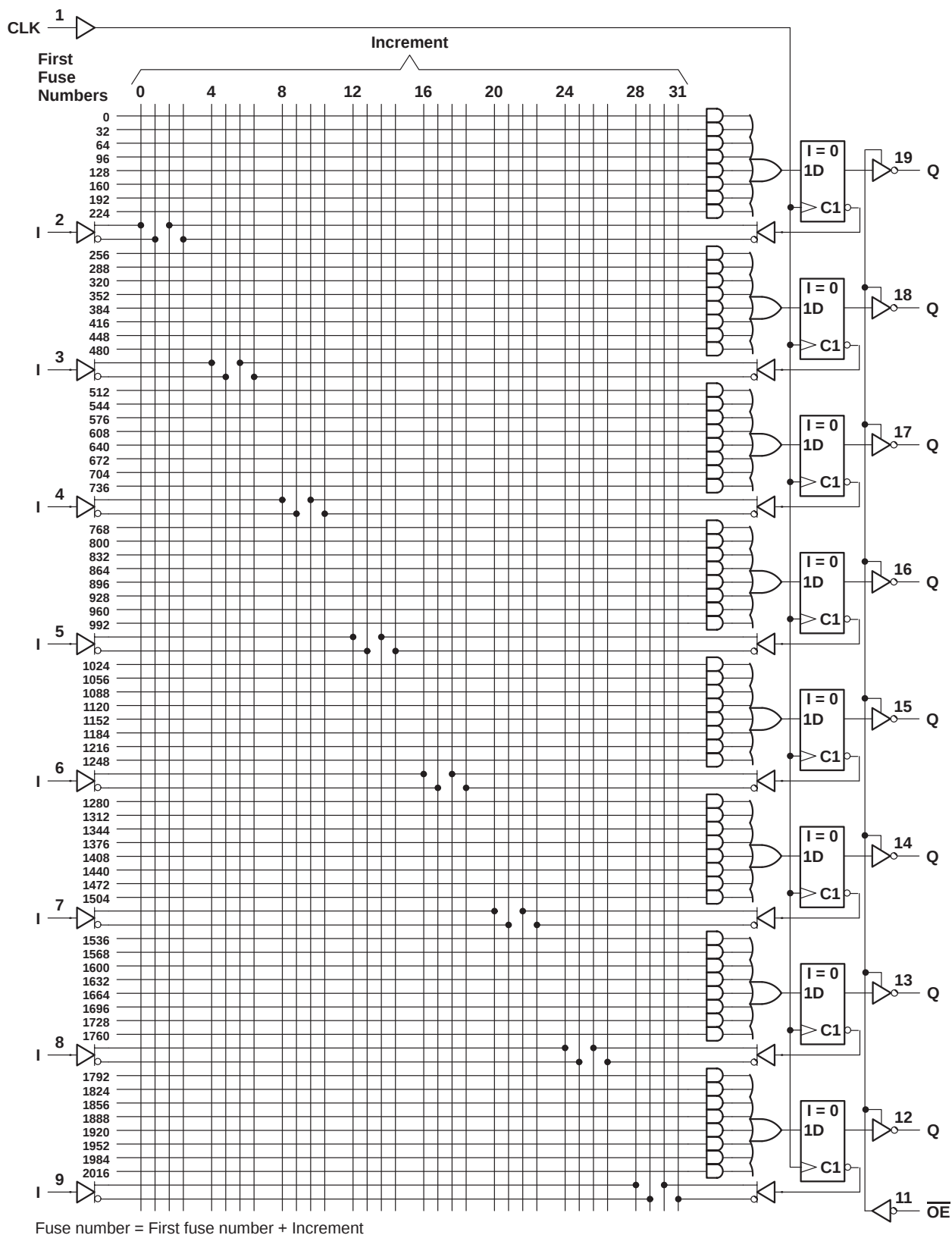
logic diagram (positive logic)



PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED PAL[®] CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

logic diagram (positive logic)



programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–55	25	125	°C

PAL16L8AM, PAL16R4AM, PAL16R6AM, PAL16R8AM STANDARD HIGH-SPEED PAL[®] CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.5	V
V_{OH}		$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	2.4	3.2		V
V_{OL}		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 12\text{ mA}$		0.25	0.4	V
I_{OZH}	Outputs	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			20	μA
	I/O ports					100	
I_{OZL}	Outputs	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
	I/O ports					-100	
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			0.2	mA
I_{IH}	I/O Ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			100	μA
	All others					25	
I_{IL}	$\overline{\text{OE}}$ input	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.2	mA
	All others					-0.1	
$I_{OS}^{\ddagger}$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$	-30		-250	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$V_I = 0$, Outputs open		75	180	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	25	MHz
t_w	Pulse duration (see Note 2)	Clock high	15		ns
		Clock low	20		
t_{su}	Setup time, input or feedback before $\text{CLK}\uparrow$		25		ns
t_h	Hold time, input or feedback after $\text{CLK}\uparrow$		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP [†]	MAX	UNIT
f_{max}			R1 = 390 Ω , R2 = 750 Ω , See Figure 1	25	45		MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	$\text{CLK}\uparrow$	Q			10	20	ns
t_{en}	$\overline{\text{OE}}\downarrow$	Q			15	25	ns
t_{dis}	$\overline{\text{OE}}\uparrow$	Q			10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

PAL16L8A-2M, PAL16R4A-2M, PAL16R6A-2M, PAL16R8A-2M STANDARD HIGH-SPEED PAL® CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.5	V
V_{OH}		$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	2.4	3.2		V
V_{OL}		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 12\text{ mA}$		0.25	0.4	V
I_{OZH}	Outputs	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			20	μA
	I/O ports					100	
I_{OZL}	Outputs	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
	I/O ports					-100	
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			0.2	mA
I_{IH}	I/O Ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			100	μA
	All others					25	
I_{IL}	$\overline{\text{OE}}$ input	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.2	mA
	All others					-0.1	
$I_{OS}^\ddagger$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$	-30		-250	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$V_I = 0$, Outputs open		75	90	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	16	MHz
t_w	Pulse duration (see Note 2)	Clock high	25		ns
		Clock low	25		
t_{su}	Setup time, input or feedback before $\text{CLK}\uparrow$		35		ns
t_h	Hold time, input or feedback after $\text{CLK}\uparrow$		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

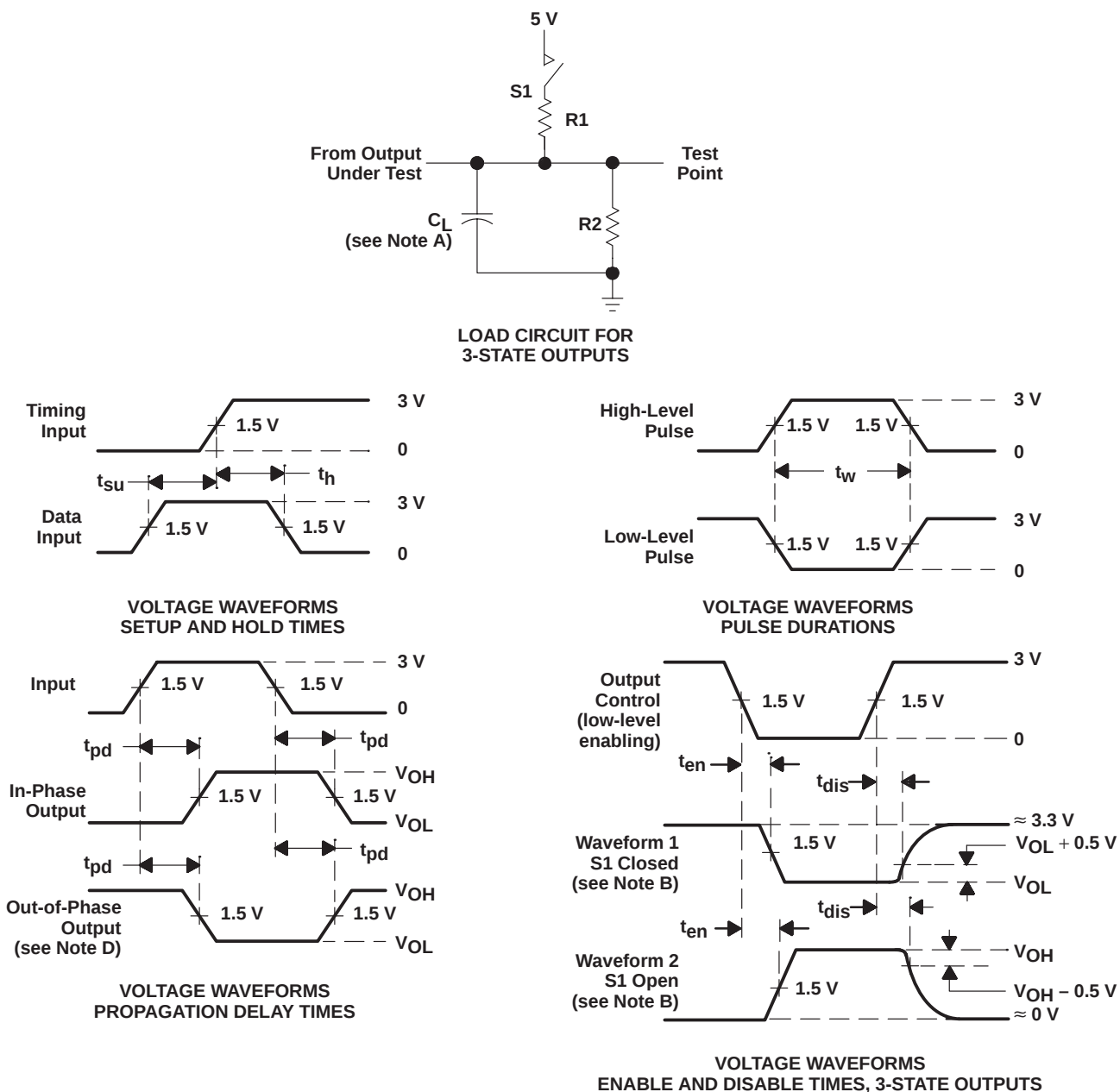
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP [†]	MAX	UNIT
f_{max}			R1 = 390 Ω , R2 = 750 Ω , See Figure 1	16	25		MHz
t_{pd}	I, I/O	O, I/O			25	40	ns
t_{pd}	$\text{CLK}\uparrow$	Q			11	25	ns
t_{en}	$\overline{\text{OE}}\downarrow$	Q			20	25	ns
t_{dis}	$\overline{\text{OE}}\uparrow$	Q			11	25	ns
t_{en}	I, I/O	O, I/O			25	40	ns
t_{dis}	I, I/O	O, I/O			25	35	ns

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 10$ MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
81036072A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103607RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103607SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036082A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103608RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103608SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036092A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103609RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103609SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036102A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103610RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103610SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036112A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103611RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103611SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036122A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103612RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103612SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036132A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103613RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103613SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
81036142A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8103614RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8103614SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8A-2MFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8A-2MJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8A-2MJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8A-2MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8AMFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8AMJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8AMJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16L8AMWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4A-2MFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4A-2MJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4A-2MJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4A-2MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4AMFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4AMJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4AMJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R4AMWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6A-2MFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6A-2MJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PAL16R6A-2MJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6A-2MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6AMFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6AMJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6AMJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R6AMWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8A-2MFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8A-2MJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8A-2MJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8A-2MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8AMFKB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8AMJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8AMJB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
PAL16R8AMWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

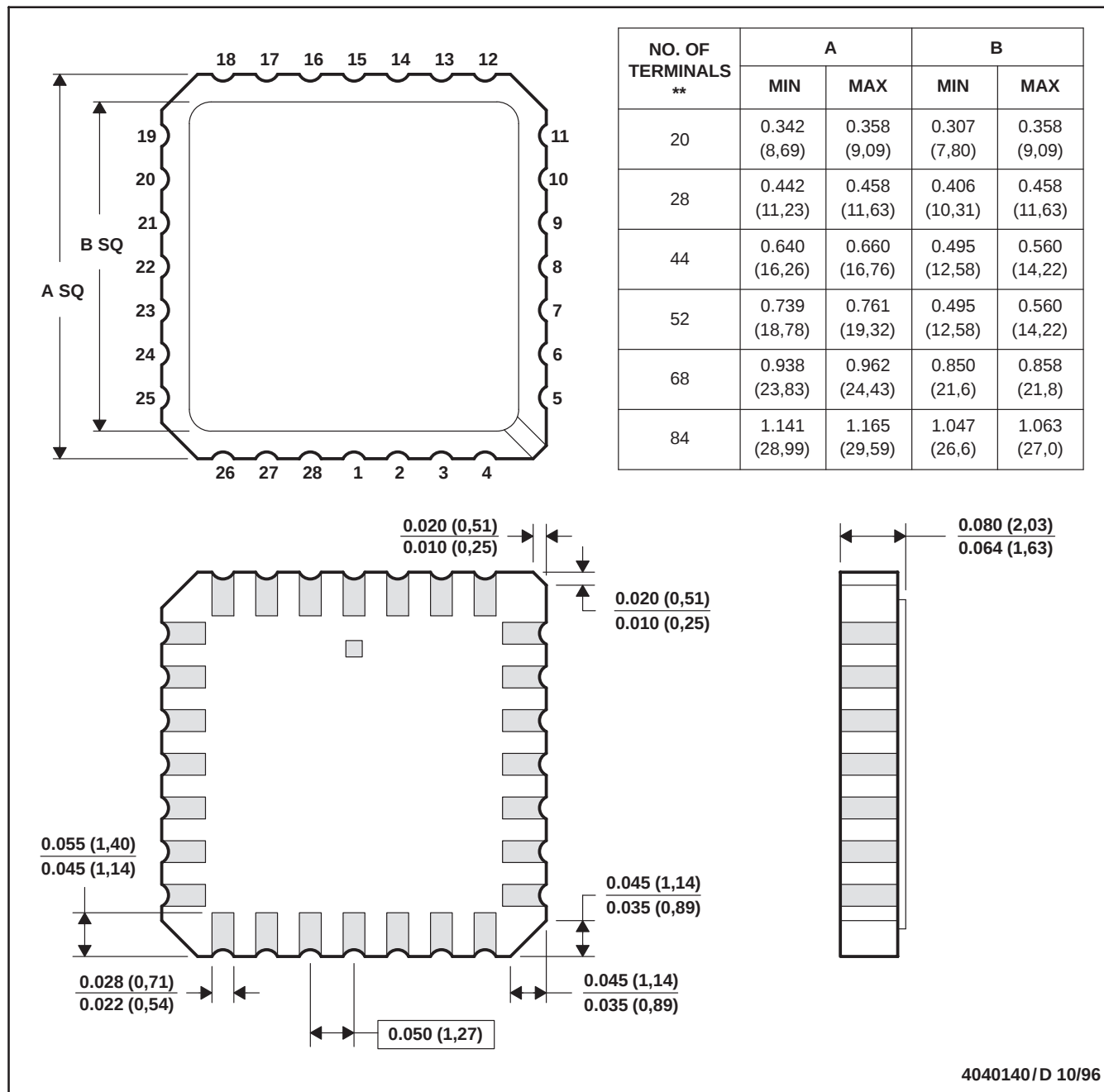


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated