

Description

This IC allows the user to select the current hysteresis level required

with a minimum of 10% of full load. A differential current sense amplifier (CSA) permits accurate inductor current measurements. The error amplifier (EA) has its non-inverting input connected to the ICs internal reference voltage. Trimming of the bandgap reference is done at the inverting input of the Error Amplifier to achieve a $\pm 1\%$ tolerance. The output stage provides 1A peak current capability.

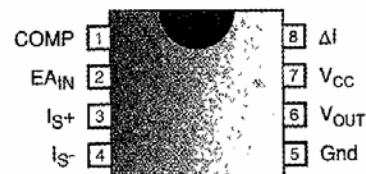
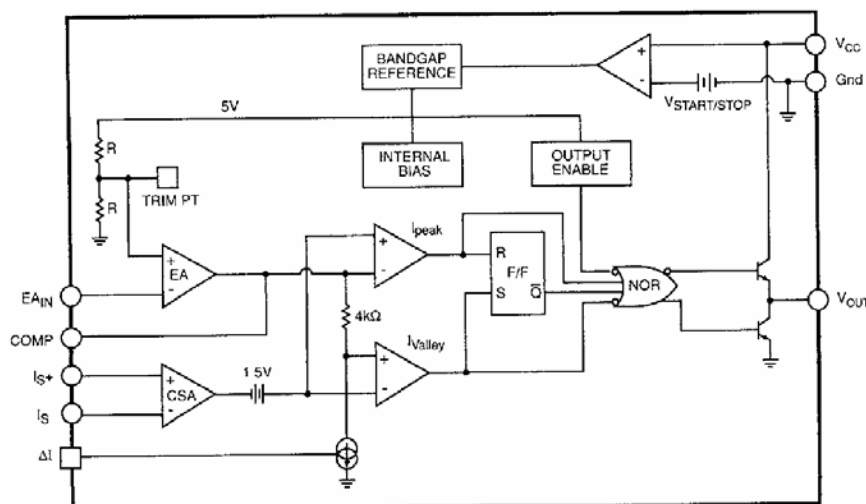
Supply voltage	20V
Output current	+1A (peak)
.....	+200mA (steady state)
Operating Temperature	
Industrial	-25° to +85°C
Commercial	0° to 70°C

Features

- ☐ Provides Hysteretic Current-Mode Control.
- ☐ Inherent Short Circuit Protection for the Power Supply.
- ☐ High Current Totem Pole Output.
- ☐ Eliminates Right-Half Plane Zero in Continuous Conduction Flyback and Boost Converter topologies.
- ☐ Feedforward Load Regulation

Package Options

8 Lead PDIP & SO



Electrical Characteristics: $-25 \leq T_A \leq 85^\circ\text{C}$ for the CS322/4 I, $0 \leq T_A \leq 70^\circ\text{C}$ for the CS322/4 C. $V_{CC}=20\text{V}$,
Voltage on ΔI pin = 0.5V, Unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
■ Output Section					
Output Low Level	$I_{SINK}=20\text{mA}$		0.25	0.40	V
	$I_{SINK}=200\text{mA}$		1.5	2.2	V
Output High Level	$I_{SINK}=20\text{mA}$	18.0	18.5		V
	$I_{SINK}=200\text{mA}$	17.5	18.0		V
Rise Time	$T_J=25^\circ\text{C}$, $C=1\text{nF}$ (Note 1)		30	60	ns
Fall Time	$T_J=25^\circ\text{C}$, $C=1\text{nF}$ (Note 1)		30	60	ns
Output Resistance	$7\text{V} < V_{CC} < V_{ULVO}$ (Stop Threshold)		50	65	k Ω
■ Undervoltage Lockout Section					
Start-Up Current			0.8	1.5	mA
Operating Supply Current			14	20	mA
Start Threshold					
CS-322		13.5	14.5	15.5	V
CS-324		8.5	9.0	9.5	V
Stop Threshold					
CS-322		9.5	10.5	11.5	V
CS-324		7.4	7.8	8.2	V
■ Error Amplifier Section					
Input Bias Current	$EA_{IN} = 2.5\text{V}$		-0.3	-1.0	μA
A_{VOL}	$1 < V_{COMP} < 3.5\text{V}$	65	90		dB
Unity Gain Bandwidth	(Note 1)	1	2		MHz
$V_{OUT HI}$		3.8	4.0		V
$V_{OUT LO}$			0.7	1.1	V
Reference Input Voltage	$COMP=EA_{IN}$	2.45	2.50	2.55	V
■ Current Sense Amplifier					
Gain	$V_{Sense+}=1.4\text{V}$, $V_{Sense-}=1\text{V}$	4.35	5.00	5.65	V/V
Maximum Differential Input Signal	$V_{Sense+} = V_{Sense-}=1\text{V}$		0.50		V
Internal Offset Voltage			1.5		V
PSRR			70		dB
Input Bias Current			-40	-65	μA
Com-Mode Voltage Range		-0.25		$V_{CC}-5.00$	V
CMRR			60		dB
■ Hysteresis Level					
Hysteresis Level	$V_{\Delta I}=0.25\text{V}$ (Note 2)		50		mV
Hysteresis Voltage					
Dynamic Range					
$V_{\Delta I HI}$			5		V
$V_{\Delta I LO}$			0		V

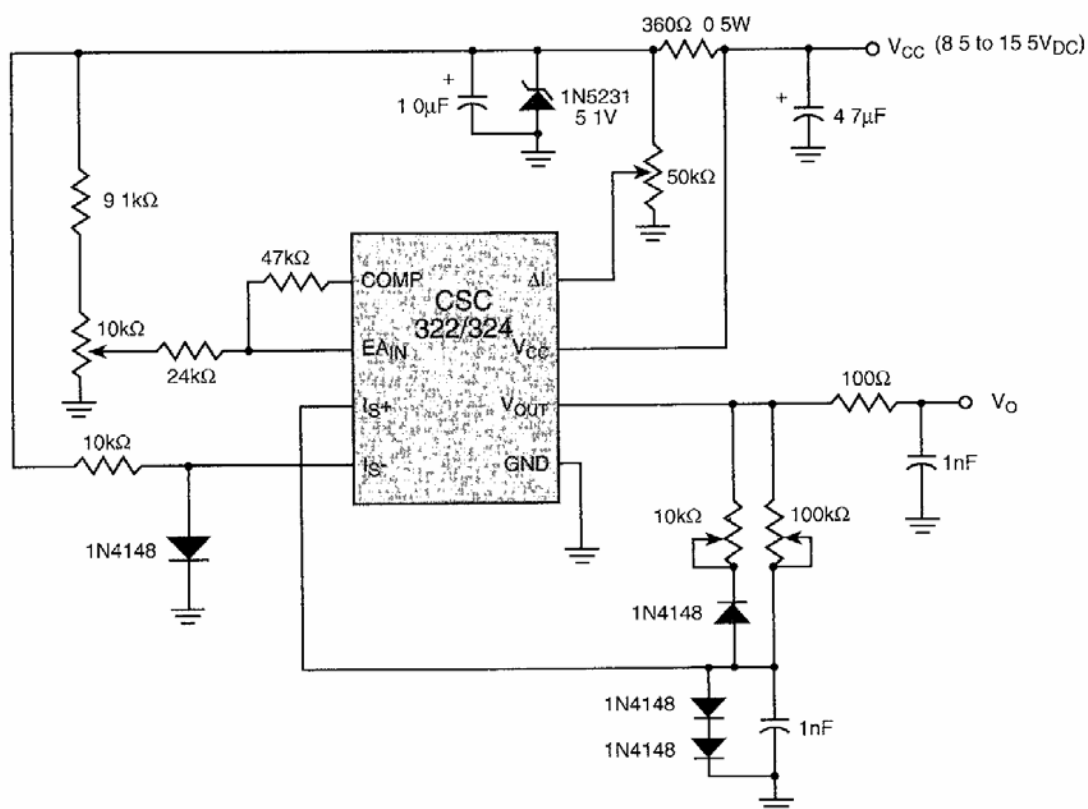
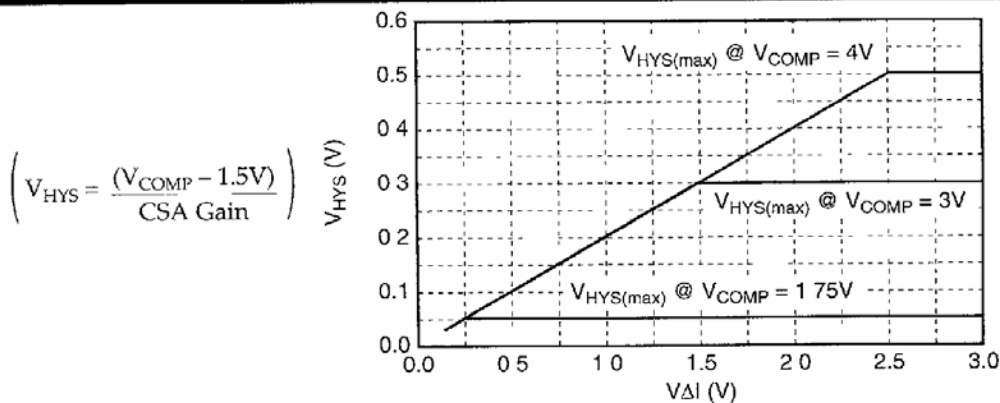
Note: 1. Although guaranteed, these parameters are not 100% tested in production.

2. $V_{\Delta Sense} = 0.2V_{\Delta I}$ measured across I_{S+} and I_{S-} .

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
8L PDIP & 8L SO		
1	COMP	Output of Error Amplifier.
2	EA _{IN}	Inverting input of Error Amplifier.
3	I _S ⁺	Non-inverting input of Current Sense Amplifier.
4	I _S ⁻	Inverting input of Current Sense Amplifier.
5	Gnd	Ground.
6	V _{OUT}	Output driver.
7	V _{CC}	Positive power supply input
8	ΔI	Input voltage that determines the width of the Hysteretic Band.

Test Circuit

 V_{HYS} vs $V_{\Delta I}$ 

Package Specification

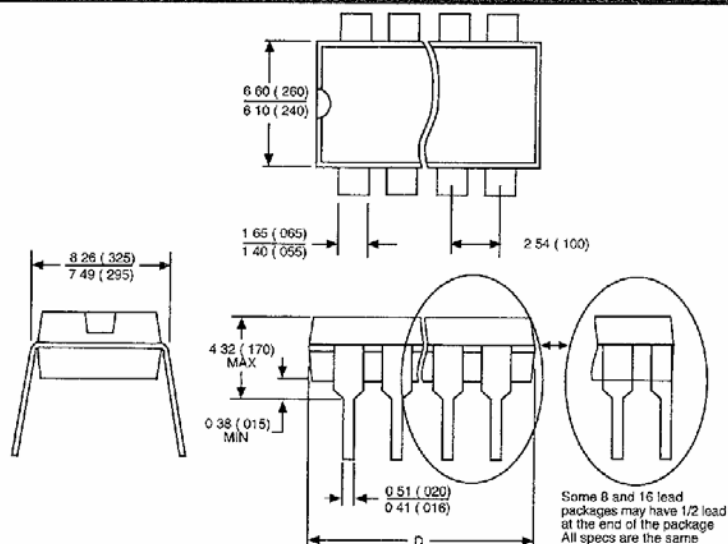
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L PDIP	9.40	9.14	.370	.360
8L SO	5.00	4.80	.197	.188

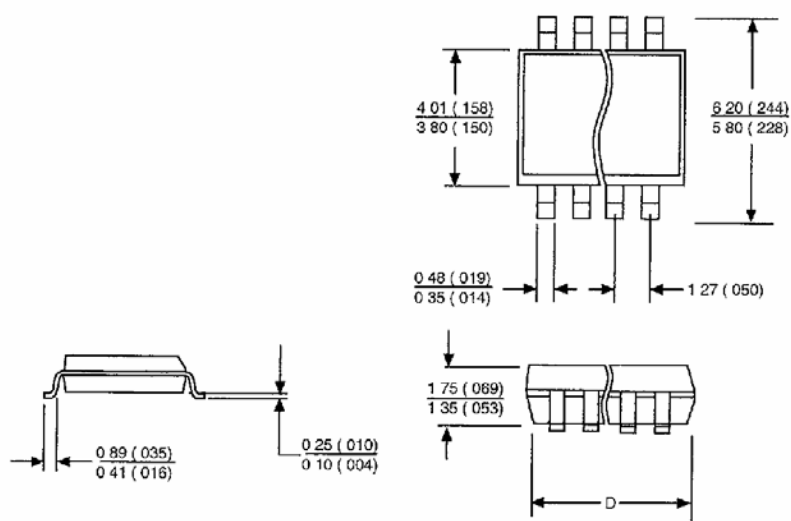
PACKAGE THERMAL DATA

Thermal Data		8 L PDIP	8L SO	
$R\theta_{JC}$	typ	52	45	$^{\circ}\text{C}/\text{W}$
$R\theta_{JA}$	typ	100	165	$^{\circ}\text{C}/\text{W}$

PDIP: 300 mil Wide



SO Narrow: 150 mil Wide



Ordering Information

Part Number	0°C to 70°C	-25°C to 85°C	Description
CS-322CN8	•		8L PDIP
CS-322CD8	•		8L SO
CS-324CN8	•		8L PDIP
CS-324CD8	•		8L SO
CS-322IN8		•	8L PDIP
CS-324IN8		•	8L PDIP