FMS9875

GBR YP_BP_R Graphics Digitizer

Triple 8-Bit, 108/140 MHz A/D Converter with Clamps and PLL

Features

- 108/140 Ms/s conversion rate
- RGB and YP_BP_R clamps
- 444 and 422 output timing
- Adjustable Gain and offset
- Internal Reference Voltage
- I^2C/SMBus compatible Serial Port
- 100-pin package

Applications

- YP_BP_R Digitizers
- Projectors
- TV sets

Description

As a fully integrated graphics interface, the FMS9875 can digitize RGB or YP_BP_R video signals at resolutions up to 1280 x 1024 with 75 Hz refresh rate. Compatible video formats include NTSC-601, PAL-601, SMPTE 293M, SMPTE 296M and SMPTE 274M.

The ADC sampling clock can be derived from either an external source or from incoming horizontal sync using the internal PLL. Setup and control is via registers accessible through an SMBus/I^2C compatible serial port.

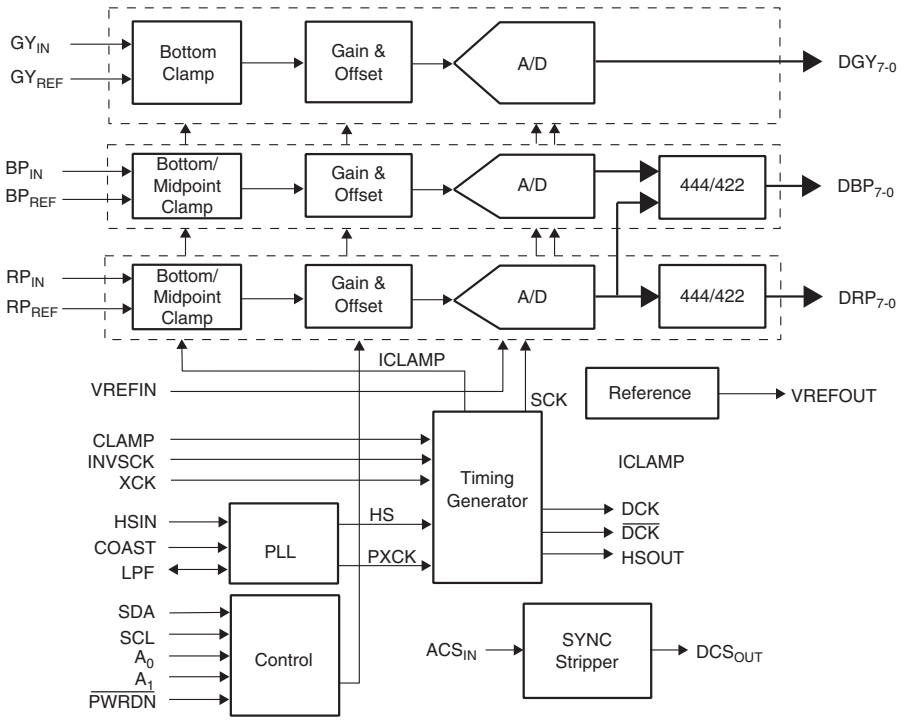
Input amplitude range is 500–1000mV with either DC or AC coupling. AC coupled inputs can be clamped to programmable midpoint/bottom levels or to external reference levels using either internal or externally generated clamp timing.

Common to the three channels are clamp pulses, a bandgap reference voltage and clocks derived from the HSYNC PLL or an external clock source. Digital data output levels are 2.5–3.3V CMOS compliant.

Power is derived from a single +3.3 Volt power supply. Package is a low cost 100-lead MQFP. Performance specifications are guaranteed over 0°C to 70°C.

Product Number	Speed
FMS9875KAC100	108 Ms/s
FMS9875KAC140	140 Ms/s

Block Diagram



Architectural Overview

Three separate digitizer channels are controlled by common timing signals derived from the Timing Generator. A/D clock signals can be derived from either a PLL or an external clock XCK. With the PLL selected, A/D clocks track the incoming horizontal sync signal connected to the HSIN input. Setup is controlled by registers that are accessible through the serial interface.

Conversion Channels

Typical RGB or YP_BP_R input signals, GYIN, BPIN, and RPIN are ground referenced with 700mV amplitude. If a sync signal is embedded then the usual format is sync on green or Y with the sync tip at ground, the black level elevated to 300mV and peak green at 1000mV. Either type of input can be accepted by using the clamp function with AC coupling.

Clamps

AC coupled input video signals must be level shifted to match the signal and A/D converter reference levels during the back porch (see Figure 1). Y/G inputs should be clamped to the A/D converter lower reference level. P_BP_R signals should be clamped to the A/D converter midrange level (nominally 350 mV), which is 50% of full scale (nominally 700 mV).

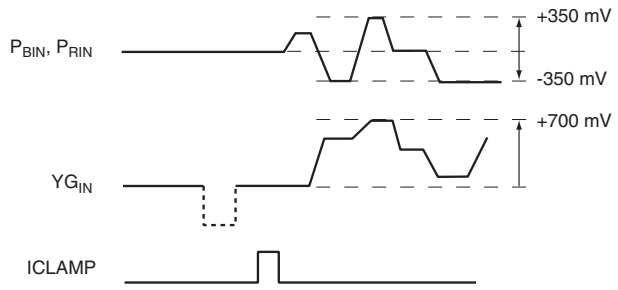


Figure 1. Clamping to the back-porch

Clamp pulses, ICLAMP, are derived from internal Timing and Control logic or from the external CLAMP input. Clamp timing is common to the three input channels.

With the A/D range set to 700mV ground referenced, clamp levels are:

- RGB: 000mV
- Y: 000mV
- P_BP_R: +350mV

Clamp levels can be set through the registers or through the YG_{REF}, BP_{REF} and RP_{REF} pins.

Gain and Offset

Gain and Offset registers serve two functions: 1) Adjustment of contrast and brightness by setting RGB values in tandems. 2) Matching the gain and offsets between channels, by setting RGB values individually to obtain the same output levels at zero and full-scale.

A/D conversion range can be matched to the amplitude of the incoming video signal by programming Gain Registers GGY, GBP and GRP, which vary sensitivity (LSB/volt) over a 2:1 range. Incoming video signal amplitudes varying from 0.5 to 1.0 volt can be accommodated.

Input offset voltage of each converter is programmable in 1 LSB steps through the 6-bit OSGY, OSBP and OSRP registers. Range of adjustment is equivalent to –31 to +32 LSB.

A/D Converter

Each A/D converter digitizes the analog input into 8-bit data words. Latency is $5–5^1/_2$ clock cycles, depending upon the state of the INVSCK pin.

V_{REFIN} is the source of reference voltage for the three A/D converters. V_{REFIN} can be connected to either the internal bandgap voltage, V_{REFOUT} or an external voltage.

Output Data Configuration

For RGB outputs, data format is unsigned binary: 00 corresponds to the lowest input; FF corresponds to the highest input.

For YP_BP_R outputs, the data format is:

- Y (0 to 700mV input): unsigned binary.
- P_BP_R (±350mV input): twos-complement or offset binary.

Output data format is:

- 24-bit YP_BP_R444
- 16-bit YP_BP_R422

With 422 sampling, P_BP_R samples are coincident with even samples of Y, beginning with 0.

HSOUT, L-to-H transition identifies the first sample.

Timing and Control

Timing and Control logic encompasses the Timing Generator, PLL and Serial Interface.

Timing Generator

All internal clock and synchronization signals are generated by the Timing Generator. Master Clock source is either the PLL or the external clock input, XCK. Register bit, XCKSEL selects the Master Clock source. Two clocks are generated.

Sampling clock, SCK is supplied to all three A/D converters. Phase of SCK (relative to HSIN) can be adjusted in 32 11.25 degree phase increments using the 5-bit PHASE register.

Output data clocks, DCK and $\overline{DCK}$ are provided for synchronizing data transfer from the digitizer outputs. DCK and $\overline{DCK}$ are slaved to SCK.

Incoming horizontal sync HS_{IN} is propagated by the Timing and Control to HS_{OUT} with a delay that aligns the leading edge with the output data.

Phase Locked Loop

With a horizontal sync signal connected to the HSIN input pin, the PLL generates a high frequency internal clock signal, PXCK that is fed to the Timing and Control logic. Frequency of PXCK is set by the register programmable PLL divide ratio, PLLN.

COAST is an input that disables the PLL lock to the horizontal sync input, HSIN. If HSIN is to be disregarded for a period such as the vertical sync interval, COAST allows the VCO frequency to be maintained. Missing horizontal sync pulses during the vertical interval can cause tearing at the top of a picture, if COAST is not used.

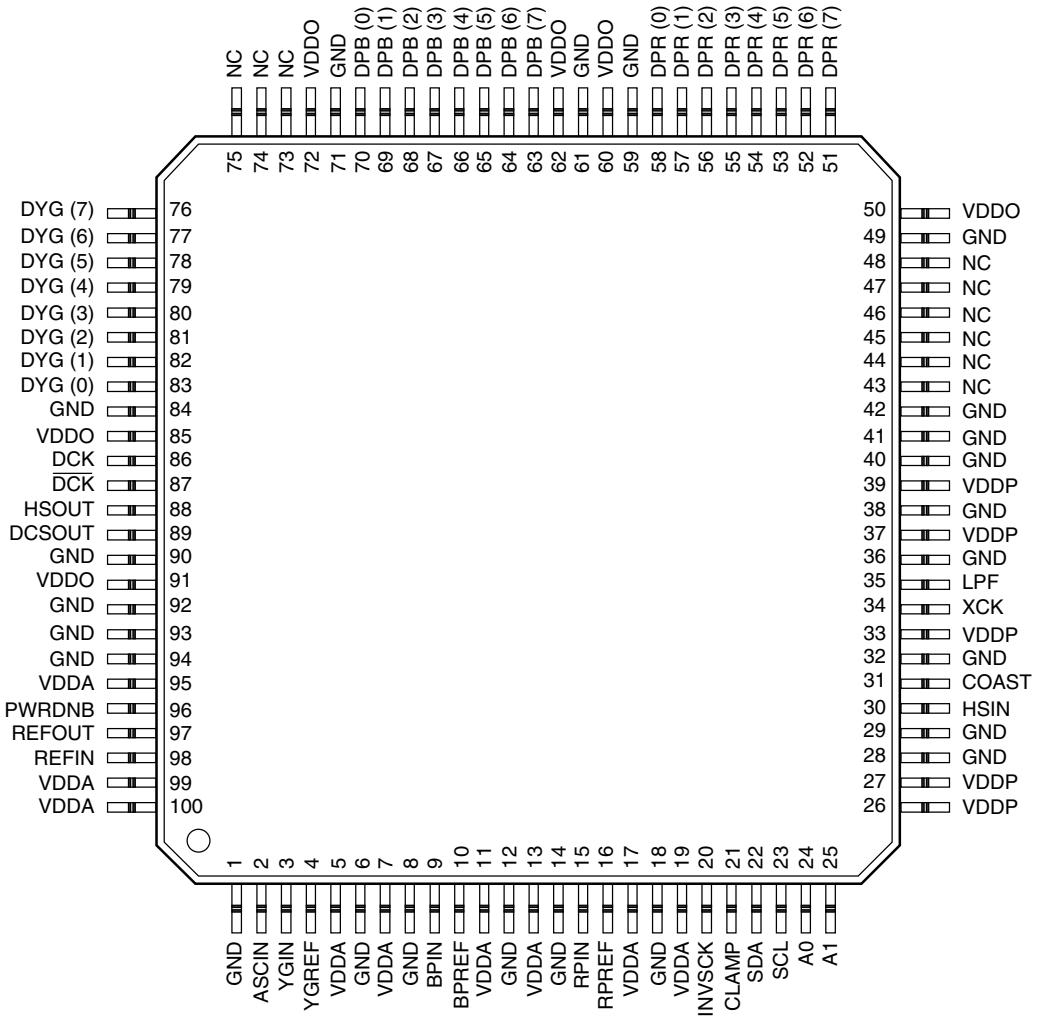
Two pixels per clock mode is set by programming the PLL to half the pixel rate. By toggling the INVCK pin between frames, even and odd pixels can be read on alternate frames.

Serial Interface

Registers are accessed through an I^2C/SMBus compatible serial port. Four serial addresses are pin selectable.

Pin Assignments

100-Lead MQFP (KG)



Pin Descriptions

Pin Name	Pin No.	Type/Value	Pin Function Description
Converter Channels			
YG_{IN}, BP_{IN}, RP_{IN}	3, 9, 15	Input	**Analog Inputs.** RGB or YP_BP_R.
YG_{REF}, BP_{REF}, RP_{REF}	4, 10, 16	Input	**Clamp Reference Inputs.** Voltage reference inputs for YG, BP and RP clamps.
DYG_{7-0}	76–83	Output	**Luminance/Green Channel Data Output.**
DPB_{7-0}	63–70	Output	**P_B/Blue Channel Data Output.**
DPR_{7-0}	51–58	Output	**P_R/Red Channel Data Output.**
Timing Generator			
CLAMP	21	Input	**External Clamp Input.**
INVSCK	20	Input	**Invert Sampling Clock.** Inverts SCK, the internal clock sampling the analog inputs. Supports Alternate Pixel Sampling mode for capture pixel rates up to 216Ms/s.
XCK	34	Input	**External Clock input.** Enabled if register bit, XCKSEL = H. Replaces PXCK clock generated by PLL. If unused, connect to ground through a 10kΩ resistor.
DCK	86	Output	**Output Data Clock.** Clock for strobing output data to external logic.
$\overline{DCK}$	87	Output	**Output Data Clock Inverted.** Inverted clock for strobing output data to external logic.
HSOUT	88	Output	**Horizontal Sync Output.** Reconstructed HSYNC delayed by FMS9875 latency with leading edge synchronized to start of data output. Polarity is always active HIGH.
Phase Locked Loop			
HSIN	30	Schmitt	**Horizontal Sync input.** Schmitt trigger threshold is 1.5V. A 5V source should be clamped at 3.3V or current limited, to prevent overdriving ESD protection diodes.
COAST	31	Input	**PLL COAST.** Extraneous or missing horizontal sync pulses can be ignored by asserting the COAST input. With COAST asserted, the HSIN signal is ignored by the PLL without affecting PXCK and the derived clocks: SCK, DCK and $\overline{DCK}$. With register bit, COASTPOL = 1: COAST = L: PLL locked to HSIN. COAST = H: PLL VCO input floats with HSIN disregarded COAST polarity may be inverted using the COASTPOL register bit.
LPF	35	Passive	**PLL Low Pass Filter.** Connect recommended PLL filter to LPF pin. (see *Schematic, PLL Filter*)
Sync Stripper			
ACS_{IN}	2		**Analog Composite Sync Input.** Input to sync stripper with 150mV threshold.
DCS_{OUT}	89		**Digital Composite Sync Output.** Output from sync stripper.
Control			
SDA	22	Bi-directional	**Serial Port Data.** Bi-directional data (I^2C/SMBUS).
SCL	23	Input	**Serial Port Clock.** Clock input (I^2C/SMBUS).
A_0	24	Input	**Address bit 0.** Lower bit of serial port address.
A_1	25	Input	**Address bit 1.** Upper bit of serial port address.
$\overline{PWRDN}$	96	Input	**Power Down/Output Control.** Powers down the FMS9875 with outputs high impedance.

Pin Descriptions

Pin Name	Pin No.	Pin Function Description
Power and Ground		
V_{DDA}	5, 7, 11, 13, 17, 19, 95, 99, 100	**ADC Supply Voltages.** Provide a quiet noise free voltage.
V_{DDP}	26, 27, 33, 37, 39	**PLL Supply Voltage.** Most sensitive supply voltage. Provide a very quiet noise free voltage.
V_{DDO}	50, 60, 62, 72, 85, 91	**Digital Output Supply Voltage.** Decouple judiciously to avoid propagation of switching noise.
GND	1, 6, 8, 12, 14, 18, 28, 29, 32, 36, 38, 40, 41, 42, 49, 59, 61, 71, 84, 90, 92, 93, 94	**Ground.** Returns for all power supplies. Connect ground pins to a solid ground-plane.
V_{REFIN}	98	**Voltage Reference Input.** Common reference input to RGB converters. Connect to VREFOUT, if internal reference is used.
V_{REFOUT}	97	**Voltage Reference Output.** Internal band-gap reference output. Tie to ground through a 0.1µF capacitor.

Addressable Memory

Register Map

Name	Address	Function	Default (hex)
$PLLN_{11-4}$	00	**PLL divide ratio, MSBs.** PLLN + 1 = total number of pixels per horizontal line.	69 (1693)
PLLCTRL	01	**PLL Control Register.** 1. Lower four bits of PLL divide ratio. 2. PLL Subdivide phase. 3. PLL Subdivide ratio.	D0 (1693)
GGY_{7-0}	02	**Gain, green/luminance channel.** Adjustable from 70 to 140%.	80
GBP_{7-0}	03	**Gain, blue/P_B channel.** Adjustable from 70 to 140%.	80
GRP_{7-0}	04	**Gain, red/P_R channel.** Adjustable from 70 to 140%.	80
$OSGY_{5-0}$	05	**Offset, green/luminance channel.** OSR_{5-0} is stored in the six upper register bits 7-2. Default value is decimal 32. $OSGY_{5-0}$ | X | X	80
$OSBP_{5-0}$	06	**Offset, blue/P_B channel.** OSR_{5-0} is stored in the six upper register bits 7-2. Default value is decimal 32. $OSBP_{5-0}$ | X | X	80
$OSRP_{5-0}$	07	**Offset, red/P_R channel.** OSR_{5-0} is stored in the six upper register bits 7-2. Default value is decimal 32. $OSRP_{5-0}$ | X | X	80
CD_{7-0}	08	**Clamp delay.** Delay in pixels from trailing edge of horizontal sync.	80
CW_{7-0}	09	**Clamp width.** Width of clamp pulse in pixels.	80
CONFIG 1	0A	**Configuration Register No. 1**	F4

Name	Address	Function	Default (hex)
$PHASE_{7-0}$	0B	**Sampling clock phase.** $PHASE_{4-0}$ stored in upper register bits 7-3. PHASE sets the sampling clock phase in 11.25° increments. Default value is decimal 16. $PHASE_{4-0}$ | X | X | X	80
PLLCTRL	0C	**PLL Control.**	24
CONFIG 2	0D	**Configuration Register No. 2.**	00
	0E	**Clamp Control Register.**	00
	0F	**Reserved.**	00

Register Definitions

PLL Control Register (01)

Bit no.	Name	Type	Description
1-0	$SUBDIV_{1-0}$	R/W	**PLL Subdivide ratio.** Selects the ratio of the divider following the PLL. **00:** divide-by 1 **01:** divide-by 2 **10:** divide-by 4 **11:** reserved X | X | X | X | X | X | $SUBDIV_{1-0}$
2	PLLFAZ	R/W	**PLL Sub-divider Phase.** Selects the phase of the divide-by-2 output. (Invalid for other outputs)
3	–	R/W	**Reserved.**
7-4	$PLLN_{3-0}$	R/W	**PLL divide ratio, LSBs.** PLLN + 1 = total number of pixels per horizontal line. $PLLN_{3-0}$ | X | X | X | X

Configuration Register 1 (0A)

Bit no.	Name	Type	Description
0			
1	XCKSEL	R/W	**External Clock Select.** Select internal clock source. **0:** Internal PLL **1:** XCK input.
2	XCLAMPOL	R/W	**External Clamp Polarity.** Select clamp polarity. **0:** Active L. **1:** Active H.
3	XCLAMP	R/W	**External Clamp Select.** Select clamp source. **0:** Internally generated by PLL referenced to HSIN. **1:** External CLAMP input.
4	COASTPOL	R/W	**Coast Polarity.** Select COAST input polarity. **0:** Active L. **1:** Active H.
5	HSPOL	R/W	**HSIN Polarity.** Select horizontal sync input polarity. PLL is locked to selected edge: **0:** Falling edge. **1:** Rising edge.
6	—	R	**1:**
7	—	R	**1:**

PLL Configuration Register (0C)

Bit no.	Name	Type	Description
1-0	—		
4-2	$IPUMP_{2-0}$	R/W	**Charge Pump Current.** Selects Charge Pump current (µA). **000:** 50 **001:** 100 **010:** 150 **011:** 250 **100:** 350 **101:** 500 **110:** 750 **111:** 1500
6-5	$FVCO_{1-0}$	R/W	**VCO Frequency Range.** Selects VCO frequency range (MHz). **00:** 10–40 **01:** 10–70 **10:** 20–120 **11:** 20–150
7	—	R/W	**Reserved.** **0:** Run. **1:** (reserved).

Configuration Register 2 (0D)

Bit no.	Name	Type	Description
0	—	—	**Reserved.** Set to 0.
3-1	REV	R	**Revision Number.** Die revision number.
4	OUTPHASE	R/W	**Output Data Phase.** In the alternate pixel mode, selects either odd (1, 3, 5, …) or even (2, 4, 6 ….) samples following the HSYNC leading edge to be emitted from output data ports. **0:** Even samples **1:** Odd samples
5	TWOS	R/W	**P_BP_R Data Output Format.** **0:** Offset binary. **1:** Two's complement.
6	PRFIRST	R/W	**P_BP_R Data Output Timing.** **0:** P_B data first, P_R data second. **1:** P_R data first, P_B data second.
7	422	R/W	**Output Data Format.** **0:** 444 **1:** 422 with P_BP_R multiplexed onto the DBP_{7-0} output.

Clamp Control Register (0E)

Bit no.	Name	Type	Description
1-0	—	—	**Reserved.** Set to 00.
3-2	RPLEVEL	R/W	**RP Clamp.** Clamps R or P_R input to selected level. **00:** Clamp to internal 0 V. **01:** Clamp to external voltage at RP_{REF} input. **10:** Clamp to internal mid-scale. **11:** Clamp to high impedance.
5-4	BPLEVEL	R/W	**BP Clamp.** Clamps B or P_B input to selected level. **00:** Clamp to internal 0 V. **01:** Clamp to external voltage at BP_{REF} input. **10:** Clamp to internal mid-scale. **11:** Clamp to high impedance.
7-6	GYLEVEL	R/W	**GY Clamp.** **00:** Clamp to internal 0 V. **01:** Clamp to external voltage at YG_{REF} input. **10:** Clamp to internal mid-scale. **11:** Clamp to high impedance.

Functional Description

There are two major sections within the FMS9875:

1. Analog-to-digital Converter Channels, one for each channel, GY, RP, BP and the voltage reference.
2. Timing and Control comprising the PLL, Timing Generator, Sync Stripper and Serial Interface.

A/D Converter Channels

Each of the RGB/YP_BP_R channels consists of:

1. A clamp to set the lower reference of each G/Y, B and R channel or the midpoint reference of the P_B and P_R channels.
2. Gain and offset stages to match the A/D converter range to input signal levels.
3. An Analog-to-Digital Converter to digitize the analog input.

A plot of output codes versus input voltage has a staircase-like shape. With FMS9875 Gain and Offset register values set to match a nominal 700 mV input, Tables 1 and 2 show the output codes in deciminal and binary, corresponding to the mid-point input voltages of each step.

Note:

1. The midpoint of code 000 lies 1/2 of one code-size below the 000/001 transition.
2. The midpoint of code 255 lies 1/2 of one code-size above the 254/255 transition.
3. For AC coupled inputs, during the blanking period:
   a) Y, G, B and R inputs should be clamped to the FMS9875 bottom reference.
   b) P_B and P_R inputs should be clamped to the FMS9875 mid-range level. (Half the range plus the offset voltage)

Table 1. YP_BP_R and GBR Decimal Output Coding

Input (mV)	Y, G, B, R	P_B, P_R	
		Offset Binary	Two's Complement
700	255	255	127
697.25	254	254	126
351.37	128	128	000
348.63	127	127	255
345.88	126	126	254
2.75	001	001	129
0	000	000	128

Table 2. YP_BP_R and GBR Binary Output Coding

Input (mV)		Y, G, B, R	P_B, P_R	
350 mV ref.	0 mV ref.		Offset Binary	Two's Complement
700	350	1111 1111	1111 1111	0111 1111
697.25	347.25	1111 1110	1111 1110	0111 1110
351.37	1.37	1000 0000	1000 0000	0000 0000
348.63	-1.37	0111 1111	0111 1111	1111 1111
345.88	-4.12	0111 1110	0111 1110	1111 1110
2.75	-347.25	0000 0001	0000 0001	1000 0001
0	-350	0000 0000	0000 0000	1000 0000

Analog Inputs

Input signal range is 500 to 1000mV to support conversion of single-ended signals with a typical amplitude of 700mV p-p. With the clamp active, each input can accommodate composite sync, a negative 300mV excursion.

Inputs are optimized for a source resistance of 37.5 to 75Ω. To reduce noise sensitivity, the 400MHz input bandwidth may be reduced by adding a small series inductor prior to the 75Ω terminating resistor. See Applications Section.

Clamps

If the incoming signals are not ground referenced, a clamp must be used to establish the incoming video range. Prior to each A/D converter, each channel includes a clamp that allows capacitively coupled input levels to be matched to the A/D converter reference level when the clamp pulse is active. Source of the clamp timing is determined by the XCLAMP register bit.

Clamping levels depend upon the incoming signal format:

1. **RGB**. All signals must be clamped to the A/D converter lower reference voltage, which is ground.
2. **YP_BP_R**. The Y signal must be clamped to ground. P_BP_R signals must be clamped to the mid-level of the A/D converter range, to establish the zero level of the signed P_BP_R signals.

With 700 mV incoming signal levels, nominal clamp levels are 0 mV for ground and 350 mV for mid-level. Offset and gain control can be used to trim input levels to match the clamp voltages.

Clamps levels can be derived from either of two sources:

1. Internal Voltages:
   a) Y and GBR signals are clamped to the A/D converter lower reference voltage that can be adjusted by the Offset register value.
   b) PBPR signals are clamped to the A/D mid-scale v oltage, which cannot be adjusted by the Offset control. Instead, the data output is forced to code 128 during the clamping period.

Clamp Control Register bits should be set as follows:

Table 3. Internal Clamp Setup

	GYLEVEL	BPLEVEL	RPLEVEL
GBR	00	00	00
YP_BP_R	00	10	10

2. External voltages levels connected to the GY_{REF}, BP_{REF} and RP_{REF} inputs. Nominal values are 0 mV for Y and 350 mV for P_B and P_R. Clamp Control Register bits should be set as follows:

Table 4. External Clamp Setup

	GYLEVEL	BPLEVEL	RPLEVEL
GBR	01	01	01
YP_BP_R			

External clamp levels should be established to match the incoming signals. For example, with 650 mV peak-to-peak P_BP_R signals, the mid-point should be set to 325 mV.

Internal clamp timing is generated by the Timing and Control Block. Position and width of the internal clamp pulse, ICLAMP are programmable through registers CD and CW. External clamp input is selected by register bit XCLAMP and the external clamp polarity selected through register bit XCLAMPOL. To disable the clamp for DC coupled inputs, set XCLAMP = 1 with either of these conditions:

1. XCLAMPOL = 0 with input CLAMP = H.
2. XCLAMPOL = 1 with input CLAMP = L.

Best performance will be achieved with the clamp set active for most of the black signal level interval between the trailing edge of horizontal sync and the start of active video. Insufficient clamping can cause brightness changes at the top of the image and slow recovery from large changes in Average Picture Level (APL). Recommended clamp delay value, CD is 0x10 to 0x20 for most standard video sources.

Analog-to-Digital Converter

Figure 2 is a block diagram of the ADC core with gain and offset functions. G_{7-0}, OS_{5-0}, V_{IN} and D_{7-0} generically refer to the gain and offset register values, analog input and parallel data output of any RGB channel.

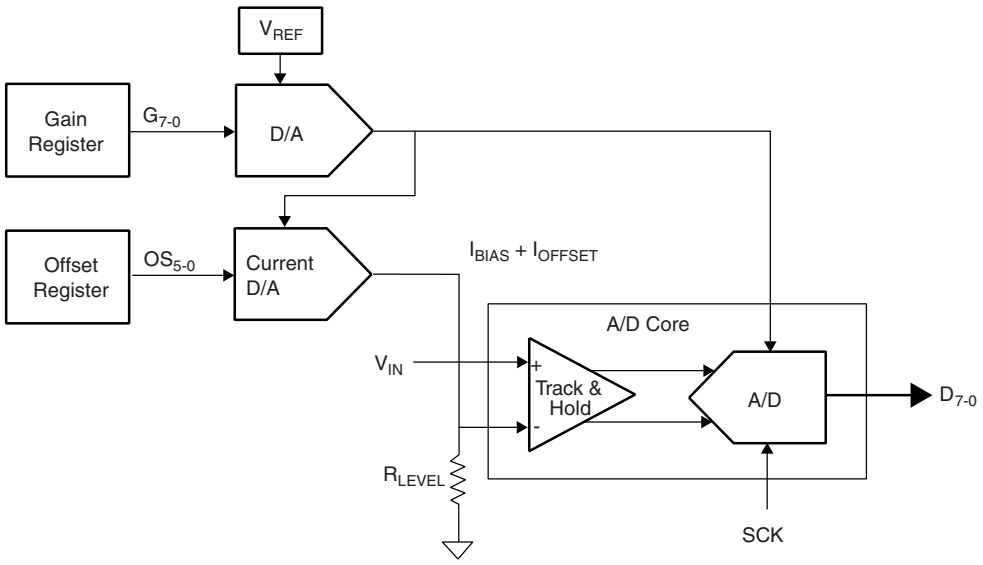


Figure 2. A/D Converter Architecture

Within the A/D converter core are the following elements:

1. Differential track and hold.
2. Differential analog-to-digital converter.

Setting the gain register value G_{7-0} (GRP_{7-0}, GGY_{7-0}, GBP_{7-0}), establishes the gain D/A converter voltage which is the upper A/D reference voltage. Increasing the gain register value reduces the output level. Conversion range is defined by the gain setting according to Table 5.

Table 5. Gain Calibration

G_{7-0}	Conversion Range (mV)
0	500
102	700
255	1000

A/D Converter sensitivity is:

$$S = \frac{255}{500} \bullet \frac{255}{255 + G_{7-0}} \text{LSB/mV}$$

Offset is set through the Track and Hold, which translates the ground referenced input to a differential voltage centered around A/D common mode bias voltage.

The 6-bit Offset D/A converter injects a current into R_{LEVEL} with two components:

1. I_{BIAS} to establish the A/D common mode voltage.
2. I_{OFFSET} to set the offset from the common mode level.

Voltage offset from the common mode voltage at the inverting input of the Track and Hold is:

$$V_{OS} = (OS_{5-0} - 31) \bullet \frac{255 + G_{7-0}}{255} \bullet \frac{500}{255}$$

D/A converter gain tracks A/D gain with 1 LSB of offset corresponding to 1LSB of gain. Increasing the offset of a video signal increases brightness of the picture. Data output from the A/D converter is:

$$D_{7-0} = S \bullet V_{IN} - (OS_{5-0} - 31)$$

Impact of the offset values $OSGY_{5-0}$, $OSBP_{5-0}$, and $OSRP_{5-0}$ is shown in Table 6.

Table 6. Offset Calibration

OS_{5-0}	Equivalent Offset (bits)
0	-31_d
31	0
63	32_d

Sampling Clock PHASE Adjustment

Bandwidth of TV video is typically well below the horizontal sampling rate. Consequently, PHASE has little impact on images sampled in the YP_BP_R format or RGB signals derived from a video source. By contrast, PC-generated image quality is strongly impacted by the $PHASE_{4-0}$ value. If PHASE is not set correctly, any section of an image consisting of vertical lines may exhibit tearing.

Figure 3 shows how an analog input, V_{IN} is sampled by the rising edge of SCK after a delay PHASE from the rising edge of either PXCK or XCK. SCK can be delayed up to 32 steps in 11.25° increments by adjusting the register value, $PHASE_{4-0}$.

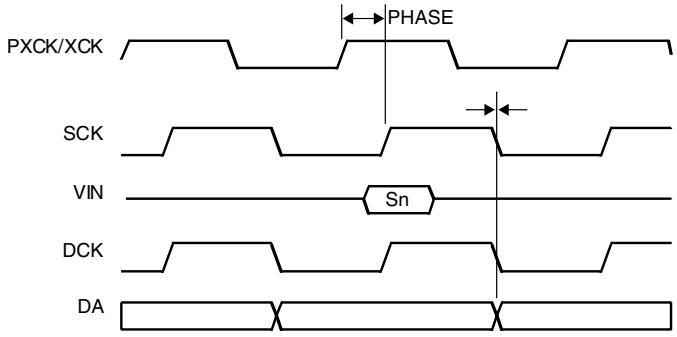


Figure 3. Internal Sampling Clock, SCK Timing

Output data and clocks: DCK and $\overline{DCK}$ are delayed in tandem with SCK relative to PXCK or XCK. There is a 5-5$^1/_2$ clock latency between the data sample S_n and the corresponding data out DA_{7-0}.

Ideally, incoming pixels (PC generated) would be trapezoidal with fast rise-times and the sampling edge of the A/D clock, SCK would be positioned along the level section of the incoming pixel waveform as shown in Figure 4. There is a narrow zone of uncertainly where sampling during pixel rise time would cause an error in the value of the A/D data output, D_{7-0}, which is shown as a value, 0-255.

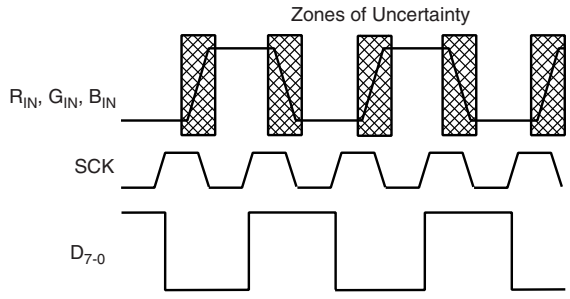


Figure 4. Ideal Pixel Sampling

In practice, high-resolution pixels have relatively long rise-times. As shown in Figure 5, there are narrow zones of serendipity when the pixel amplitude is level. Samples are valid in these zones.

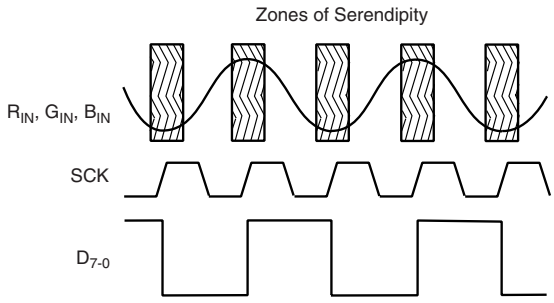


Figure 5. Acceptable Pixel Sampling

Referring to Figure 6, when the sample clock, SCK has some jitter, if the sampling edge occurs anywhere within the zone of uncertainty where the pixel rise time is steep, there will be amplitude modulation of the digitized data, D_{7-0}, due to the sampling clock jitter. To avoid corruption of the image, setting the value $PHASE_{7-0}$ is critical. $PHASE_{4-0}$ should be trimmed to position the sampling edge of SCK within the zone of serendipity.

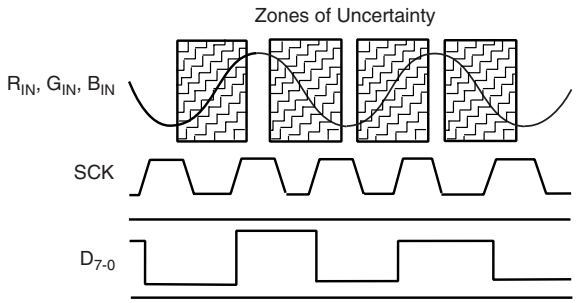


Figure 6. Improper Pixel Sampling

Voltage References

An on-chip voltage reference is generated from a bandgap source. V_{REFOUT} is the buffered output of this source that can be connected to V_{REFIN} to supply a voltage reference that is common to the three converter channels.

V_{REFIN}, with a nominal voltage of 1.25V, is the source of the differential reference voltages for each A/D converter. Reference voltages supplied to the differential inputs of the comparators in the A/D converters are derived from V_{REFIN}.

Digital Data Outputs

Input horizontal sync HSIN and outgoing data, D[7..0] are resynchronized to the internal delayed sample clock, SCK. Output timing relationships are defined in Figure 7. Latency of the first pixel, N varies according to the mode:

1. Normal.
2. Alternate pixel sampling.

Data transitions on the falling edge of the $\overline{DCK}$ clock. Pixel data should be sampled on the rising edge of the DCK clock.

Levels are 3.3 volt CMOS. $\overline{PWRDN}$ = L sets the outputs high-impedance. $\overline{PWRDN}$ = H enables the outputs.

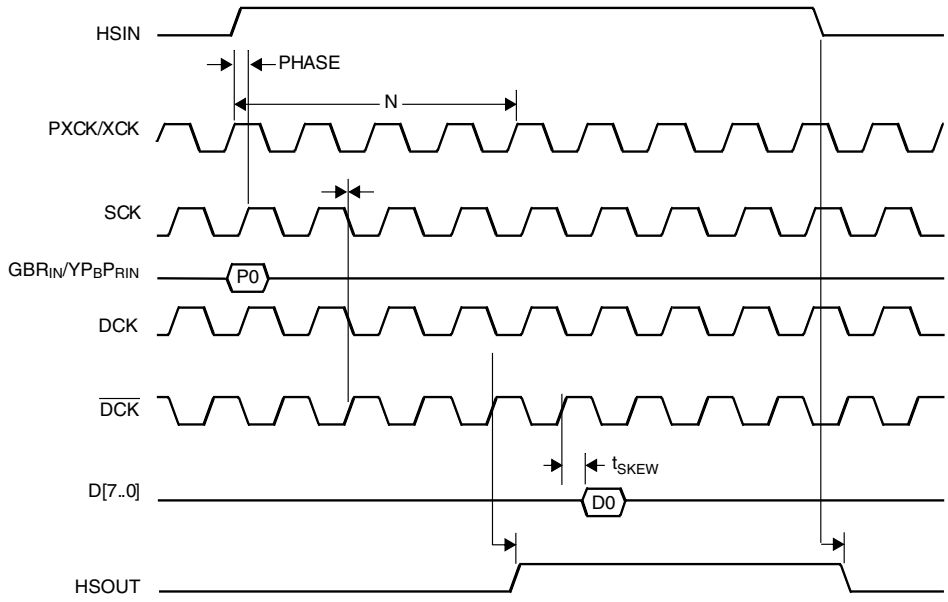


Figure 7. Output Timing

Figures 8 through 12 depict data output timing relative to the sampling clock and inputs for all modes. Timing is referenced to the leading edge of HSIN when the first sample is taken at the rising edge of SCK. Register bit OUTPHASE, determines if odd or even samples are directed to the data ports.

Note the timing of the HSOUT waveform:

1. HSOUT is always active HIGH.
2. Leading edge of HSOUT is aligned to the leading or trailing edge (selected by the HSPOL register bit) of HSIN delayed by 5 to 5.5 pixels
3. Leading edge is aligned with DCK.
4. Trailing edge is linked to HSIN.
5. If HSIN does not terminate before mid-line, HSOUT is forced low. A 50% duty cycle indicates that HSPOL is incorrectly set.

HS is the internal sync pulse generated from HSIN. SCK is the internal A/D converter sampling clock.

Pixel sampling is referenced to the rising edge of HSIN. Data outputs are delayed by 5 to 5.5 pixels. To allow for clamping, start-of-active-video (SAV) can begin any time after the falling edge of HSIN. End-of-active-video (EAV) follows SAV any time before the next HSIN pulse.

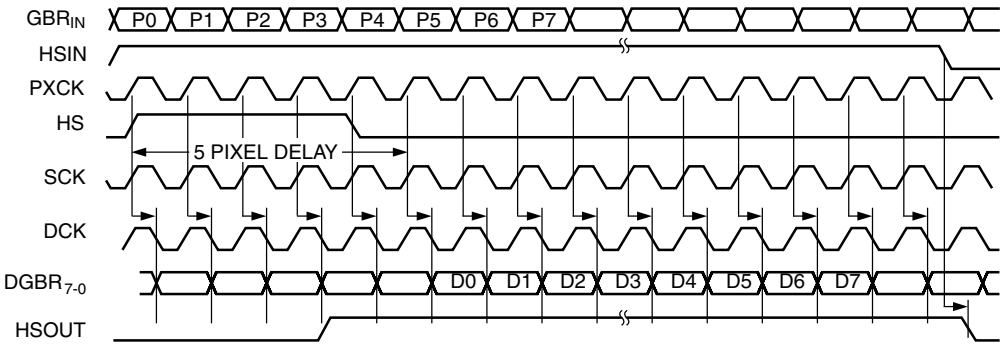


Figure 8. GBR Mode

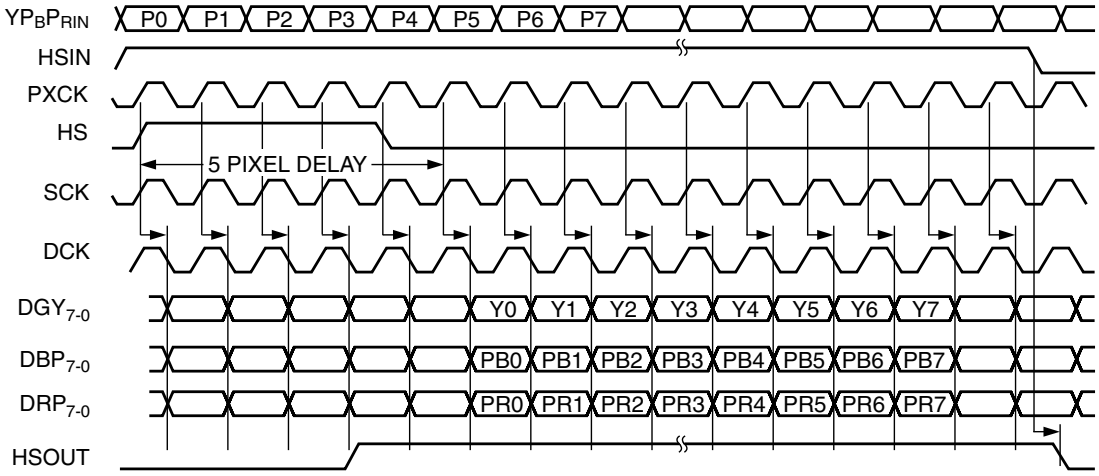


Figure 9. YP_BP_R444 Mode

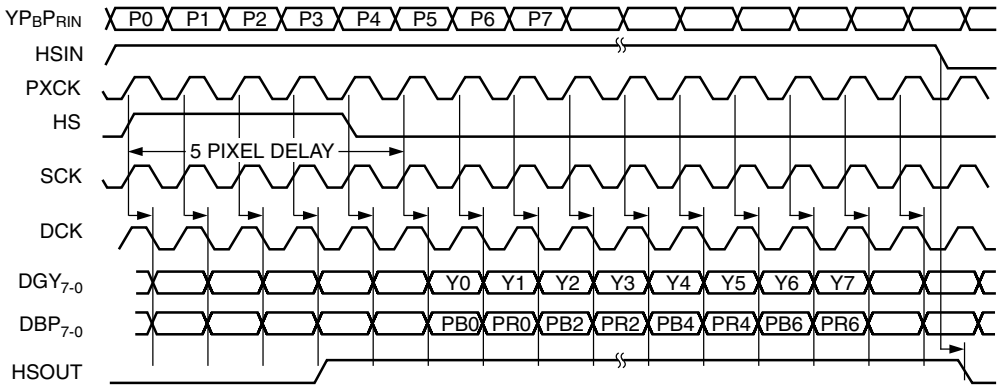


Figure 10. YP_BP_R422 Mode

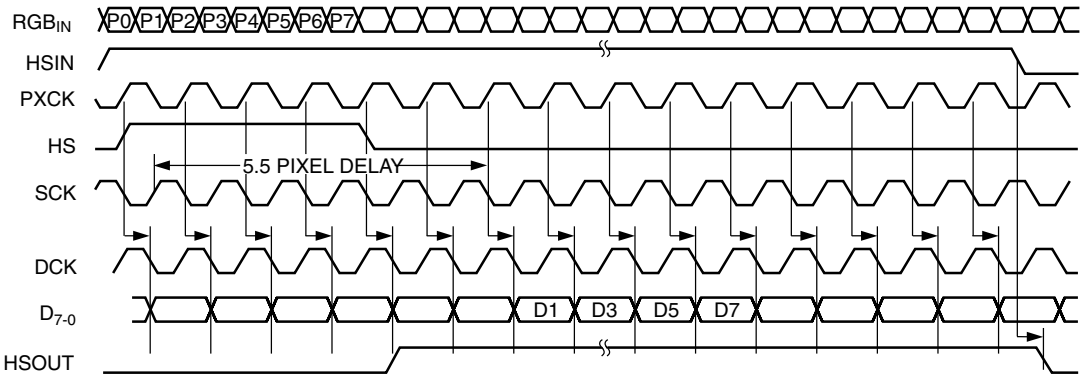


Figure 11. RGB Alternate Pixel Sampling Mode, (Even Pixels)

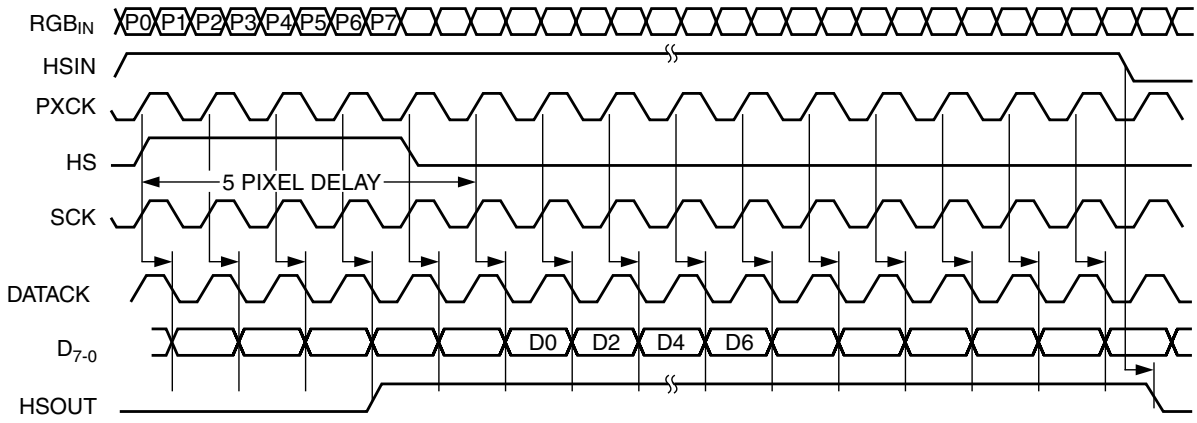


Figure 12. RGB Alternate Pixel Sampling Mode, (Odd Pixels)

Alternate Pixel Sampling Mode

A logic H on the INVSCK pin inverts the sampling phase of SCK. In the Alternate Pixel Sampling Mode:

1. The PLL is run at half rate. SCK, DCK and $\overline{DCK}$ are half rate.
2. CKINV is toggled between frames.

On one frame, along each line, even pixels are sampled. On the other, odd pixels are sampled.

Alternate Pixel Sampling is similar to interlacing used in broadcast video, except that the columns of pixels are interlaced instead of lines.

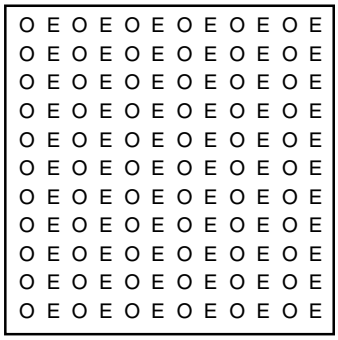


Figure 13. Odd and Even Pixels in a Frame

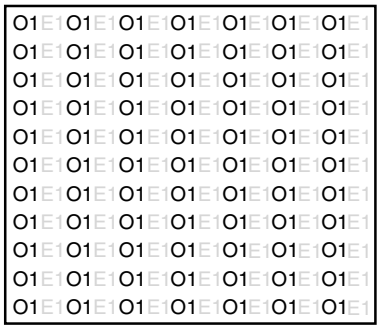


Figure 14. Odd Pixels from Frame 1

Figure 13. Even Pixels from Frame 2

Figure 14. Subsequent Output Combining Frames 2 and 3

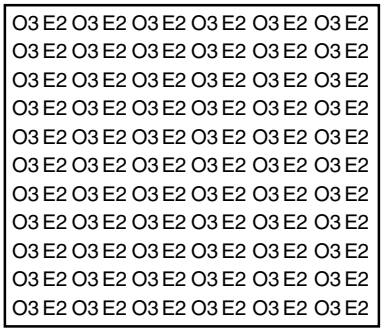
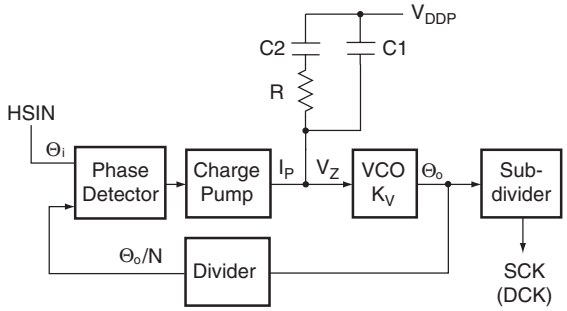


Figure 15. Combined Frames 2 and 3

Timing and Control

Timing and Control logic encompasses the PLL, Timing Generator and Sync Stripper.

Phase Locked Loop



Two clock types originate in the PLL:

1. Data clocks DCK and $\overline{DCK}$.
2. Internal sampling clock SCK.

DCK and $\overline{DCK}$ are used to strobe data from the FMS9875 to following digital circuits. SCK is the ADC sample clock which has adjustable phase controlled through the PHASE register. DCK and $\overline{DCK}$ are phase aligned with SCK.

Reference for the PLL is the horizontal sync input, HSIN with polarity selected by the HSPOL bit.

Frequency of the HS_{IN} input is multiplied by the value PLLN + 1 derived from the $PLLN_{11-4}$ and $PLLN_{3-0}$ registers. PLLN + 1 should equal the number of pixels per horizontal line including active and blanked sections. Typically blanking is 20–30% of active pixels. Divide ratios from 2–4095 are supported. SCK, DCK and $\overline{DCK}$ run at a rate PLLN + 1 times the HS_{IN} frequency.

The PLL consists of a phase comparator, charge pump VCO and ÷N counter, with the charge pump connected through the LPF pin to an external filter. These elements must be programmed to match the incoming video source to be captured.

Values of IPUMP and FVCO for common video standards timing are shown in Table 7. Timing of many computer video outputs does not comply with VESA recommendations. PLLN should be optimized to avoid vertical noise bars on the displayed image.

Modes marked 2X are 2X-oversampled modes where the number of samples per horizontal line is doubled. To select this mode, the Phase-locked Loop Divide Ratio value must changed from PLL_{1x} to:

$$PLL_{2x} = 2 \bullet (PLL_{1x} + 1) - 1$$

Table 7. Recommended IPUMP and FVCO values for Standard Display Formats

Standard	Test Rank	Resolution	Refresh Rate	Horizontal Frequency	Sample Rate	$FVCO_{1-0}$	$IPUMP_{2-0}$	$SUBDIV_{1-0}$
NTSC-601	C	720 x 483i (1X)	30 Hz	15.734 kHz	13.5 MHz	00	101	2
PAL-601	C	720 x 583i (1X)	25 Hz	15.625 kHz	13.5 MHz	00	101	
NTSC-601	C	720 x 483i (2X)	30 Hz	15.734 kHz	27 MHz	00	101	1
PAL-601	C	720 x 583i (2X)	25 Hz	15.625 kHz	27 MHz	00	101	
SMPTE 293M	C	720 x 483p	60 Hz	31.4685 kHz	27 MHz	00	111	2
SMPTE 296M	C	1280 x 720p	60 Hz	45.00 kHz	74.25 MHz	01	111	1
SMPTE 274M	C	1920 x 1080i	30 Hz	33.750 kHz	74.25 MHz	01	111	
VGA	C	640 X 480	60 Hz	31.5 kHz	25.175 MHz	01	110	2
	C		75 Hz	37.5 kHz	31.500 MHz	01	110	
	C		85 Hz	43.3 kHz	36.000 MHz	01	110	
SVGA	C	800 X 600	60 Hz	37.9 kHz	40.000 MHz	01	110	1
	C		75 Hz	46.9 kHz	49.500 MHz	01	110	
	CT		85 Hz	53.7 kHz	56.250 MHz	01	110	
XGA	C	1024 X 768	60 Hz	48.4 kHz	65.000 MHz	10	110	1
	C		75 Hz	60.0 kHz	78.750 MHz	10	110	
	C		85 Hz	68.3 kHz	94.500 MHz	11	110	
SXGA	C	1280 X 1024	60 Hz	64.0 kHz	108.000 MHz	11	110	1
	CT		72 Hz	78.1 kHz	135.000 MHz	11	111	
	CT		75 Hz	80.0 kHz	135.000 MHz	11	111	

Notes:

1. VESA Monitor Timing Standards and Guidelines, September 17, 1998 and others.
2. Frame refresh rate is twice the field refresh rate for interlace (i) formats and equal to the field rate for progressive (p) formats.
3. When $SUBDIV_{1-0}$ = 2, VCO runs at 2x sample rate.

Values of IPUMP and FVCO are set through the PLL Configuration Register (0x0C). Recommended external filter components are shown in Figure 16. RF quality ±10% ceramic capacitors with X7R dielectric are recommended.

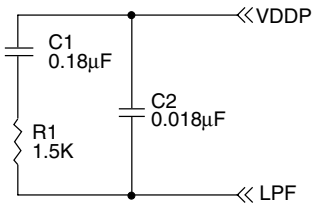


Figure 16. Schematic, PLL Filter.

Loop performance is established by setting:

1. VCO frequency range through $FVCO_{1-0}$. (see Table 8)
2. Charge Pump Current through $IPUMP_{2-0}$. (see Table 9)
3. External loop filter component values.

Table 8. VCO Frequency Bands

$FVCO_{2-0}$	Frequency Range (MHz)	KVCO (MHz/V)
00	10–40	35
01	10–70	60
10	20–120	80
11	20–150	95

Table 9. Charge Pump Current Levels

$IPUMP_{2-0}$	Current (µA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

Setting $PHASE_{4-0}$ selects the sampling phase of SCK relative to PXCK in 32 steps of 11.25°. Phase of the output data, DCK and $\overline{DCK}$ is slaved to the SCK phase.

RMS Clock jitter is less than 2% of pixel period in all operating modes.

At frequencies below 80 MHz, the percentage jitter begins to rise. Increased jitter at low frequencies can be counteracted in either of two ways:

1. Use 2X over-sampling. For example with NTSC-601, the 1X sample rate should be 13.5 MHz. If the divide ratio is increased from 858 (PLLN = 857) to 1716 (PLLN = 1715), the sampling rate is 27 MHz.
2. Use 1X sampling by doubling the VCO frequency, then dividing the PLL frequency by two. For example, with NTSC-601, the divide ratio is doubled to 1716 (PLLN = 1715), then the sub-divide ratio is set to two ($SUBDIV_{1-0}$ = 01) to reduce the sampling rate from 27 MHz to 13.5 MHz with 858 pixels per line.

COAST

When COAST is active, PLL lock to HSIN is disabled, while the VCO frequency is retained. VCO frequency remains stable over several lines without updates from HSIN. COAST can be connected directly to the vertical sync signal or supplied by the graphics controller. If 1/2H pulses are present within HSIN, the COAST period must encompass all 1/2H pulses. COAST polarity may be inverted using the COASTPOL register bit. In the description below, the setting COASTPOL = H is used.

Operation of COAST is depicted in Figure 17. HSOUT polarity is always positive. When COAST = L, HSOUT tracks HSIN (shown with postive polarity in Figure 1):

1. HSOUT rising edge tracks HSIN delayed by a few pixels.
2. HSOUT falling edge tracks the trailing edge of HSIN with no delay.

When COAST = H, the PLL flywheels, disregarding the incoming HSIN references, while the HSOUT waveform depends upon the state of HSIN.

1. If HSIN = H:
   a.) HSOUT rising edge remains locked to the PLL.
   b.) HSOUT trailing edge falls after 50% of the HSOUT period has expired.
2. HSIN transitions:
   a.) HSOUT rising edge remains locked to the PLL.
   b.) HSOUT falling edge is terminated by the trailing edge of HSIN.
3. If HSIN = L, then HSOUT = L

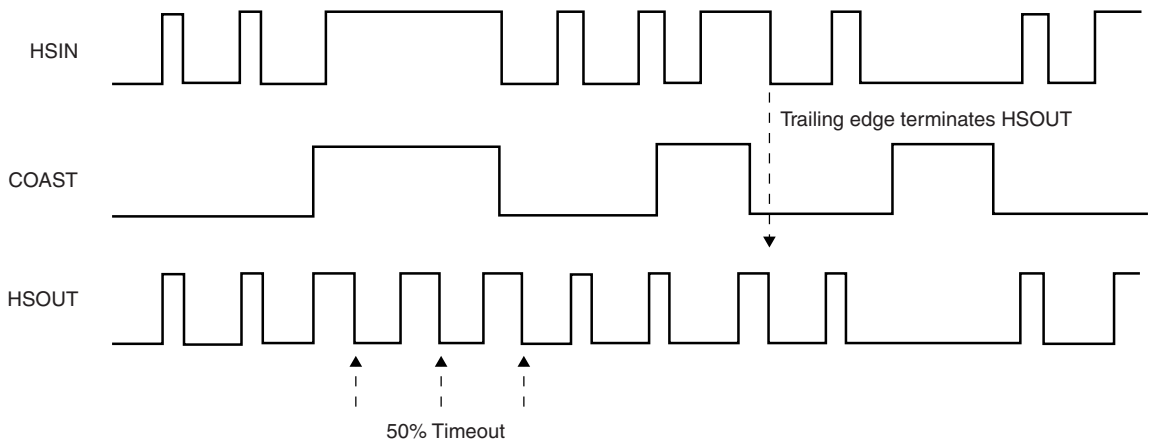


Figure 17.

Timing Generator

Timing and Control logic generates:

1. Internal sampling clock, SCK.
2. Output data clocks, DCK and $\overline{DCK}$.
3. Output horizontal sync, HS_{OUT}.
4. Internal clamp pulse, ICLAMP.

With HSPOL set correctly, ICLAMP delay follows the trailing edge of horizontal sync in (HSIN). Delay is set by the CD register. Width of ICLAMP is set by the CW register. Range of CD and CW values is 1–255 pixels.

Sync Stripper

Some video signals include embedded composite sync rather than separate horizontal and vertical sync signals, typically sync on green. Composite sync is extracted from Composite Video at the ACS_{IN} pin.

When the ACS_{IN} signal falls below a 150mV ground referenced threshold, sync is detected. Composite Sync Output, DCS_{OUT} reflects the ACS_{IN} sync timing with non-inverted CMOS digital levels.

Power Down

$\overline{PWRDN}$ = L minimizes FMS9875 power consumption. Data outputs become high impedance. Clocks generation is stopped. Register contents are retained. Sync stripping and the internal voltage reference function.

Serial Interface

Register access is via a 2-wire I^2C/SMBus compatible interface. As a slave device, the 7-bit address is selected by the A_{1-0} pins (see Table 10). Serial port pins SDA and SCL communicate with the host SMBus/I^2C controller which act as a master.

Since the serial control port is design to interface with 3.3V logic, the pins must be protected, if SDA and SCL signals originate from 5V logic. Series connected 150Ω resistors are recommended. (See Applications Section)

Table 10. Serial Interface Address Codes

A_{1-0}	7-Bit Address
00	4C
01	4D
10	4E
11	4F

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). When receiving and transmitting data through the serial interface, the FMS9875 acts as a slave, responding only to commands by the I^2C/SMBus master.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA may change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.

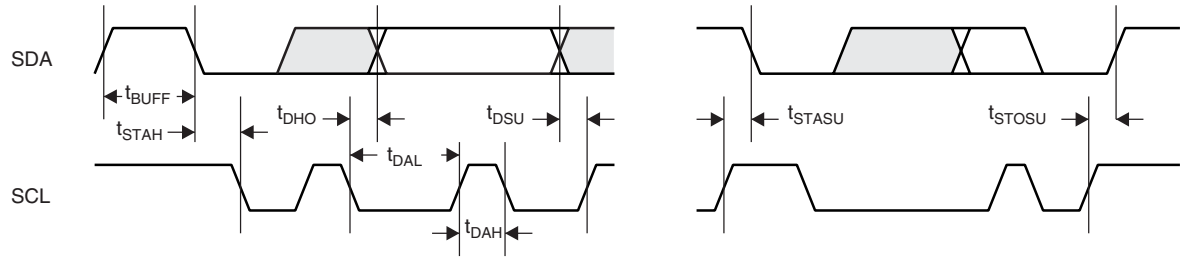


Figure 18. Serial Bus: Read/Write Timing

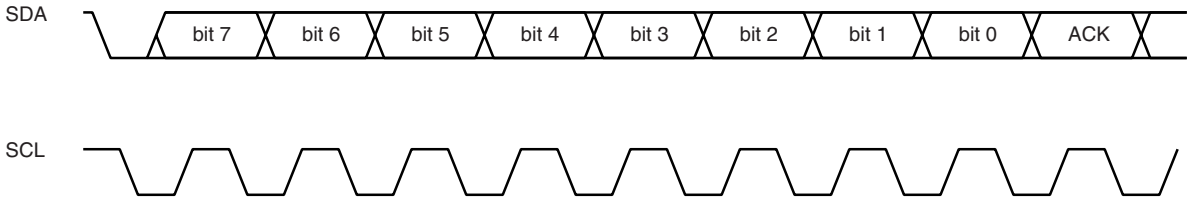


Figure 19. SerialBus: Typical Byte Transfer

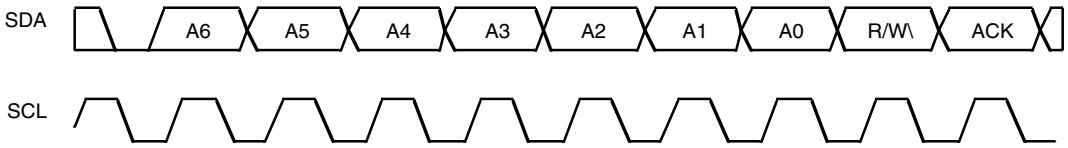


Figure 20. Serial Bus: Slave Address with Read/$\overline{\text{Write}}$ Bit

There are five steps within an I^2C/SMBus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the Serial Bus interface is inactive, SCL = H and SDA = H. Communications are initiated by sending a start signal (Figure 18, left waveform) that is a HIGH-to-LOW transition on SDA while SCL is HIGH. A start signal alerts all slaved devices that a data transfer sequence is imminent.

After a start signal, the first eight bits of data comprise a seven bit slave address followed a single R/W bit (Read = H, Write = L) to set the direction of data transfer: read from; or write to the slave device. If the transmitted slave address matches the address of the FMS9875 which set by the state of the ADD pin, the FMS9875 acknowledges by pulling SDA LOW on the 9th SCL pulse (see Figure 20). If the addresses do not match or the register being accessed is 0x0F, the FMS9875 does not acknowledge.

For each byte of data read or written, the MSB is the first bit of the sequence.

Data Transfer via Serial Interface

If a slave device, such as the FMS9875 does not acknowledge the master device during a write sequence, SDA remains HIGH so the master can generate a stop signal. During a read sequence, if the master device does not acknowledge by bringing SDA = L, the FMS9875 interprets SDA = H as “end of data.” SDA remains HIGH so the master can generate a stop signal.

To write data to a specific FMS9875 control register, three bytes are sent:

1. Write the slave address byte with bit R/$\overline{\text{W}}$ = L.
2. Write the pointer byte.
3. Write to the control register indexed by the pointer.

After each byte is written, the pointer auto-increments to allow multiple data byte transfers within one write cycle.

Data is read from the control registers of the FMS9875 in a similar manner, except that two data transfer operations are required:

1. Write the slave address byte with bit R/$\overline{\text{W}}$ = L.
2. Write the pointer byte.
3. Write the slave address byte with bit R/$\overline{\text{W}}$ = H
4. Read the control register indexed by the pointer.

After each byte is read, the pointer auto-increments to allow multiple data byte transfers within one read cycle.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle. After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH. (see Figure 18, right waveform)

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

Write to one register

1. Start signal
2. Slave Address byte (R/$\overline{W}$ bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Stop signal

Write to four consecutive registers

1. Start signal
2. Slave Address byte (R/$\overline{W}$ bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Data byte to (base address + 1)
6. Data byte to (base address + 2)
7. Data byte to (base address + 3)
8. Stop signal

Read from one register

1. Start signal
2. Slave Address byte (R/$\overline{W}$ bit = LOW)
3. Pointer byte (= base address)
4. Stop signal (optional)
5. Start signal
6. Slave Address byte (R/$\overline{W}$ bit = HIGH)
7. Data byte from base address
8. Stop signal

Read from four registers

1. Start signal
2. Slave Address byte (R/$\overline{W}$ bit = LOW)
3. Pointer byte (= base address)
4. Stop signal (optional)
5. Start signal
6. Slave Address byte (R/$\overline{W}$ bit = HIGH)
7. Data byte from base address
8. Data byte from (base address + 1)
9. Data byte from (base address + 2)
10. Data byte from (base address + 3)
11. Stop signal

Absolute Maximum Ratings
(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{CC} (Measured to GND)	-0.5		4	V
Digital Inputs				
Applied voltage (Measured to GND)[2]	-0.3		V_{DDA}	V
Forced current [3, 4]	-5.0		5.0	mA
Analog Inputs				
Applied Voltage (Measured to GND)[2]	-0.5		V_{DDA}	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
Applied voltage (Measured to GND)[2]	-0.5			V
Forced current [3, 4]	-6.0		6.0	mA
Forced current [3, 4]	-8.0		8.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:
1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DDA}	ADC Power Supply Voltage	3.0	3.3	3.6	V
V_{DDP}	PLL Power Supply Voltage	3.0	3.3	3.6	V
V_{DDO}	Output Power Supply Voltage	2.2	3.3	3.6	V
T_A	Ambient Temperature, Still Air	0		70	°C
V_{TMAX}	A/D analog input range, min.			550	mV p-p
V_{TMIN}	A/D analog input range, max.	875			mV p-p

Test Rank Definitions

Rank	
P	Production tested at 70°C.
D	Guaranteed by design over full temperature range.
C	Guaranteed by characterization and design over full temperature range.
T	Target specification, pending characterization.

Electrical Characteristics[1]

Parameter		Temp.	Test Rank	Min	Typ	Max	Unit
Power Supply Currents							
I_{DDA}	Supply current, ADC	25°C	P			220	mA
I_{DDD}	Supply current[2], Digital Output	25°C	P			50	mA
I_{DDP}	Supply current, PLL	25°C	P			50	mA
P_D	Power dissipation	Full	D			1100	mW
I_{PD}	Power-down current	Full	PC			30	mA
P_{DD}	Powered-down disspation	Full	D			100	mW
Digital Inputs/Outputs							
C_I	Input Capacitance	25°C	D		3		pF
I_{IH}	Input Current, HIGH	Full	PC	-2		+2	µA
I_{IL}	Input Current, LOW	Full	PC	-2		+2	µA
V_{IH}	Input Voltage, HIGH	Full	D	V_{DDD}–0.8			V
V_{IL}	Input Voltage, LOW	Full	D			0.8	V
I_{OHD}	Output Current, HIGH, data	Full	D		4		mA
I_{OHC}	Output Current, HIGH, clock	Full	D		8		mA
I_{OLD}	Output Current, LOW, data	Full	D		4		mA
I_{OLC}	Output Current, LOW, clock	Full	D		8		mA
V_{OH}	Output Voltage, HIGH (I_{OH} = max.)	Full	D	V_{DDO}–0.1			V
V_{OL}	Output Voltage, LOW (V_{DD3}) (I_{OL} = max.)	Full	D			0.1	V
Serial Bus I/O							
V_{SMIH}	Input Voltage, HIGH	Full	D	V_{DDD}–0.8			V
V_{SMIL}	Input Voltage, LOW	Full	D			0.8	V
V_{SMOL}	Output Voltage, LOW (I_{SMOL} = max.)	Full	D			0.1	V
I_{SMOH}	Output Current, HIGH	Full	D			1	µA
I_{SMOL}	Output Current, HIGH	Full	D		4		mA
Analog Inputs							
I_B	Input bias current	Full	PC			1	µA
E_{OS}	Input Offset Voltage[3]	Full	D	-75	0	+75	mV
V_{ACSIN}	Analog Composite Sync Threshold	Full	C	125	150	175	mV
Reference Output							
V_{REF}	Output Voltage	Full	PC	1.15	1.25	1.38	V
	Temperature Coefficient	Full	C		±50		ppm/°C

Notes:

1. Unless otherwise stated, 0 to 70°C
2. DCK, $\overline{DCK}$ load = 15 pF; data load = 5 pF.
3. With Gain = 102.

Switching Characteristics

Parameter			Temp.	Test Rank	Min.	Typ.	Max.	Unit
Analog-to-Digital Converters								
	Conversion rate	FMS9875KAC100	Full	CT	10		108	Ms/s
		FMS9875KAC140			10		140	
t_{SKEW}	DCK Clock to Data Out Skew		Full	CT	-0.5		2	ns
Timing Generator								
	HSIN input frequency		Full	C	15		110	kHz
	Maximum PLL clock rate	FMS9875KAC100	Full	CT	108			MHz
		FMS9875KAC140			140			
	Minimum PLL clock rate		Full	PC			12	MHz
	Sampling phase tempco		Full	C		20		ps/°C
Serial Bus Interface								
t_{DAL}	SCL Pulse Width, LOW		Full	C	4.7			µs
t_{DAH}	SCL Pulse Width, HIGH		Full	C	4.0			µs
t_{STAH}	SDA Start Hold Time		Full	C	4.0			µs
t_{STASU}	SCL to SDA Setup Time (Stop)		Full	C	4.7			µs
t_{STOSU}	SCL to SDA Setup Time (Start)		Full	C	4.0			µs
t_{BUFF}	SDA Stop Hold Time Setup		Full	C	4.7			µs
t_{DSU}	SDA to SCL Data Setup Time		Full	C	250			ns
t_{DHO}	SDA to SCL Data Hold Time		Full	C	0			ns

A/D Converter Performance Characteristics

Parameter		Temp.	Test Rank	Min.	Typ.	Max.	Unit
Analog to Digital Converter							
E_{LI}	Integral Linearity Error	Full	PC	-2.0		2.0	LSB
E_{LD}	Differential Linearity Error	Full	PC	-1.0		1.0	LSB
	Missing Codes	Full	PC			0	
	Input full scale matching[1]	Full	PC		2.5	6	%FS
	Offset adjustment range	Full	D		25		%FS
OS_Z	Offset Register Value to Zero Offset	Full	C	4	32	59	LSB
	Gain tempco	25°C	C		300		ppm/°C
B_W	Analog bandwidth, full power	25°C	D		400		MHz
	Transient response	25°C	C		2		ns
t_{OV}	Over-voltage recovery time	25°C	C		1.5		ns

Notes

1. Without offset trim. (OSGY = OSBP = OSRP = 32.)

PLL Performance Characteristics

Parameter			Temp.	Test Rank	Min.	Typ.	Max.	Unit
Clock Input								
t_{JPP}	Peak-to-peak PLL Jitter	**MHz**	25°C	C				ps
		31.5				6000		
		49.5				3117		
		78.75				1493		
		108				892		
		135				750		
t_{JRMS}	RMS Jitter	**MHz**	25°C	C				ps
		31.5				873		
		49.5				488		
		78.75				245		
		108				148		
		135				122		
t_{J2PP}	Peak-to-peak jitter with subdivide ratio equal to 2.	**MHz**	25°C	C				ps
		31.5				1600		
		49.5				1700		
t_{J2RMS}	RMS jitter with subdivide ratio equal to 2.	**MHz**	25°C	C				ps
		31.5				330		
		49.5				203		

Notes

1. In Figures 21-23, the dashed curve is with subdivide ratio = 2.

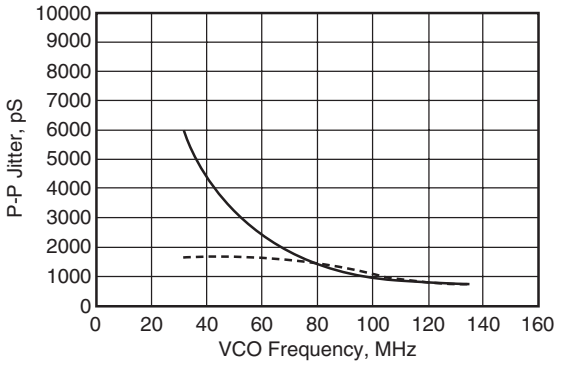


Figure 21. Pixel Clock Peak-to-Peak Jitter

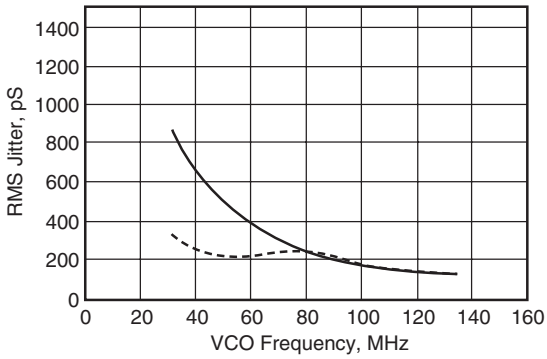


Figure 22. Pixel Clock RMS Jitter

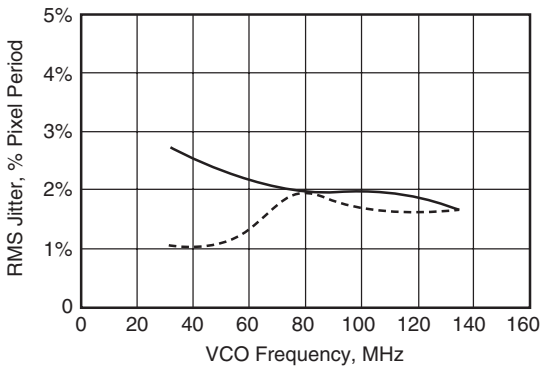


Figure 23. Pixel Clock % RMS Jitter

Applications Information

For additional applications information see Applications Notes available from the factory.

To minimize component count, use of the following on-chip circuits is recommended:

1. ADC sampling clock.
2. Clamp.
3. Voltage reference

Optimum PLL Configuration Register (address 0x0C) settings for typical modes are listed in Table 7. Unless otherwise indicated, all modes are compliant with VESA or SMPTE specifications. For unlisted modes, values should be adjusted to optimize performance.

By adjusting the values in the gain (GRP, GGY, GBP) and offset (OSRO, OSGY, OSBP) registers, the input conversion range can be matched to the incoming analog signals.

AC Coupled Digitizer

Shown in Figure 24 is an implementation of a video digitizer with AC coupled YP_BP_Rinputs. Horizontal sync input.

Output data is three channel 24-bit pixels with a maximum rate of 140Ms/s. Data is clocked out on the negative edge of DCK. HSOUT is delayed HSIN.

Control is through the serial port with 150Ω resistors inserted to allow interfacing with 5V logic. If the serial bus is operates with 3.3V levels, these resistors are unnecessary.

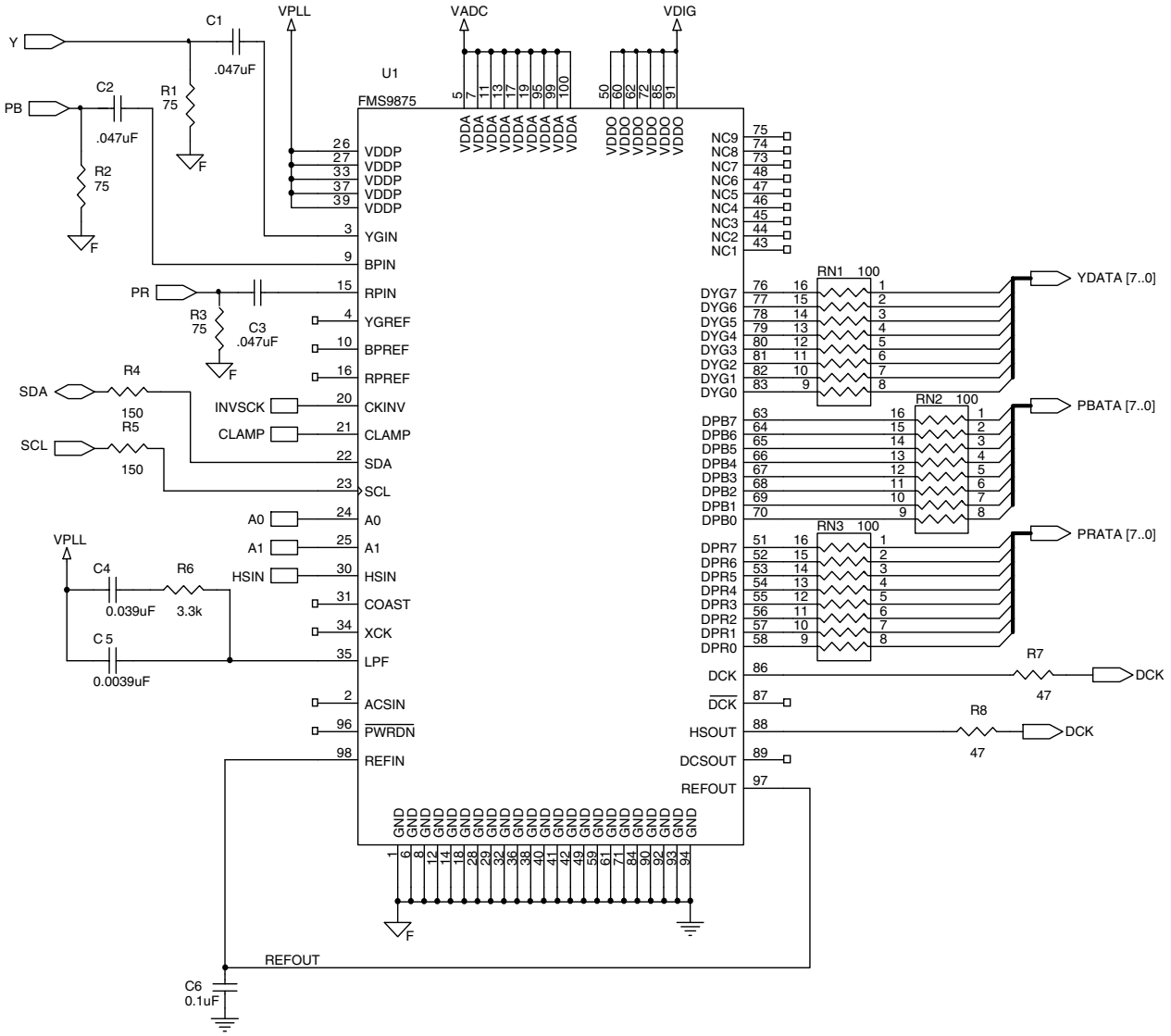


Figure 24. Schematic, VGA Digitizer, AC Coupled RGB

Printed Wiring Board Design Guidelines

Recommended strategy is to mount the FMS9875 over a ground plane with carefully routed analog inputs and digital outputs. All connections should be treated as transmission lines to ensure that reflections due to mismatches are minimized and ground return currents do not interfere with critical signals.

Analog Inputs

Recommendations:

1. Keep analog trace lengths short to minimize crosstalk.
2. Terminate analog inputs with 75Ω resistors, placed close to the FMS9875 analog inputs, R_{IN}, G_{IN} and B_{IN}. By matching transmission line impedances, reflections will be minimized.
3. Layout traces as 75Ω transmission lines.
4. Avoid running analog traces near digital traces. Due to the wide input bandwidth (400MHz) digital noise can easily leak into analog inputs or cause excessive PLL jitter.
5. If necessary, limit bandwidth by adding a ferrite bead in series with each RGB input as shown in Figure 25. A Fair-Rite #2508051217Z0 is recommended. Alternatively, bandwidth reduction using a shunt 10pF capacitor may reduce snow (intensity noise) caused by HF noise riding on the RGB input. Mismatches, reflections and noise may cause ringing or distortion of the incoming video signals.
6. Locate the PLL filter close to the FMS9875 package and clear of other signals.
7. Bypass the reference with a 0.1µF capacitor to ground.

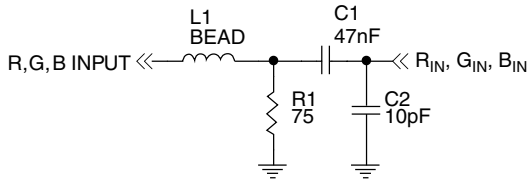


Figure 25. RGB Input Filter Options

Digital I/O

Recommendations:

1. Route digital I/O signals clear of analog inputs.
2. Terminate clock lines to reduce reflections. Treat clock lines as transmission lines.
3. Scale the HSIN input to 3.3V, using a resistor network or a series 1 kΩ resistor.
4. Limit Serial Port inputs voltages applied to SDA and SDL pins with 150Ω resistors connected directly to the pins.
5. If necessary, to reduce reflections, EMI or spikes add a 50–200Ω resistor at each data output pin.
6. If necessary, to reduce reflections, EMI or spikes add a 50–200Ω resistor at each data output pi.
7. To minimize noise within the FMS9875, restrict the capacitive load at the digital outputs to < 10pF.

Power and Ground

A schematic of the recommended power distribution is shown in Figure 26. Note that:

1. Analog and digital circuits are layed out over a common solid ground plane.
2. Each FMS9875 pin is decoupled with a 0.1µF capacitor.
3. A group of pins may be de-coupled through a common capacitor if no pin is more than 5 mm from the capacitor.
4. A separate regulated supply is used for the phase-locked loop power supply, V_{DDP}.
5. Capacitors are attached to each PLL pin or pin-pair.

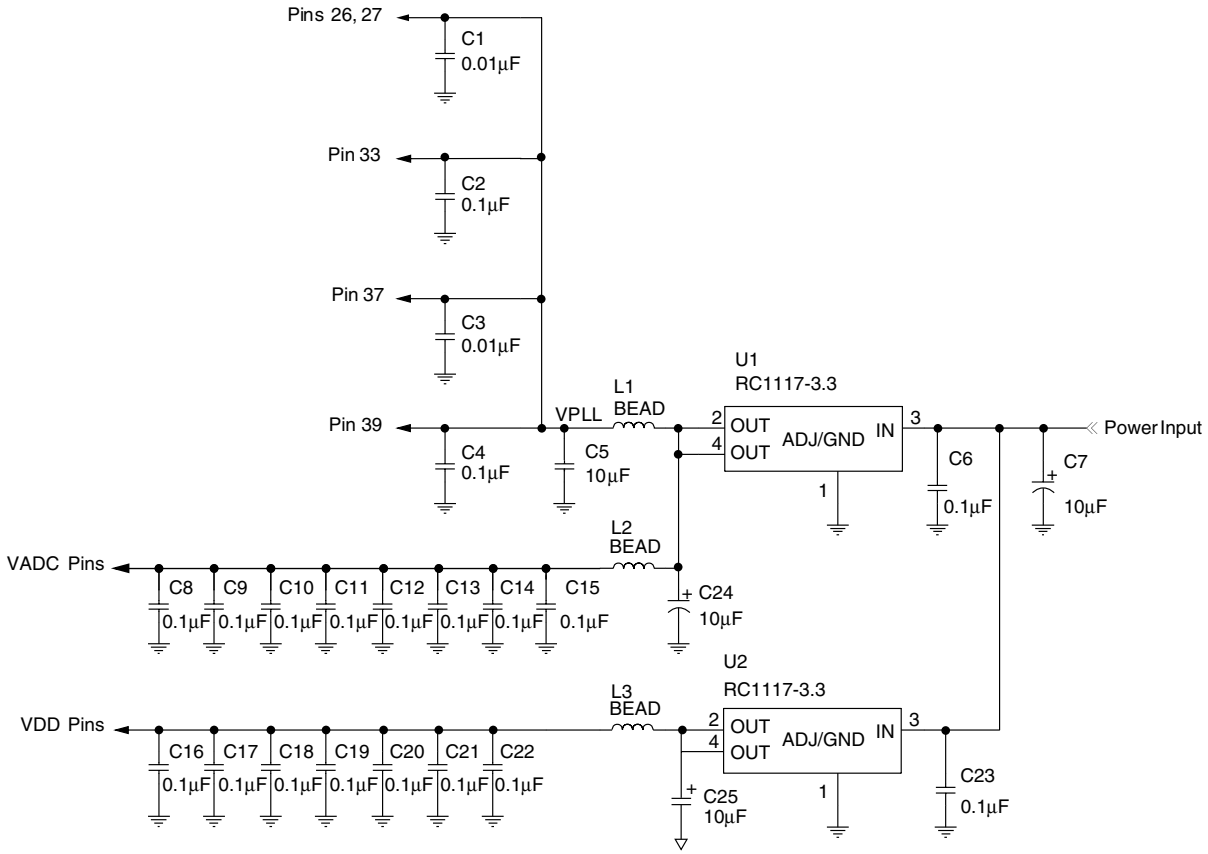


Figure 26. Recommended Power Distribution

Physical placement of PLL power supply decoupling components is critical. Bearing in mind the following suggestions:

1. All components should be placed in close proximity to the FMS9875 pins.
2. Routing through vias should be avoided, if possible.
3. Each V_{DDP}/GND pin pair: 26&27/28, 33/32, 37/38, and 39/40 should be decoupled with a either a 0.01 or 0.1 µF capacitor (see Figure 24).
4. Use Fair-rite 274 301 9447 bead.

Firmware

Best performance can be achieved by correctly setting the FMS9875 registers. Here are some recommendations:

1. For analog video, the sampling rate is usually 2X–3X the video bandwidth. PLLN and PHASE are not critical.
2. For PC video, set the value of PLLN equal to the number of pixels to be sampled minus one. With this setting, the number of samples per horizontal line equals the number of pixels. If PLLN + 1 does not equal the number of pixels, there will be irregular intensities on text and an interference pattern on a vertical grill pattern.
3. In the GBR mode, calibrate Offset and Gain by first setting each input to 0mV. Then adjust OSGY, OSBP, and OSRP to set each RGB data output D_{7-0} = 0x00. Next with 700mV input, adjust GGY, GBP and GRP so that each RGB data output D_{7-0} = (same value), typically 240 decimal. Average values during calibration to minimize the impact of noise.
4. In the YP_BP_R mode, the Y-channel calibration procedure is the same as for GBR. P_BP_R channels must be calibrated differently. If the internal mid-scale clamp is used, Offset is automatically preset. Only the Gain need be adjusted to accomodate the swing from peak blue to peak orange on the P_B channel; and peak red to peak cyan onthe P_R channel. Average values during calibration to minimize the impact of noise.
5. Clamp registers, CD and CW, should be programmed to maximize the period of the clamp during the backporch, while not encroaching into the sync or active video periods.
6. PHASE must be trimmed to minimize onscreen snow (intensity noise) when a vertical grill pattern is displayed.
7. FVCO must be set to encompass the incoming frequency range.
8. IPUMP must be set to minimize intensity noise.
9. To ensure correct power-on defaults, program all registers including Test Register 0x0F, which must be set to 0x00 for normal operation. Note that unlike registers 0x00 through 0x0D, register 0x0F does not acknowledge. The ACK bit remains H instead of being pulled L.

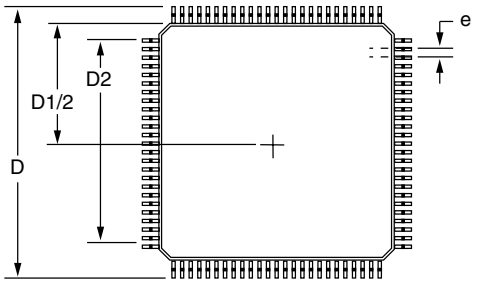
Mechanical Dimensions

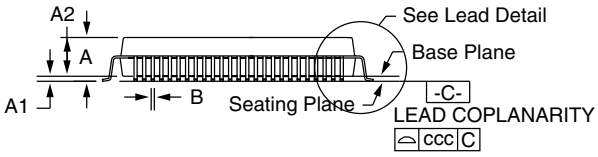
100-Lead MQFP (KG) Package

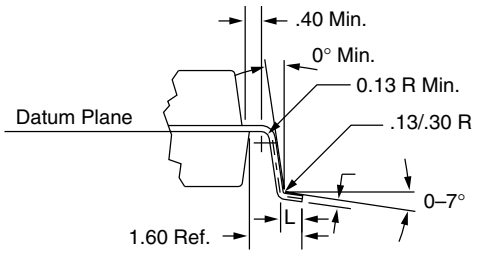
Symbol	Millimeters			Notes
	Min.	Typ.	Max	
A	—	2.82	3.00	
A1	—	0.15	—	
A2	2.62	2.67	2.77	3, 5
D		17.20 BSC		
D1		14.00 BSC		
D2		12.00 BSC		
L	0.73	0.88	1.03	4
N		100		
e		0.50 BSC		
b	0.17	—	0.27	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1994.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm per side.
3. "N" is the number of terminals, 25 per side.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm in excess of the "b" dimension at the maximum material condition.







Lead Detail

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
FMS9875KGC100	0°C to 70°C	Commercial	100 Lead MQFP	9875KGC100
FMS9875KGC100X	0°C to 70°C	Commercial	100 Lead MQFP with Tape and Reel	9875KGC100
FMS9875KGC140	0°C to 70°C	Commercial	100 Lead MQFP	9875KGC140
FMS9875KGC140X	0°C to 70°C	Commercial	100 Lead MQFP with Tape and Reel	9875KGC140