CIRRUS LOGIC®

CS5361

114 dB, 192 kHz, Multi-Bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-Bit Conversion
- 114 dB Dynamic Range
- -105 dB THD+N
- System Sampling Rates up to 192 kHz
- Less than 150 mW Power Consumption
- High Pass Filter or DC Offset Calibration
- Supports Logic Levels Between 5 and 2.5V
- Differential Analog Architecture
- Linear Phase Digital Anti-Alias Filtering
- Overflow Detection

General Description

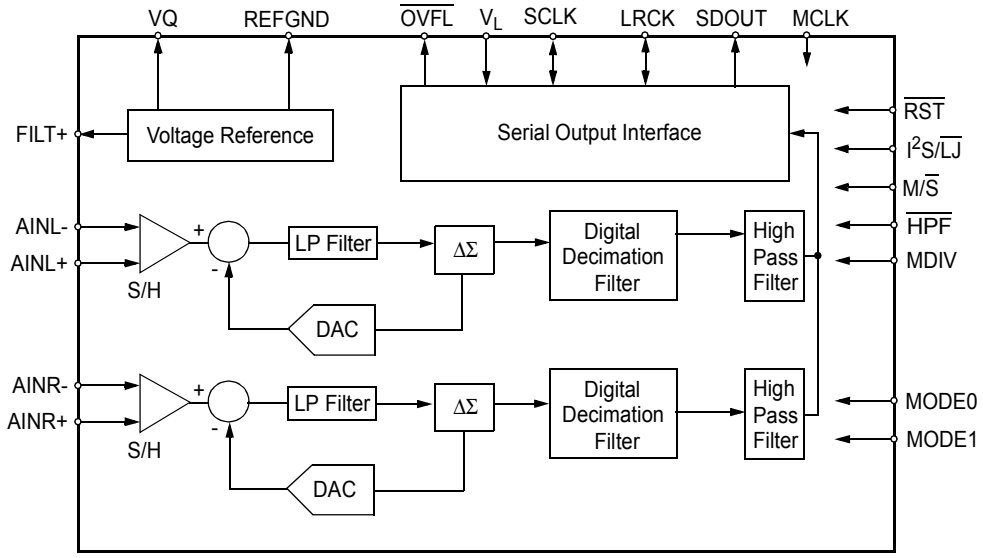
The CS5361 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 192 kHz per channel.

The CS5361 uses a 5th-order, multi-bit delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5361 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD-R, CD-R, digital mixing consoles, and effects processors.

ORDERING INFORMATION

CS5361-KS	-10° to 70° C	24-pin SOIC
CS5361-BS	-40° to 85° C	24-pin SOIC
CS5361-KZ	-10° to 70° C	24-pin TSSOP
CS5361-BZ	-40° to 85° C	24-pin TSSOP
CDB5361	Evaluation Board	



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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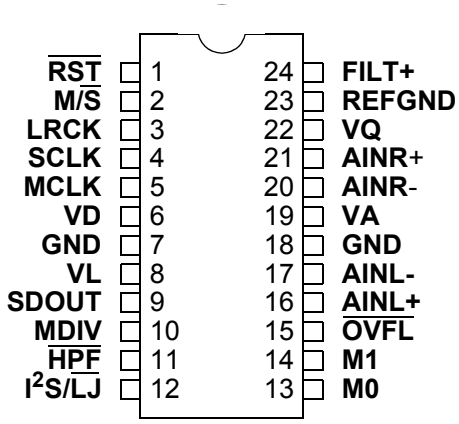
1 PIN DESCRIPTIONS



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - The device enters a low power mode when low.
M/S	2	**Master/Slave Mode** *(Input)* - Selects operation as either clock master or slave.
LRCK	3	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	4	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	7,18	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VL	8	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	9	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MDIV	10	**MCLK Divider** *(Input*) **-** Enables a master clock divide by two function.
HPF	11	**High Pass Filter Enable** *(Input*) **-** Enables the Digital High-Pass Filter.
I2S/LJ	12	**Serial Audio Interface Format Select** (*Input*) -Selects either the left-justified or I^2S format for the SAI.
M0 M1	13, 14	**Mode Selection** (*Input*) - Determines the operational mode of the device.
OVFL	15	**Overflow** *(Output, open drain)* **-** Detects an overflow condition on both left and right channels.
AINL+ AINL-	16, 17	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VA	19	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
AINR- AINR+	20, 21	**Differential Right Channel Analog Input** (*Input*) -Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
VQ	22	**Quiescent Voltage** *(Output)* **-** Filter connection for the internal quiescent reference voltage.
REF_GND	23	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
FILT+	24	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

2 TYPICAL CONNECTION DIAGRAM

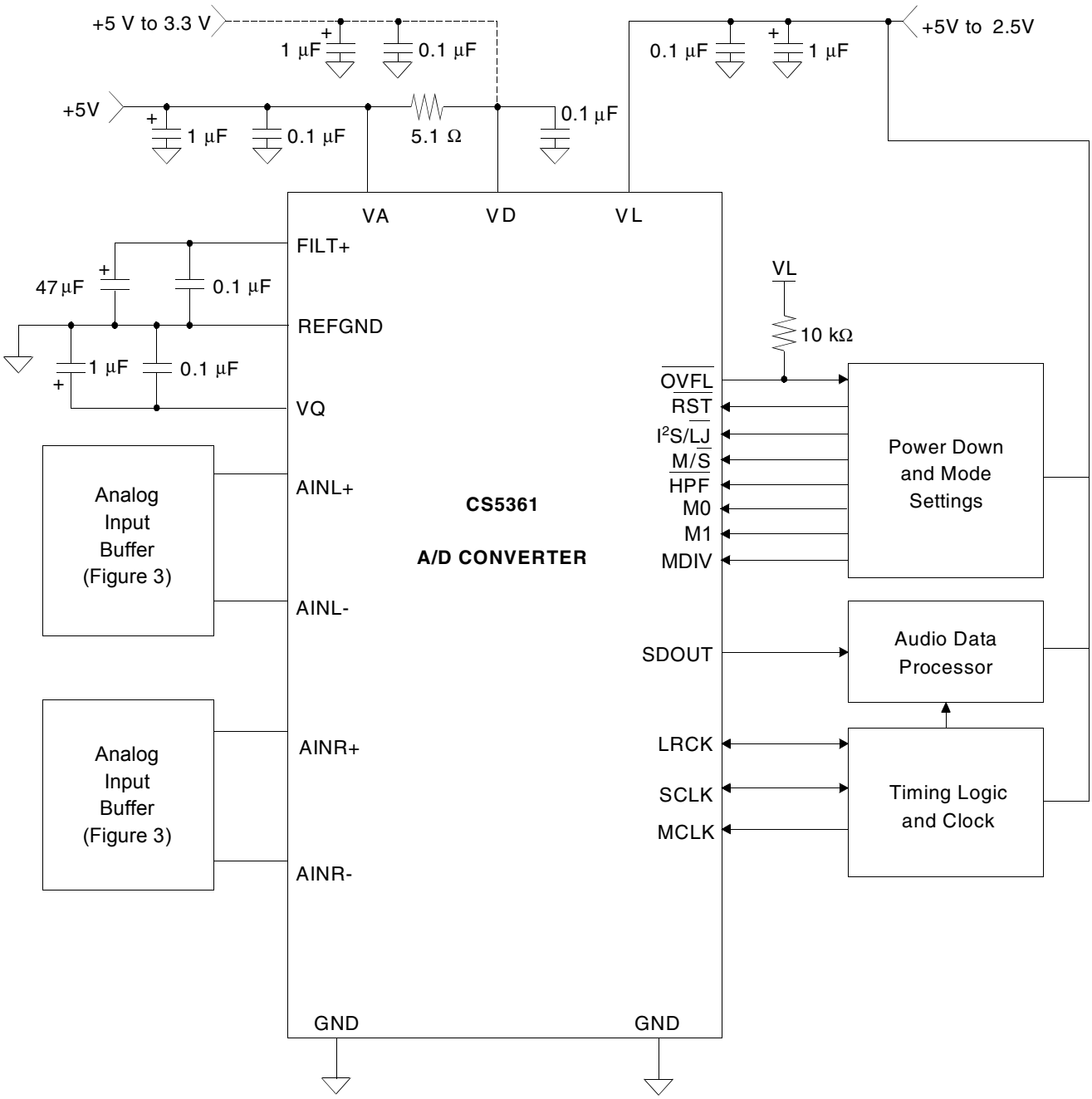


Figure 1. Typical Connection Diagram

3 APPLICATIONS

3.1 Operational Mode/Sample Rate Range Select

The output sample rate, Fs, can be adjusted from 2kHz to 192kHz. The CS5361 must be set to the proper speed mode via the mode pins, M1 and M0. Refer to Table 1.

M1 (Pin 14)	M0 (Pin 13)	MODE	Output Sample Rate (Fs)
0	0	Single Speed Mode	2kHz - 50kHz
0	1	Double Speed Mode	50kHz - 100kHz
1	0	Quad Speed Mode	100kHz - 192kHz
1	1	Reserved	

Table 1. CS5361 Mode Control

3.2 System Clocking

The device supports operation in either Master Mode, where the left/right and serial clocks are synchronously generated on-chip, or Slave Mode, which requires external generation of the left/right and serial clocks. The device also includes a master clock divider in Master Mode where the master clock will be internally divided prior to any other internal circuitry when MDIV is enabled, set to logic 1. In Slave Mode, the MDIV pin needs to be disabled, set to logic 0.

3.2.1 Master Mode

In Master mode, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 2. Refer to Table 2 for common master clock frequencies.

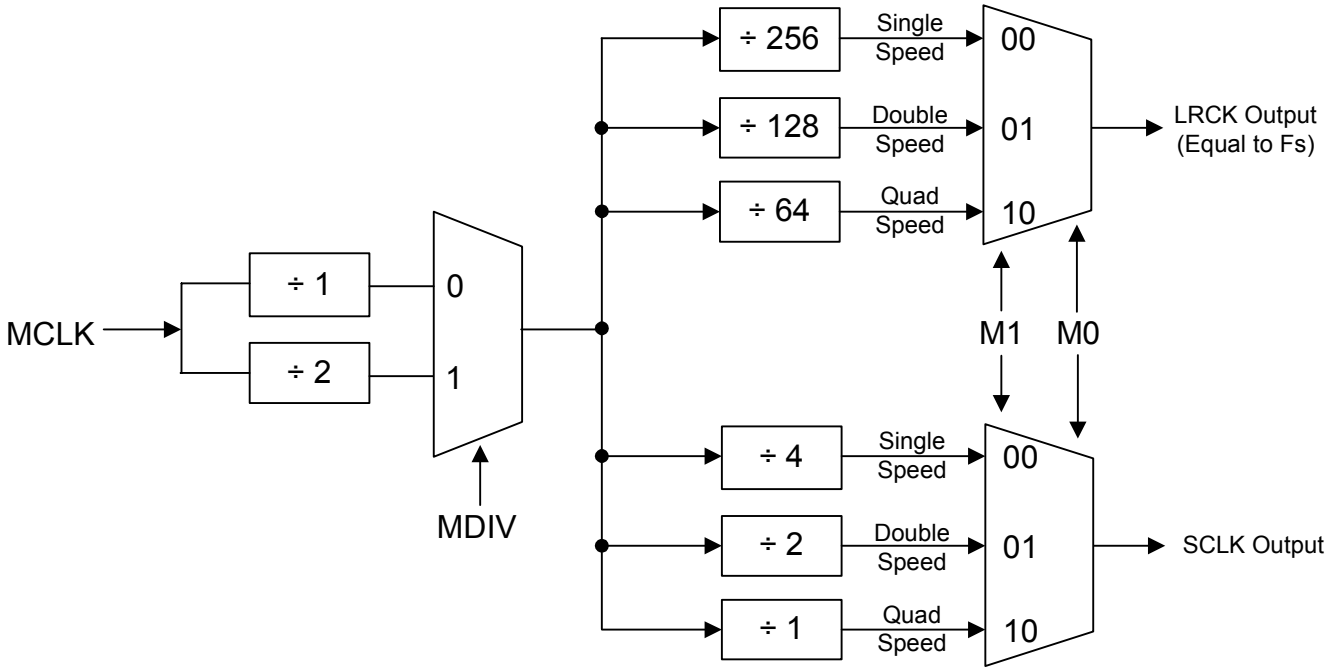


Figure 2. CS5361 Master Mode Clocking

SAMPLE RATE (kHz)	MDIV = 0 MCLK (MHz)	MDIV = 1 MCLK (MHz)
32	8.192	16.384
44.1	11.2896	22.5792
48	12.288	24.576
64	8.192	16.384
88.2	11.2896	22.5792
96	12.288	24.576
176.4	11.2896	22.5792
192	12.288	24.576

Table 2. CS5361 Common Master Clock Frequencies

3.2.2 Slave Mode

LRCK and SCLK operate as inputs in Slave mode. The left/right clock must be synchronously derived from the master clock and be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance. Refer to Table 3 for required clock ratios.

	Single Speed Mode Fs = 2kHz to 50kHz	Double Speed Mode Fs = 50kHz to 100kHz	Quad Speed Mode Fs = 100kHz to 192kHz
MCLK/LRCK Ratio	256x, 512x	128x, 256x	128x, 256x
SCLK/LRCK Ratio	32x, 64x, 128x	32x, 64x	64x

Table 3. CS5361 Slave Mode Clock Ratios

3.3 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

The internal reference voltage must be stable for the device to produce valid data. Therefore, there is a delay between the release of reset and the generation of valid output, due to the finite output impedance of FILT+ and the presence of the external capacitance.

3.4 Analog Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) the digital passband frequency, where n=0,1,2,...Refer to Figure 3 which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

Please see the Addendum at the end of the datasheet for an analog input buffer that can be used with both the CS5351 as well as the CS5361 with a simple change in the bill of materials.

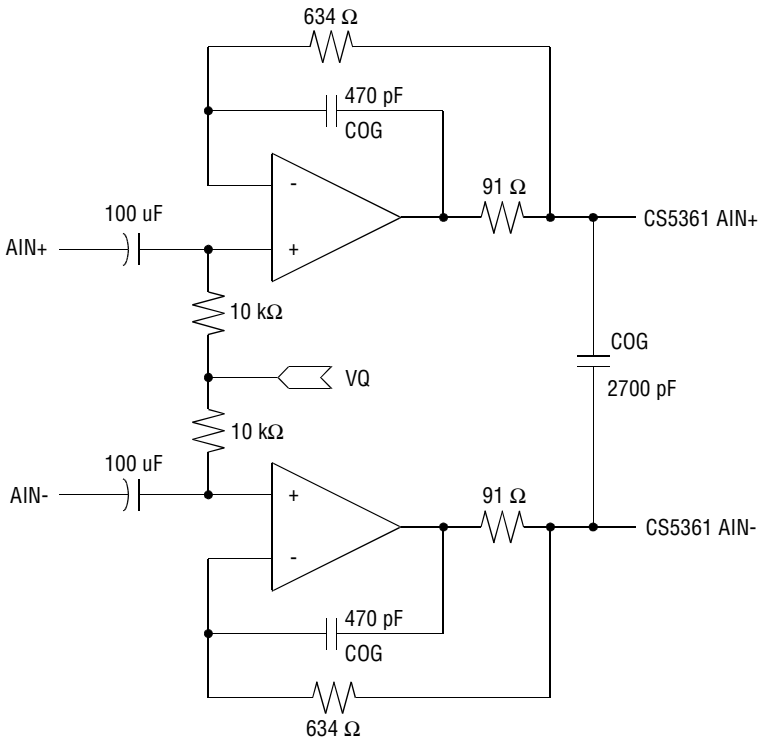


Figure 3. CS5361 Recommended Analog Input Buffer

3.5 High Pass Filter and DC Offset Calibration

The operational amplifiers in the input circuitry driving the CS5361 may generate a small DC offset into the A/D converter. The CS5361 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the $\overline{\text{HPF}}$ pin is taken high during normal operation, the current value of the DC offset register is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1) Running the CS5361 with the high pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2) Disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5361.

3.6 Overflow Detection

The CS5361 includes overflow detection on both the left and right channels. This time multiplexed information is presented as open drain, active low on pin 15, $\overline{\text{OVFL}}$. The OVFL_L and OVFL_R data will go to a logical low as soon as an overrange condition in either channel is detected. The data will remain low

as specified in the Switching Characteristics - Serial Audio Port section. This ensures sufficient time to detect an overrange condition regardless of the speed mode. After the timeout, the OVFL_L and OVFL_R data will return to a logical high if there has not been any other overrange condition detected. Please note that an overrange condition on either channel will restart the timeout period for both channels.

3.6.1 $\overline{OVFL}$ Output Timing

In left-justified format, the $\overline{OVFL}$ pin is updated one SCLK period after an LRCK transition. In I^2S format, the $\overline{OVFL}$ pin is updated two SCLK periods after an LRCK transition. Refer to Figures 23 and 24. In both cases the $\overline{OVFL}$ data can be easily demultiplexed by using the LRCK to latch the data. In left-justified format, the rising edge of LRCK would latch the right channel overflow status, and the falling edge of LRCK would latch the left channel overflow status. In I^2S format, the falling edge of LRCK would latch the right channel overflow status and the rising edge of LRCK would latch the left channel overflow status.

3.7 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5361 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REFGND. The CDB5361 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

3.8 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS5361's in the system. If only one master clock source is needed, one solution is to place one CS5361 in Master mode, and slave all of the other CS5361's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5361 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

4 CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (CS5361-KS/KZ)

(Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz. Typical performance characteristics are derived from measurements taken at T_A = 25°C, VL = VD = 3.3V and VA = 5.0V. Min/Max performance characteristics are guaranteed over the specified operating temperature and voltages.)

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode	**Fs = 48kHz**					
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-105	-99	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-	dB
Double Speed Mode	**Fs = 96kHz**					
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	dB
	40kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-105	-99	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-	dB
	40kHz bandwidth -1dB		-	-102	-	dB
Quad Speed Mode	**Fs = 192kHz**					
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	dB
	40kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-105	-99	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-	dB
	40kHz bandwidth -1dB		-	-102	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage (at VA = 5V)			1.9	2.0	2.1	Vrms
Input Impedance (Differential)	(Note 2)		37	-	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

Notes: 1. Referred to the typical full-scale input voltage.

ANALOG CHARACTERISTICS (CS5361-BS/BZ)

((Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz. Typical performance characteristics are derived from measurements taken at T_A = 25°C, VL = VD = 3.3V and VA = 5.0V. Min/Max performance characteristics are guaranteed over the specified operating temperature and voltages.)

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode	**Fs = 48kHz**					
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111	-	dB
Total Harmonic Distortion + Noise		THD+N				
	-1 dB		-	-105	-97	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-	dB
Double Speed Mode	**Fs = 96kHz**					
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111	-	dB
	40kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-105	-97	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-	dB
	40kHz bandwidth -1dB		-	-102	-	dB
Quad Speed Mode	**Fs = 192kHz**					
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111	-	dB
	40kHz bandwidth unweighted		-	108	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-105	-97	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	-	dB
	40kHz bandwidth -1dB		-	-102	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage (at VA = 5V)			1.8	2.0	2.2	Vrms
Input Impedance (Differential)	(Note 2)		37	-	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

Notes: 2. Measured between AIN+ and AIN-

DIGITAL FILTER CHARACTERISTICS

Parameter			Symbol	Min	Typ	Max	Unit
Single Speed Mode (2kHz to 50kHz sample rates)							
Passband	(-0.1 dB)	(Note 3)		0	-	0.47	Fs
Passband Ripple				-	-	±0.035	dB
Stopband		(Note 3)		0.58	-	-	Fs
Stopband Attenuation				-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.0	µs
Double Speed Mode (50kHz to 100kHz sample rates)							
Passband	(-0.1 dB)	(Note 3)		0	-	0.45	Fs
Passband Ripple				-	-	±0.035	dB
Stopband		(Note 3)		0.68	-	-	Fs
Stopband Attenuation				-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.0	µs
Quad Speed Mode (100kHz to 192kHz sample rates)							
Passband	(-0.1 dB)	(Note 3)		0	-	0.24	Fs
Passband Ripple				-	-	±0.035	dB
Stopband		(Note 3)		0.78	-	-	Fs
Stopband Attenuation				-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0.0	µs
High Pass Filter Characteristics							
Frequency Response	-3.0 dB			-	1	-	Hz
	-0.13 dB	(Note 4)			20	-	Hz
Phase Deviation	@ 20Hz	(Note 4)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Settling Time					10^5/Fs		s

Notes: 3. The filter frequency response scales precisely with Fs.

4. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

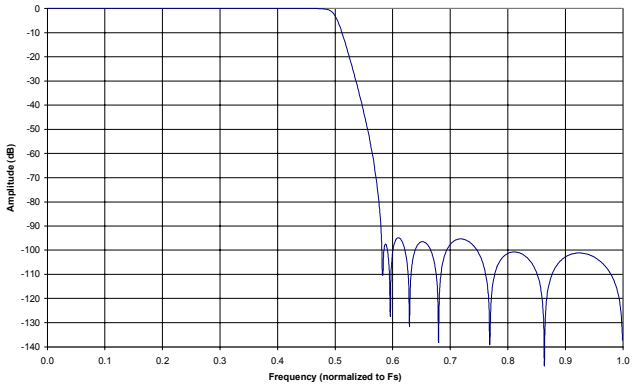


Figure 4. Single Speed Mode Stopband Rejection

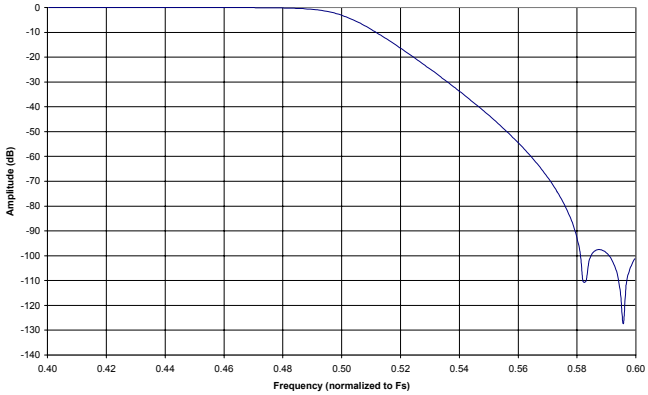


Figure 5. Single Speed Mode Transition Band

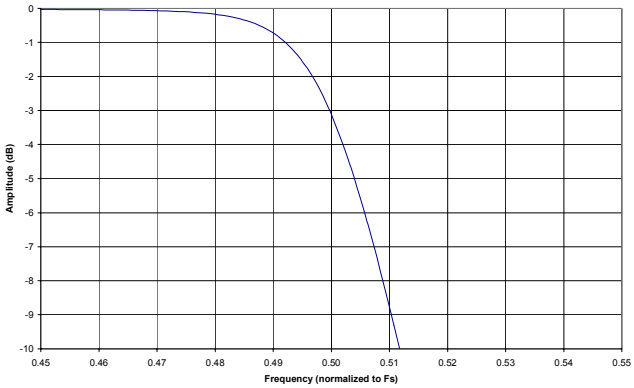


Figure 6. Single Speed Mode Transition Band (Detail)

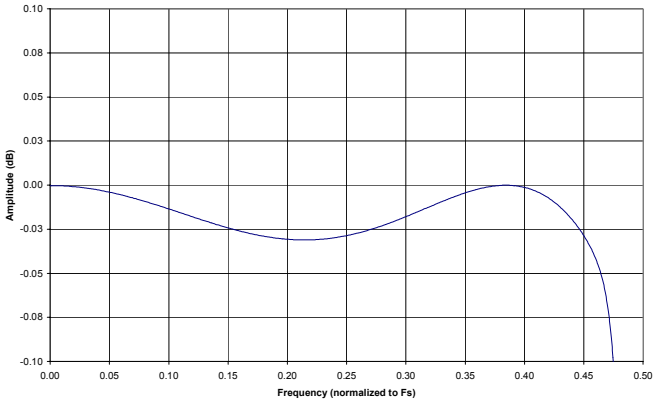


Figure 7. Single Speed Mode Passband Ripple

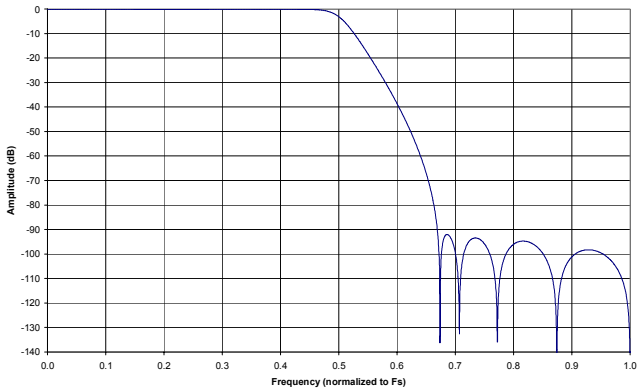


Figure 8. Double Speed Mode Stopband Rejection

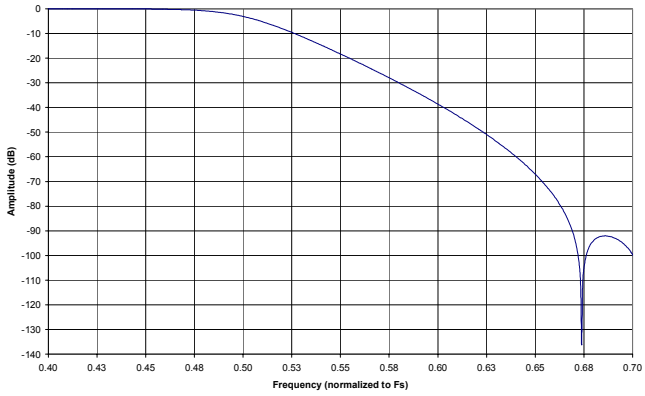


Figure 9. Double Speed Mode Transition Band

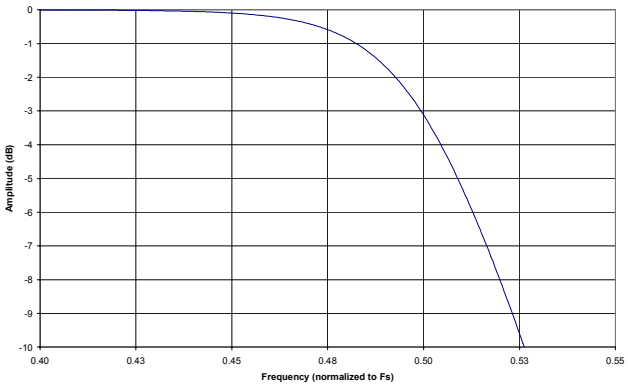


Figure 10. Double Speed Mode Transition Band (Detail)

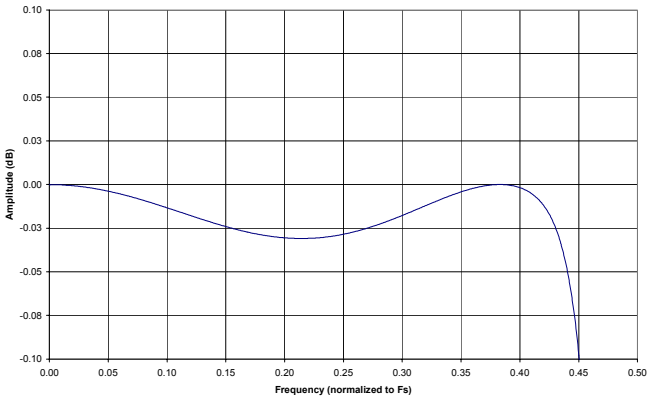


Figure 11. Double Speed Mode Passband Ripple

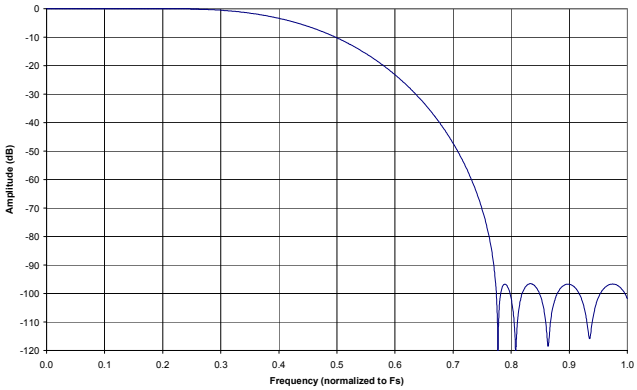


Figure 12. Quad Speed Mode Stopband Rejection

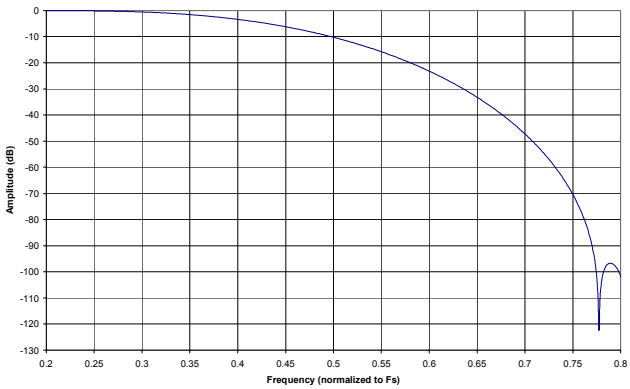


Figure 13. Quad Speed Mode Transition Band

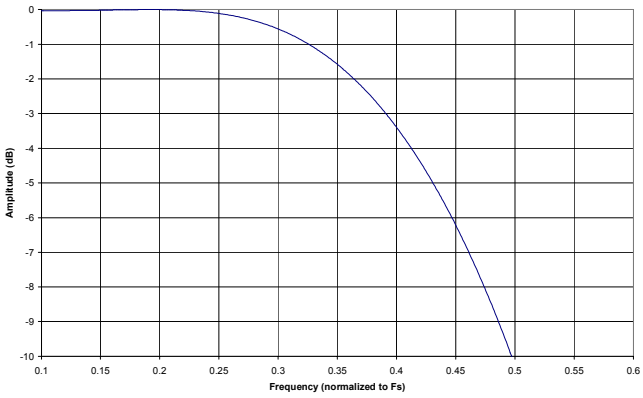


Figure 14. Quad Speed Mode Transition Band (Detail)

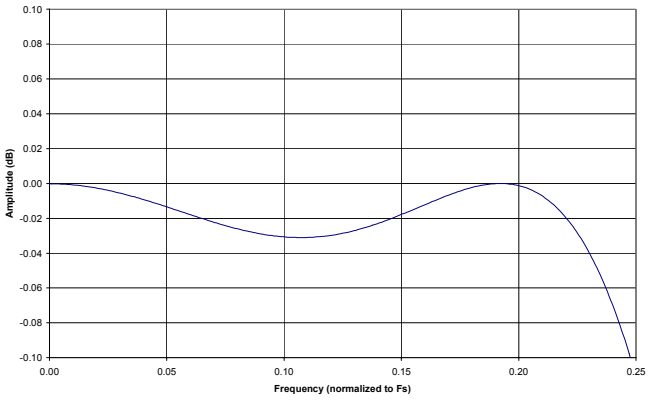


Figure 15. Quad Speed Mode Passband Ripple

DC ELECTRICAL CHARACTERISTICS (GND = 0V, all voltages with respect to ground. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Digital	VD	3.1	-	5.25	V
	Positive Logic	VL	2.37	-	5.25	V
Power Supply Current	VA	I_A	-	17.5	21	mA
(Normal Operation)	VL,VD = 5 V	I_D	-	22	26	mA
	VL,VD = 3.3V	I_D	-	14.5	17	mA
Power Supply Current	VA	I_A	-	2	-	mA
(Power-Down Mode)(Note 5)	VL,VD=5V	I_D	-	2	-	mA
Power Consumption						
(Normal Operation)	VL, VD=5V	-	-	198	235	mW
	VL, VD = 3.3V	-	-	135	161	mW
	(Power-Down Mode)	-	-	20	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 6)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	2.5	-	V
Output Impedance			-	25	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	5	-	V
Output Impedance			-	18	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

Notes: 5. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

6. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 100 uA	(% of VL)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o = 100 uA	(% of VL)	V_{OL}	-	-	15%	V
$\overline{OVFL}$ Current Sink		I_{ovfl}	-	-	4.0	mA
Input Leakage Current		I_{in}	-	-	±10	µA

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature			-	-	135	°C
Junction to Ambient Thermal Impedance		θ_{JA}	-	70	-	°C/W
Ambient Operating Temperature (Power Applied)	-KS	T_A	-10	-	+70	°C
	-BS	T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS (GND = 0V, All voltages with respect to ground.) (Note 7)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Logic	VL	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
Input Current	(Note 8)	I_{in}	-	-	±10	mA
Analog Input Voltage	(Note 9)	V_{IN}	GND-0.7	-	VA+0.7	V
Digital Input Voltage	(Note 9)	V_{IND}	-0.7	-	VL+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-50	-	+95	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 7. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

8. The maximum over/under voltage is limited by the input current.

9. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic "0" = GND = 0 V; Logic "1" = VL = 1.7V to 5.25V, VA = 5V±5%, VD = 3.1V to 5.25V, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Input Sample Rate Single Speed Mode	Fs	2	-	50	kHz
Double Speed Mode	Fs	50	-	100	kHz
Quad Speed Mode	Fs	100	-	192	kHz
$\overline{OVFL}$ to LRCK edge setup time	t_{setup}	$16/f_{sclk}$	-	-	s
$\overline{OVFL}$ to LRCK edge hold time	t_{hold}	$1/f_{sclk}$	-	-	s
$\overline{OVFL}$ time-out on overrange condition					
Fs = 44.1, 88.2, 176.4kHz		-	740	-	ms
Fs = 48, 96, 192kHz		-	680	-	ms
MCLK Specifications					
MCLK Period	t_{clkw}	40	-	1953	ns
MCLK Pulse Width High	t_{clkh}	15	-	-	ns
MCLK Pulse Width Low	t_{clkl}	15	-	-	ns
Master Mode					
SCLK falling to LRCK	t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid	t_{sdo}	0	-	40	ns
SCLK Duty Cycle		-	50	-	%
SCLK Output Frequency		-	50	-	%
Slave Mode					
Single Speed					
Output Sample Rate	Fs	2	-	50	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	163	-	-	ns
SCLK High/Low	t_{sclkhl}	20	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	40	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Double Speed					
Output Sample Rate	Fs	50	-	100	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	163	-	-	ns
SCLK High/Low	t_{sclkhl}	20	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	40	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Quad Speed					
Output Sample Rate	Fs	100	-	192	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	81	-	-	ns
SCLK High/Low	t_{sclkhl}	20	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	20	ns
SCLK falling to LRCK edge	t_{slrd}	-10	-	10	ns

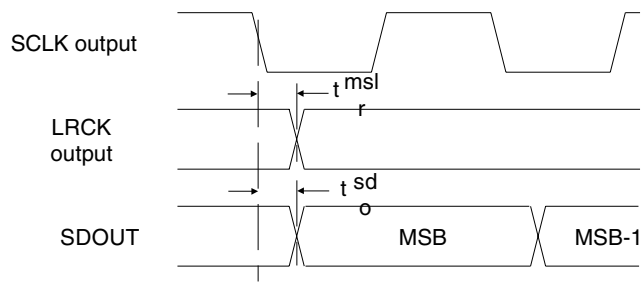


Figure 16. Master Mode, Left Justified SAI

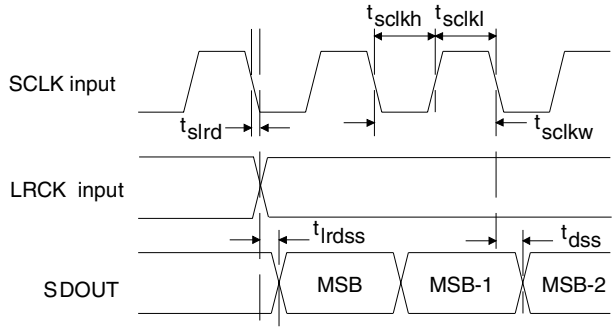


Figure 17. Slave Mode, Left Justified SAI

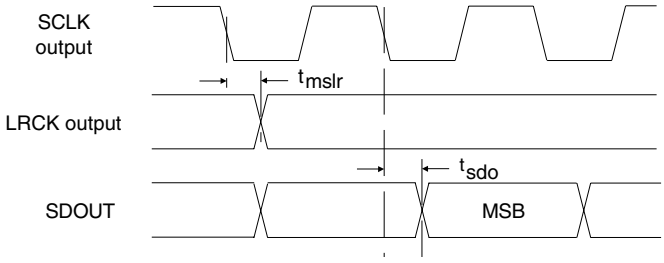


Figure 18. Master Mode, I²S SAI

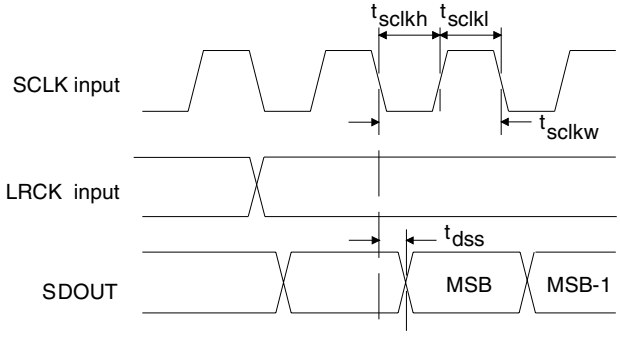


Figure 19. Slave Mode, I²S SAI

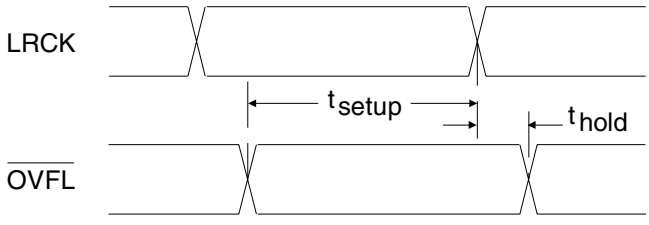


Figure 20. $\overline{\text{OVFL}}$ Output Timing

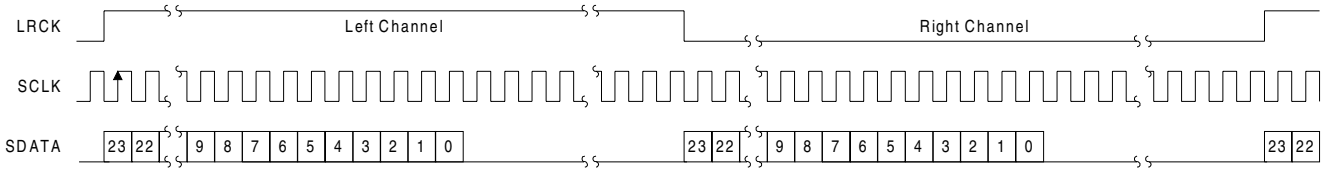


Figure 21. Left Justified Serial Audio Interface

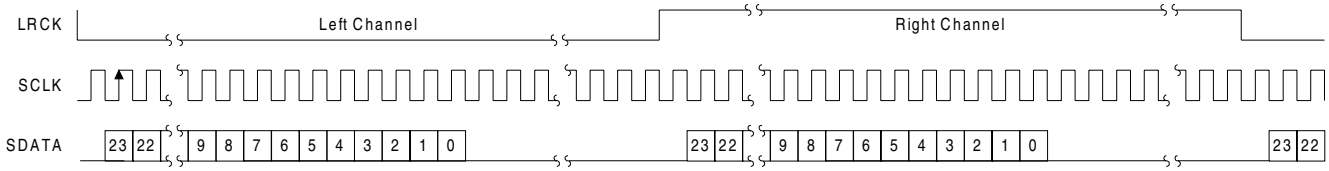


Figure 22. I²S Serial Audio Interface

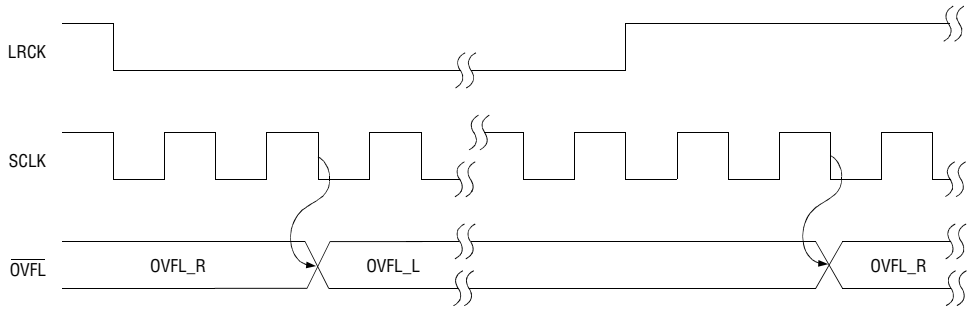


Figure 23. $\overline{\text{OVFL}}$ Output Timing, I²S Format

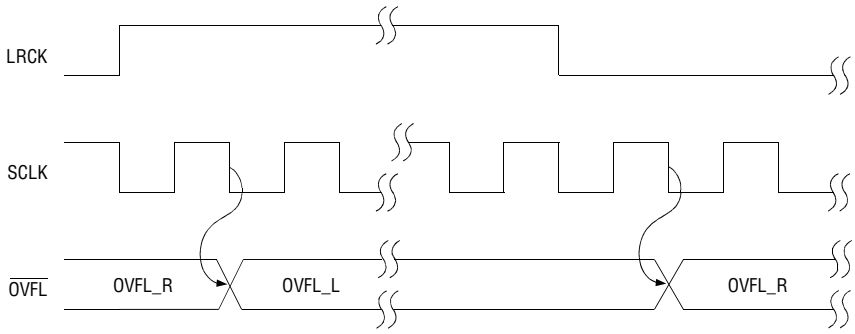


Figure 24. $\overline{\text{OVFL}}$ Output Timing, Left-Justified Format

5 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

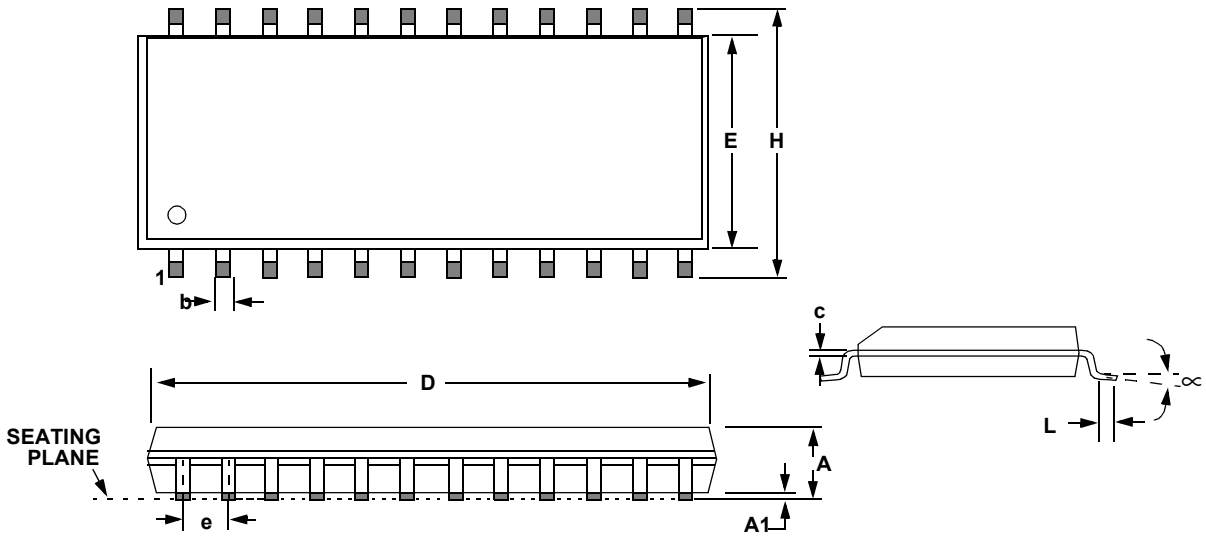
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

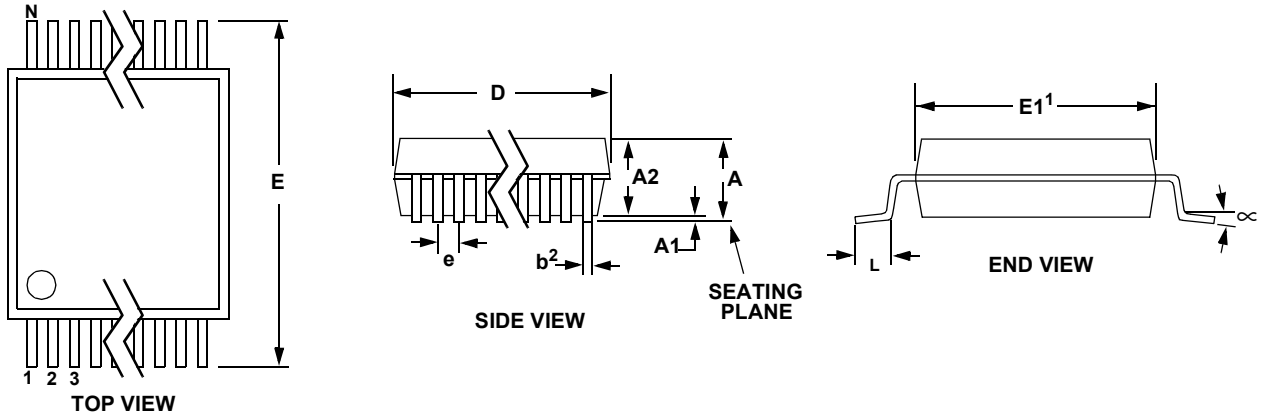
6 PACKAGE DIMENSIONS

24L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.303	0.307	0.311	7.70	7.80	7.90	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

7 ADDENDUM

The CS5351 and CS5361 family of analog-to-digital converters are functionally compatible and can easily be interchanged with minimal modifications to the input buffer circuitry.

Figure 25 shows an analog input buffer that provides anti-alias filtering, proper dc biasing, and optimum source impedance for the modulators. The input buffer shown will work well with both the CS5351 and the CS5361, merely by changing the bill of materials.

In order to use this buffer design with the CS5351, one would stuff the 0ohm resistors R19 and R22 and not populate R3 and R20. This will create a single-ended input buffer with the unused differential input pin connected to the quiescent voltage of the converter (VQ). Note that in this configuration, it is unnecessary to have the second op-amp and related components.

In order to use this buffer design with the CS5361, one would stuff the 0ohm resistors R3 and R20 and not populate R19 and R22. This will create a fully differential analog input buffer (as shown in Figure 3).

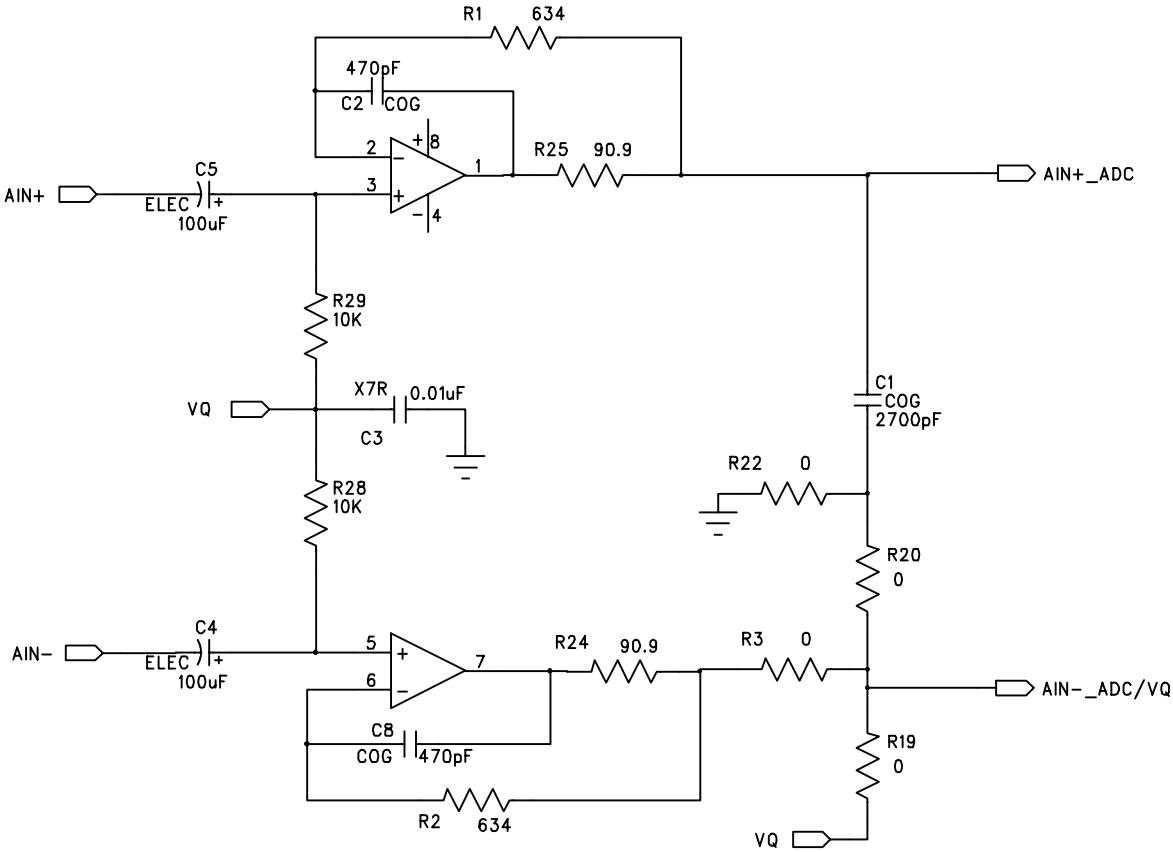


Figure 25. CS5351/CS5361 Analog Input Buffer