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Status	Product Specification
ECL Products	

100124/100124A

Hex TTL–to–ECL Translator

FEATURES

- **Typical propagation delay: 1.70ns**
- **Typical ECL supply current ($-I_{EE}$): 96mA for the 100124 and 71mA for the 100124A**
- **Typical TTL supply current (I_{TTL}): 44mA for the 100124 and 10mA for the 100124A**

DESCRIPTION

The 100124 is a hex translator that converts TTL logic levels to 100K ECL logic levels. When the common Enable (E) is Low, all true outputs are Low, and all inverting outputs are High. The differential outputs allow each circuit to be used as an inverting, noninverting, or differential line driver.

In differential operation, common mode rejection helps overcome ground offsets and transients between the 100124 and its receiver. V_{EE} and V_{TTL} may be applied in any order.

The 100124A is a low power version of the 100124. The only difference between the two parts are the limits of the ECL and TTL supply currents.

All unused inputs can be left open due to integrated pull–down resistors.

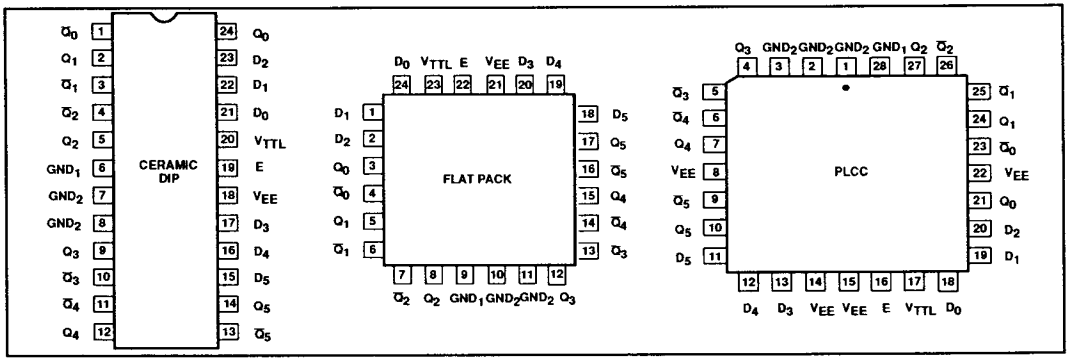
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs (TTL compatible)
E	Enable input (TTL compatible)
$Q_0 - Q_5$	True data outputs (100K ECL compatible)
$\overline{Q}_0 - \overline{Q}_5$	Complementary data outputs (100K ECL compatible)

ORDERING INFORMATION

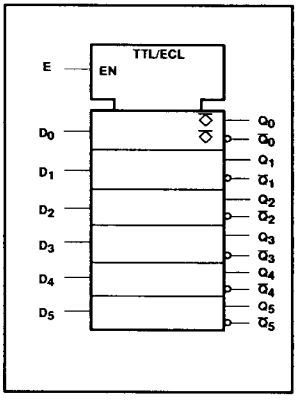
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100124F/100124AF
24–Pin Ceramic Flat Pack	100124Y/100124AY
28–Pin PLCC	100124A/100124AA

PIN CONFIGURATIONS

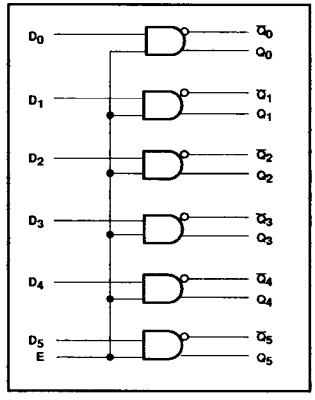


Translator | 100124/100124A

IEC/IEEE SYMBOL



LOGIC DIAGRAM

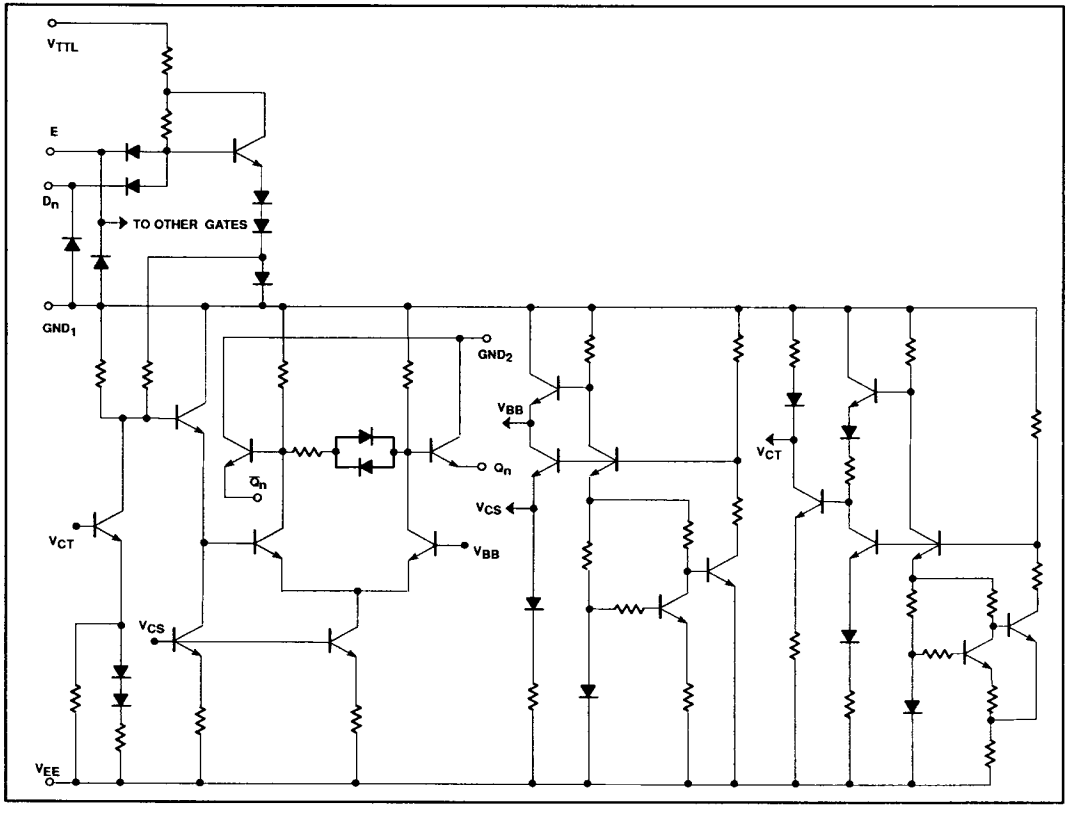


FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS	
E	D_n	Q_n	$\overline{Q}_n$
H	H	H	L
H	L	L	H
L	X	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$GND_1 = GND_2$ = ground, $T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{TTL}	TTL Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to V_{TTL}	V
I_{IN}	Input current	–30 to +5.0	mA
V_{EE}	ECL Supply voltage	–7.0 to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GND_1, GND_2	Circuit ground	0	0	0	V
V_{TTL}	TTL Supply voltage	+4.5	+5.0	+5.5	V
V_{EE}	ECL Supply voltage	–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family	–5.7			V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
T_A	Operating ambient temperature range	0	+25	+85	°C

NOTE:
When operating at other than the V_{EE} specified voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

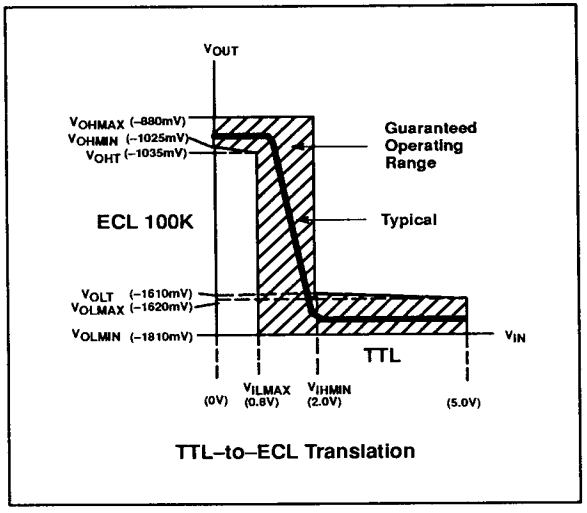
$GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	E, D_n = 2.4V, test Q_n	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			E, D_n = 2.0V, test Q_n	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			E, D_n = 0.8V, test Q_n	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			E, D_n = 0.4V, test Q_n	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
$-I_{EE}$	V_{EE} supply current	100124	All inputs ≥ V_{IHMIN}				96	140	mA
		100124A					71	90	mA
V_{IK}	Input clamp voltage	D_n inputs	Apply –18mA to one D_n, other inputs open.			–1.5			V
		E input	Apply –18mA to one E, other inputs open.			–1.5			V
I_I	Input current at maximum input voltage	D_n inputs	D_n input under test =+5.5V, other inputs = ground.					1.0	mA
		E input	E = +5.5V, other inputs = ground.					1.0	mA
I_{IH}	High level input current	D_n inputs	D_n input under test =+2.4V, other inputs = ground.					20	uA
		E input	E = +2.4V, other inputs = ground.					120	µA
$-I_{IL}$	Low level input current	D_n inputs	D_n input under test =+0.4V, other inputs = +2.4V.					1.6	mA
		E input	E = +0.4V, other inputs = +2.4V.					9.6	mA
I_{TTL}	TTL supply current	100124	All inputs at ground.				44	75	mA
		100124A					10	15	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

TRANSFER CHARACTERISTICS



TTL–to–ECL Translation

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	3.00 3.00	0.50 0.50	2.90 2.90	0.50 0.50	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	3.00 3.00	0.50 0.50	2.90 2.90	0.50 0.50	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	2.80 2.80	0.50 0.50	2.70 2.70	0.50 0.50	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

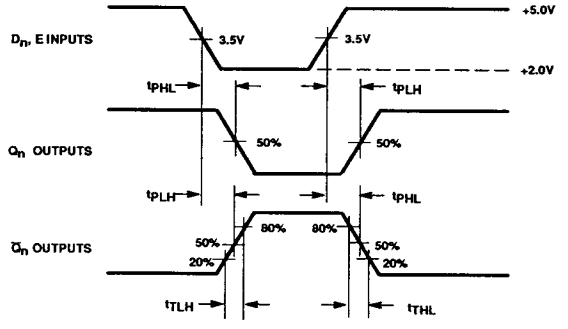
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	2.80 2.80	0.50 0.50	2.70 2.70	0.50 0.50	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

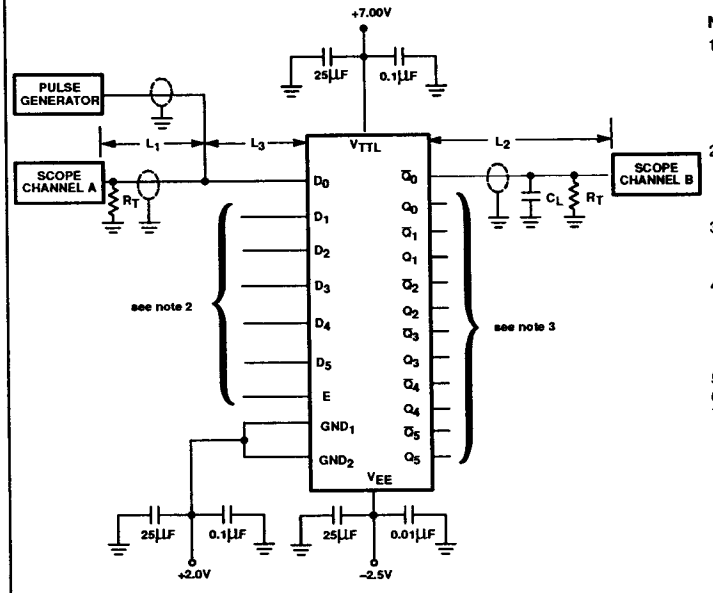
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

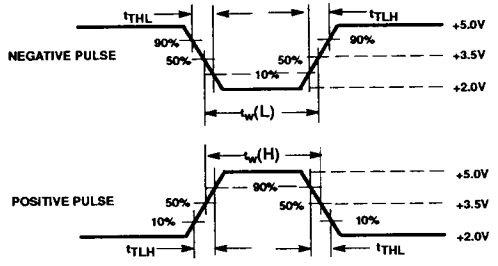
AC TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead length should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded with 50Ω to ground. The tolerance of all resistors should be ± 1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS

GND1 = GND2 = +2.0V ± 0.010V,
V_{EE} = −2.8V to −2.2V, V_{TTL} = +6.5V to +7.5V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.