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ECL Products	

100136

Counter/Shift Register

FEATURES

- **Typical propagation delay: 1.8ns**
- **Typical supply current ($-I_{EE}$): 210mA**

DESCRIPTION

The 100136 functions as a four–bit counter or as a 4–bit, bidirectional shift register. These functions are determined by the three Select Inputs $S_0 - S_2$, which also allow for parallel loading, as well as complementing, clearing and holding the register contents.

In the Parallel Load mode, data can be entered into the register via the Preset inputs ($P_0 - P_3$). Outputs $Q_0 - Q_3$ reflect the state of the register, $\overline{Q}_0 - \overline{Q}_3$ give the complement of that state. A High signal on the Master Reset input will clear the value of the register contents to zero asynchronously and without regard for signals at the other inputs.

When using the 100136 in the Count Up mode, the Terminal Count output ($\overline{TC}$) goes Low when the register reaches a value of 15. In the Count Down mode, $\overline{TC}$ goes Low when the register reaches a value of zero.

When operating the 100136 in the Right Shift mode, $D_0/\overline{CET}$ serves as the serial data input. In the Left Shift mode, D_3 serves as the serial input. When shifting, the $\overline{TC}$ output has the same level as the Q_3 output.

Two count enable inputs ($\overline{CEP}$ and $D_0/\overline{CET}$) can be used in combination with the $\overline{TC}$ output to cascade more than one 100136, allowing for counting and shift capability of eight bits or more. The dual nature of the $\overline{TC}/Q_3$ outputs and the $D_0/\overline{CET}$ input allow the same control lines, interconnected between stages, to be used for either the Count or the Right Shift operation.

Unused inputs must be tied to low voltage, either V_{IL} or V_{EE}.

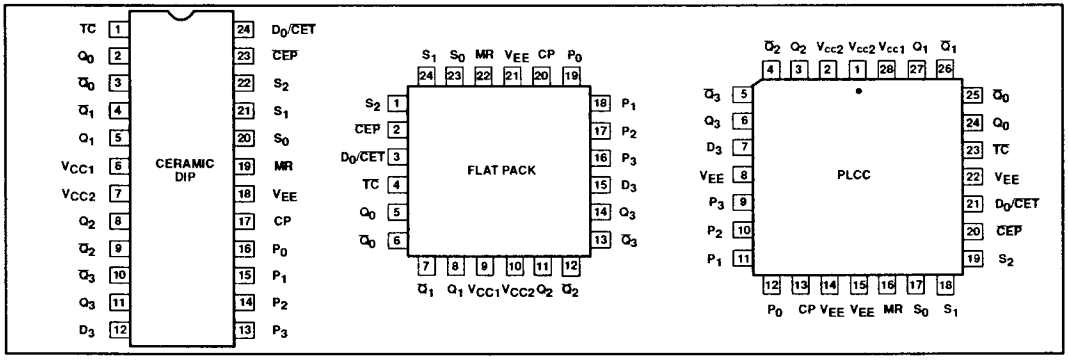
PIN DESCRIPTION

PINS	DESCRIPTION
D_3	Serial Data Inputs (Left Shift)
$P_0 - P_3$	Preset Inputs
CP	Clock Input
$D_0/\overline{CET}$	Serial Data Input (Right Shift) and Count Enable Trickle Input (Active–Low)
$\overline{CEP}$	Count Enable Parallel Input (Active–Low)
$S_0 - S_2$	Select Inputs
MR	Master Reset Input
$\overline{TC}$	Terminal Count Output
$Q_0 - Q_3$	Data Outputs

ORDERING INFORMATION

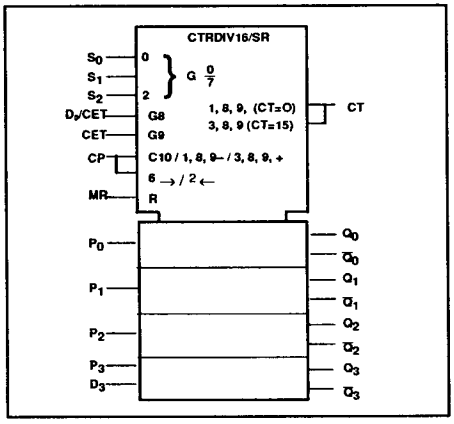
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100136F
24–Pin Ceramic Flat Pack	100136Y
28–Pin PLCC	100136A

PIN CONFIGURATIONS

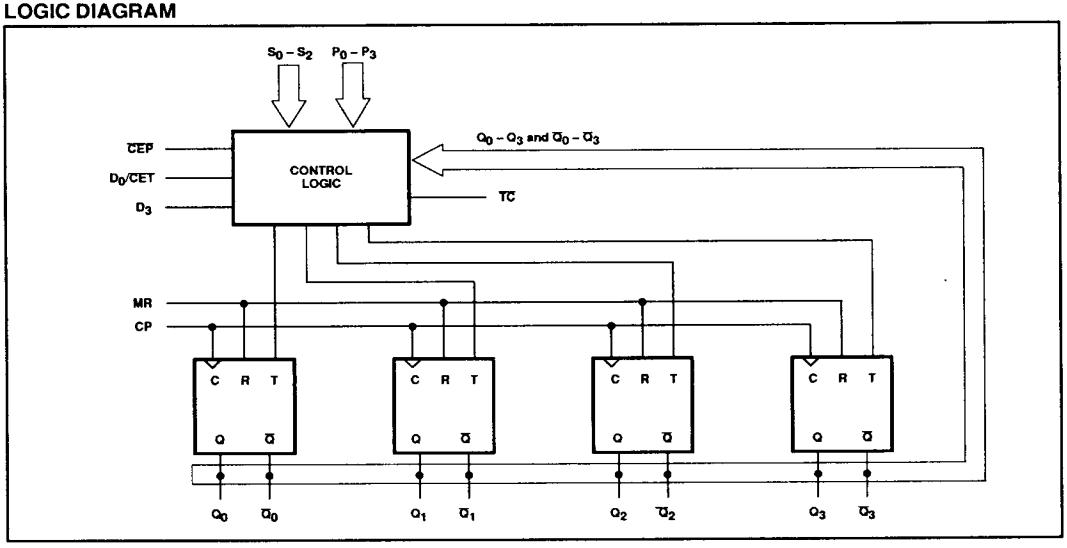


Counter/Shift Register | 100136

IEC/IEEE SYMBOL



LOGIC DIAGRAM



Counter/Shift Register 100136

FUNCTION TABLE

INPUTS								OUTPUTS					MODE
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	
L	L	L	L	X	X	X	↑	P_0	P_1	P_2	P_3	L	Parallel Load
L	L	L	H	X	X	X	↑	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Complement
L	L	H	L	X	X	L	↑	Q_1	Q_2	Q_3	L	L	Left Shift
L	L	H	L	X	X	H	↑	Q_1	Q_2	Q_3	H	H	(D_3 is the active serial input)
L	L	H	H	X	L	X	↑	L	Q_0	Q_1	Q_2	Q_2*	Right Shift
L	L	H	H	X	H	X	↑	H	Q_0	Q_1	Q_2	Q_2*	($D_0/\overline{CET}$ is the active serial input)
L	H	L	L	L	L	X	↑	(Q_{0-3}) minus 1				(1)	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	(1)	Count Down disabled with $\overline{CEP}$ High
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down disabled with $D_0/\overline{CET}$ High
L	H	L	H	X	X	X	↑	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↑	(Q_{0-3}) plus 1				(2)	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	(2)	Count Up disabled with $\overline{CEP}$ High
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up disabled with $D_0/\overline{CET}$ High
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTES:

(1) = L if $Q_0 - Q_3$ = LLLL, H if $Q_0 - Q_3 \neq$ LLLL
(2) = L if $Q_0 - Q_3$ = HHHH, H if $Q_0 - Q_3 \neq$ HHHH
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low–to–High transition
* Before the clock, $\overline{TC}$ is Q_3; after the clock, $\overline{TC}$ is Q_2

FUNCTION SELECT TABLE

S_2	S_1	S_0	FUNCTION
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Left Shift
L	H	H	Right Shift
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

NOTES:

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:

Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	P_n, S_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					180	µA
		$\overline{CEP}$						200	µA
		MR						240	µA
		D_3						280	µA
		CP						390	µA
		$D_0/\overline{CET}$						530	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			136	210	283	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage

NOTES (CONTINUED):

and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.

2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.10 2.10	0.85 0.85	2.10 2.10	0.85 0.85	2.25 2.25	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.80 4.80	1.80 1.80	4.60 4.60	1.80 1.80	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.95 2.95	1.35 1.35	2.95 2.95	1.20 1.20	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.80 4.80	2.10 2.10	4.80 4.80	2.10 2.10	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.20 3.20	1.40 1.40	3.20 3.20	1.40 1.40	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.20		0.20		0.20		ns
t_s	Setup time P_n to CP		1.70		1.70		1.70		ns
t_h	Hold time CP to P_n		0.10		0.10		0.10		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.20		0.20		0.20		ns
t_s	Setup time S_n to CP		3.80		3.80		3.80		ns
t_h	Hold time CP to S_n		–0.9		–0.9		–0.9		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.10 2.10	0.85 0.85	2.10 2.10	0.85 0.85	2.25 2.25	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.80 4.80	1.80 1.80	4.60 4.60	1.80 1.80	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.95 2.95	1.35 1.35	2.95 2.95	1.20 1.20	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.80 4.80	2.10 2.10	4.80 4.80	2.10 2.10	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.20 3.20	1.40 1.40	3.20 3.20	1.40 1.40	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.20		0.20		0.20		ns
t_s	Setup time P_n to CP		1.70		1.70		1.70		ns
t_h	Hold time CP to P_n		0.10		0.10		0.10		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.20		0.20		0.20		ns
t_s	Setup time S_n to CP		3.80		3.80		3.80		ns
t_h	Hold time CP to S_n		–0.9		–0.9		–0.9		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.15 2.15	0.85 0.85	2.15 2.15	0.85 0.85	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.60 4.60	1.80 1.80	4.40 4.40	1.80 1.80	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.75 2.75	1.35 1.35	2.75 2.75	1.20 1.20	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.60 4.60	2.10 2.10	4.60 4.60	2.10 2.10	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.00		0.00		0.00		ns
t_s	Setup time P_n to CP		1.60		1.60		1.60		ns
t_h	Hold time CP to P_n		0.00		0.00		0.00		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.00		0.00		0.00		ns
t_s	Setup time S_n to CP		3.60		3.60		3.60		ns
t_h	Hold time CP to S_n		−0.4		−0.4		−0.4		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

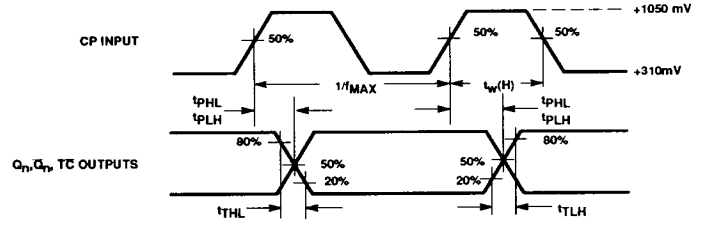
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.15 2.15	0.85 0.85	2.15 2.15	0.85 0.85	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.60 4.60	1.80 1.80	4.40 4.40	1.80 1.80	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.75 2.75	1.35 1.35	2.75 2.75	1.20 1.20	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.60 4.60	2.10 2.10	4.60 4.60	2.10 2.10	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.00		0.00		0.00		ns
t_s	Setup time P_n to CP		1.60		1.60		1.60		ns
t_h	Hold time CP to P_n		0.00		0.00		0.00		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.00		0.00		0.00		ns
t_s	Setup time S_n to CP		3.60		3.60		3.60		ns
t_h	Hold time CP to S_n		−0.4		−0.4		−0.4		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

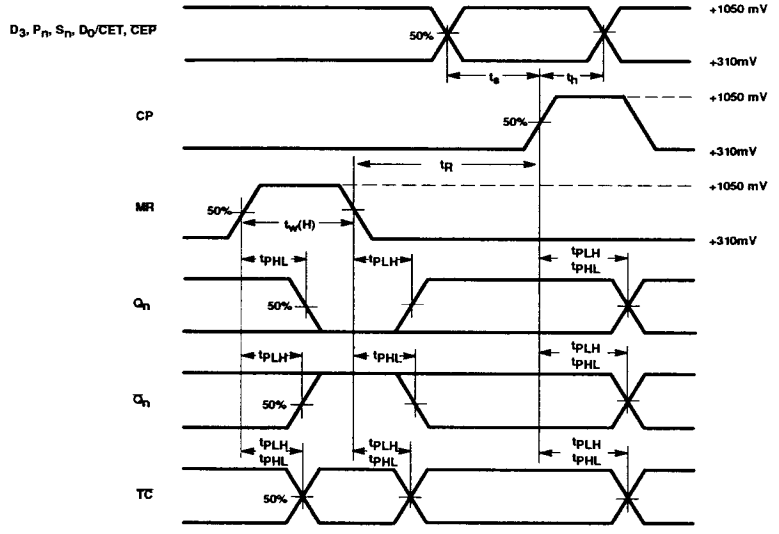
AC WAVEFORMS



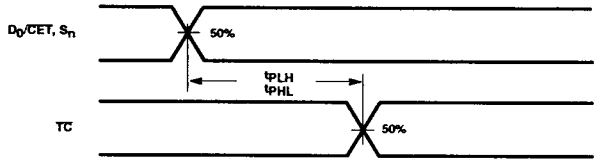
Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

AC WAVEFORMS



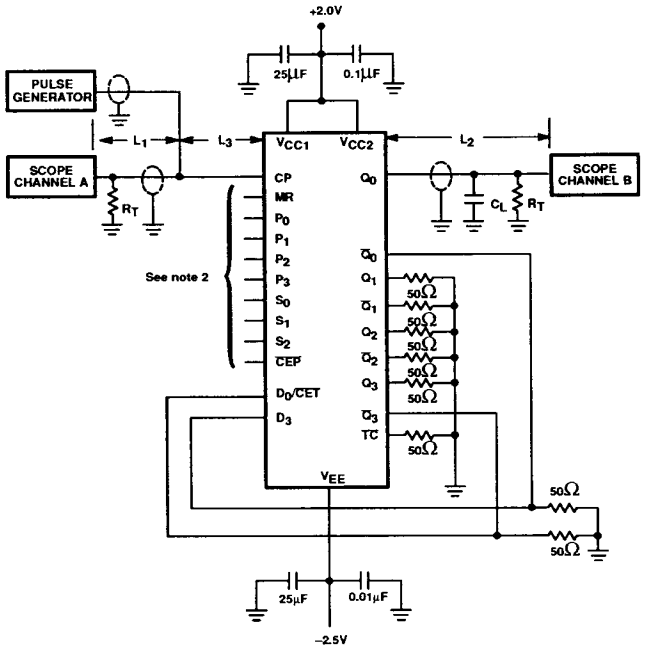
Waveform 2. Reset, Setup and Hold Times



Waveform 3. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

SHIFT FREQUENCY TEST CIRCUIT

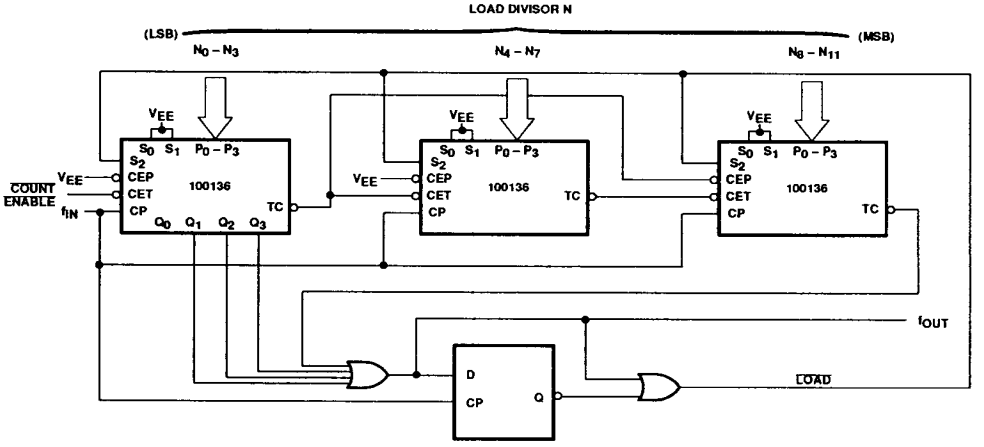


NOTES:

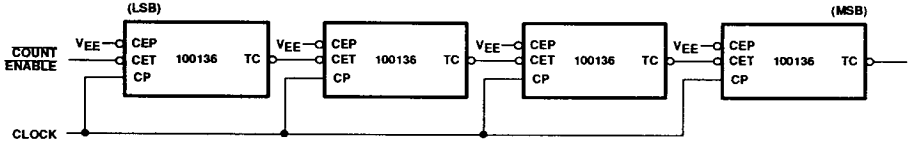
1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.
9. While S_0 through S_2 are set fo Parallel Load mode, a four–bit word is entered at inputs P_0 through P_3. Then, So through S2 can be set for Right shift or Left Shift mode, whereby a bit pattern will advance across the outputs with every rising edge of the clock pulse CP. The wires connecting $\overline{Q}_0$ to D_3 and $\overline{Q}_3$ to D_0/CET ensure circular shifting and should be as short as possible. The shift frequency is determined from the bit pattern as seen by Scope Channel B.

APPLICATION CIRCUITS

3–STAGE DIVIDER USING PARALLEL LOAD AND COUNT DOWN MODES



SLOW EXPANSION SCHEME FOR COUNTING AND RIGHT SHIFT



FAST EXPANSION SCHEME FOR COUNTING